MPC850 PBGA PIN ASSIGNMENT (JEDEC)

PIN	NAME	PIN	NAME
B2	VSSSYN	C2	VDDSYN
B3	VSSSYN1	C3	XFC
B4	KAPWR	C4	PORESET
B5	XTAL	C5	SRESET
B6	EXTAL	C6	HRESET
B7	EXTCLK	C7	OP3/MODCK2/DSDO
B8	VDDL	C8	KR/IRQ4/SPKROUT
B9	IP_B0/IWP0/VFLS0	C9	ALE_B/DSCK/AT1
B10	IP_B3/IWP2/VF2	C10	IP_B4/LWP0/VF0
B11	FRZ/IRQ6	C11	BURST
B12	BB	C12	BR
B13	TA	C13	BI
B14	BDIP/GPL_B5	C14	UPWAITB/GPL_B4
B15	CS1	C15	CS2
B16	CS3	C16	CS7/CE2_B
B17	NC	C17	CS4
D2	NC	E2	CLKOUT
D3	DP3/IRQ6	E3	D30
D4	DP0/IRQ3	E4	DP2/IRQ5
D5	WAIT_B	E5	DP1/IRQ4
D6	RSTCONF	E6	TEXP
D7	NC	E7	MODCK1/OP2/STS
D8	IP_B6/DSDI/AT0	E8	IP_B2/IOIS16_B/AT2
D9	IP_B1/IWP1/VFLS1	E9	IP_B7/PTR/AT3
D10	IP_B5/LWP1/VF1	E10	IRQ2/RSV
D11	BG	E11	TS
D12	TEA	E12	UPWAITA/GPL_A4/AS
D13	GPL_A5	E13	CS0
D14	RD/WR	E14	CS5
D15	CS6/CE1_B	E15	GPL_A3/GPL_B3
D16	GPL_A2/GPL_B2	E16	WE2/BS_AB2/PCOE
D17	OE/GPL_A1/GPL_B1	E17	WE0/BS_AB0/IORD

PIN	NAME	PIN	NAME
F2	D7	G2	D6
F3	D29	G3	D21
F4	D31	G4	D24
F5	D26	G5	D28
F6	VDDH	G6	VDDH
F7	VDDH	G7	GND
F8	VDDH	G8	GND
F9	VDDH	G9	GND
F10	VDDH	G10	GND
F11	VDDH	G11	GND
F12	VDDH	G12	GND
F13	VDDH	G13	VDDH
F14	GPL_A0/GPL_B0	G14	WE3/BS_AB3/PCWE
F15	NC	G15	A26
F16	TSIZ1	G16	TSIZ0/REG
F17	WE1/BS_AB1/IOWR	G17	A31
H2	VDDL	J2	D5
H3	D19	J3	D16
H4	D20	J4	D18
H5	D25	J5	D22
H6	VDDH	J6	VDDH
H7	GND	J7	GND
H8	GND	J8	GND
H9	GND	J9	GND
H10	GND	J10	GND
H11	GND	J11	GND
H12	GND	J12	GND
H13	VDDH	J13	VDDH
H14	A18	J14	A24
H15	A22	J15	A25
H16	A30	J16	A23
H17	A28	J17	A29
K2	D3	L2	D11
K3	D2	L3	D9
K4	D14	L4	D10
K5	D15	L5	D17
K6	VDDH	L6	VDDH
K7	GND	L7	GND
K8	GND	L8	GND
K9	GND	L9	GND
K10	GND	L10	GND
K11	GND	L11	GND
K12	GND	L12	GND
K13	VDDH	L13	VDDH
K14	NC	L14	A17
K15	A21	L15	A16
K16	A20	L16	A19
K17	VDDL	L17	A27

PIN	NAME	PIN	NAME
M2	D1	N2	D0
M3	D4	N3	D8
M4	D27	N4	D13
M5	D23	N5	D12
M6	VDDH	N6	VDDH
M7	GND	N7	VDDH
M8	GND	N8	VDDH
M9	GND	N9	VDDH
M10	GND	N10	VDDH
M11	GND	N11	VDDH
M12	GND	N12	VDDH
M13	VDDH	N13	VDDH
M14	A10	N14	A6
M15	A13	N15	A12
M16	A14	N16	A9
M17	A15	N17	A11
P2	IRQ0	R2	NC
P3	IRQ1	R3	PD[5]/UTPB[6]
P4	IRQ7	R4	PD[4]/UTPB[7]
P5	PD[3]/SOC	R5	PD[9]/UTPCLK
P6	PD[11]/RXENB	R6	PD[13]/UTPB[2]
P7	PC[6]/USBTXN	R7	PC[5]/L1TSYNCA/SDACK1/CTS3
P8	PB[17]/L1ST3	R8	PB[18]/RTS2/L1ST2
P9	PC[8]/CD2/TGATE1	R9	PA[6]/CLK2/TOUT1/TIN3
P10	NC	R10	PC[10]/TGATE1/USBRXN
P11	PA[9]/L1TXDA/SMRXD2	R11	NC
P12	PB[25]/SMTXD1/TXD3	R12	TRST
P13	TDO/DSDO	R13	PB[26]/I2CSCL/BRGO2
P14	NC	R14	PC[13]/L1ST7/RTS3
P15	PB[31]/SPISEL	R15	PB[29]/SPIMOSI/RXD3
P16	A7	R16	PB[30]/SPICLK/TXD3
P17	A8	R17	PA[15]/USBRXD
T2	PD[6]/UTPB[5]	U2	PD[8]
T3	PD[7]/UTPB[4]	U3	PD[10]/TXENB
T4	PD[12]/ UTPB[3]	U4	PD[14]/UTPB[1]
T5	PD[15]/UTPB[0]	U5	PC[4]/L1RSYNCA/CD3
T6	PB[16]/L1RQA/L1ST4	U6	PC[7]/USBTXP
T7	PA[4]/CLK4/TOUT2/TIN4	U7	PA[5]/CLK3/BRGO2/L1TCLKA/TIN2
T8	PB[19]/L1ST1	U8	VDDL
T9	PC[9]/CTS2	U9	PA[7]/CLK1/BRGO1/L1RCLKA/TIN1
T10	PB[22]/SDACK2/SMSYN2	U10	PA[8]/L1RXDA/SMTXD2
T11	PC[11]/USBRXP	U11	PB[23]/SDACK1/SMSYN1
T12	TDI/DSDI	U12	PB[24]/SMRXD1/RXD3
T13	TMS	U13	TCK/DSCK
T14	PA[12]/TXD2	U14	PC[12]/TXCAV/L1RQA/L1ST8
T15	PA[13]/RXD2	U15	PB[27]/I2CSDA/BRGO1
T16	PA[14]/USBOE	U16	PB[28]/SPIMISO/BRGO3
T17	PC[15]/RXCAV/DREQ1/L1ST5	U17	PC[14]/DREQ2/RTS2/L1ST6