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Application Note

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i.MX 8M Quad Power Consumption Measurement

1. Introduction

This application note helps you to design power management systems. It illustrates the current drain measurements of the i.MX 8M application processors taken on the NXP EVK platform through several use cases. You may choose the appropriate power supply domains for the i.MX 8M Quad chips and become familiar with the expected chip power in various scenarios.

Because the data presented in this application note is based on empirical measurements taken on a small sample size, the presented results are not guaranteed.

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2. Overview of i.MX 8M Quad voltage supplies

The i.MX 8M Quad processors have several power supply domains (voltage supply rails) and several internal power domains. Figure 1 shows the connectivity of these supply rails and the distribution of the internal power domains.

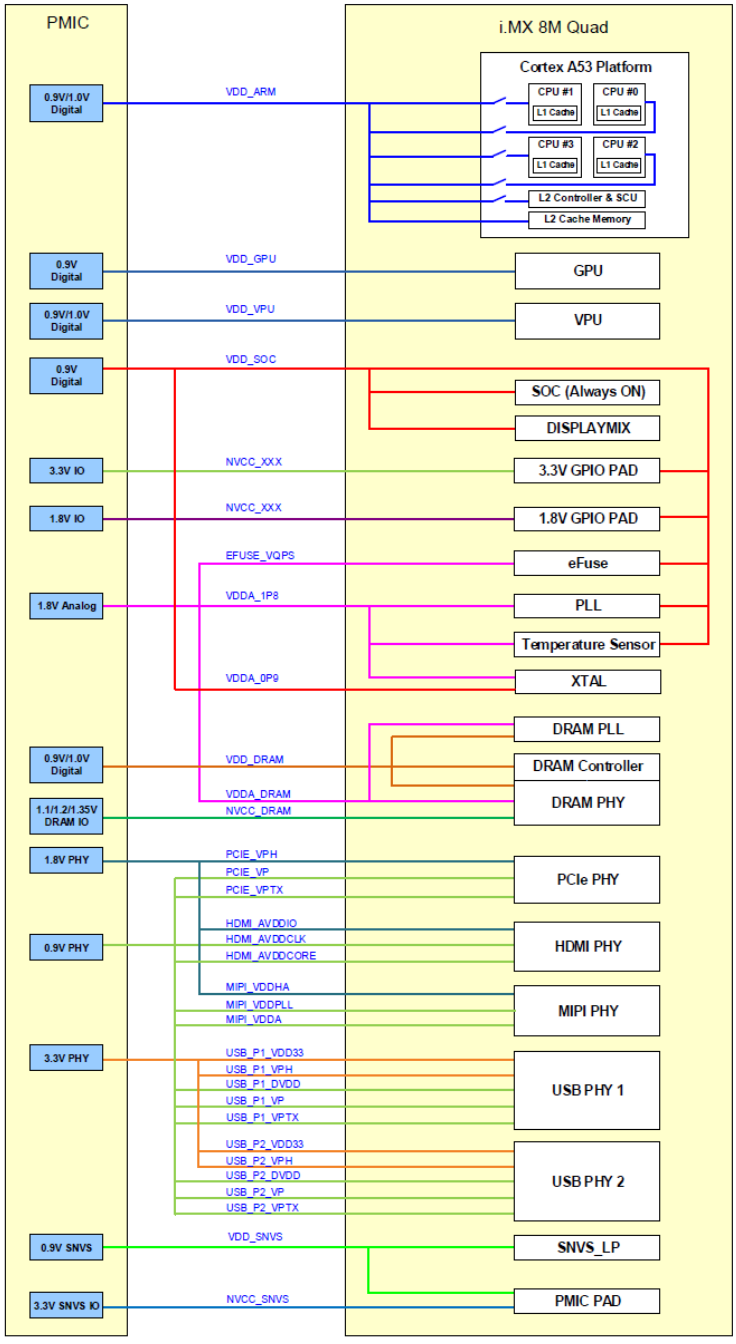

Figure 1. i.MX8M Quad power rails

NOTE

See the *i.MX 8M Quad datasheet for consumer products* (document IMX8MDQLQCEC) for the recommended operating conditions of each supply rail and for a detailed description of the groups of pins that are powered by each I/O voltage supply. For more information about the i.MX 8M Quad power rails, see the "Power Management Unit (PMU)" chapter in the *i.MX 8M Quad Applications Processor Reference Manual* (document IMX8MDQLQRM).

Figure 2 is a snippet from the IMX8M Quad EVK Board schematic showing the power distribution.

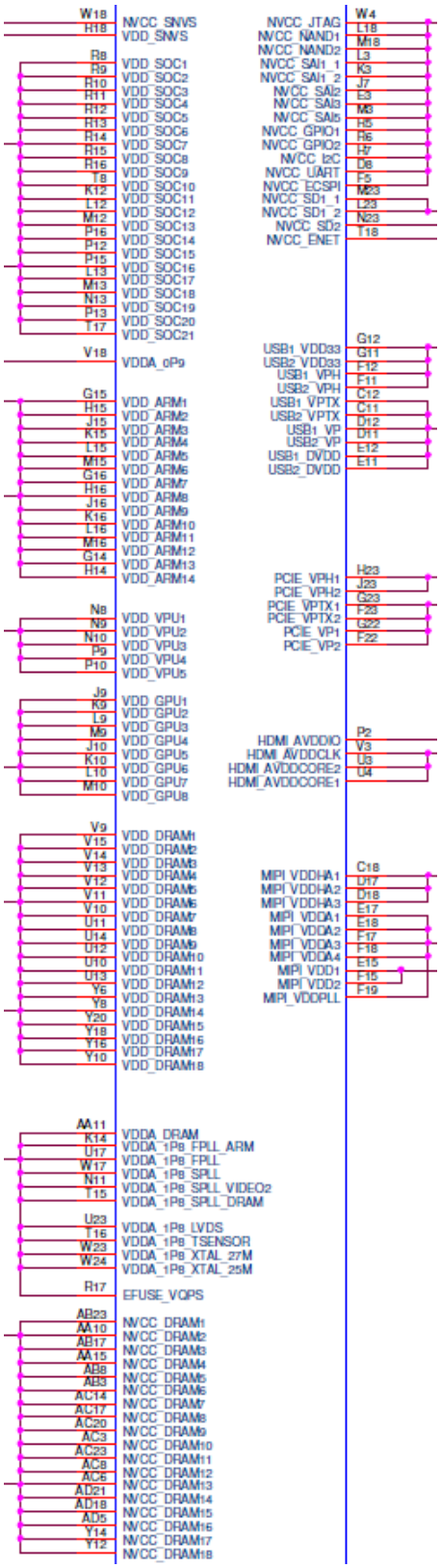

Figure 2. IMX 8M Quad power schematic

3. Internal power measurement of the i.MX 8M Quad processor

Several use cases (described in Section 6, "Use Case Configuration and Usage Guidelines") are run on the EVK platform (Revision D). The measurements are taken mainly for these power supply domains:

- VDD_ARM: ARM® Cortex®-A53 Quad cores supply.
- VDD_SOC: SoC logic supply.
- VDD_GPU: GPU power supply.
- VDD_DRAM: DRAM controller, PHY, and PLL power supply.
- VDD_VPU: VPU power supply.
- NVCC_DRAM: DRAM IO power supply (including an external DDR device).

These supply domains consume the majority of the processor's internal power. For relevant use cases, the power of additional supply domains is added. However, the power of these supply domains does not depend on specific use cases, but on whether these modules are used or not. The power consumption of the SNVS is comparatively negligible (except for the Deep-Sleep Mode).

The NVCC_* power consumption depends primarily on the board-level configuration and the components. Therefore, it is not included in the i.MX 8M Quad internal power analysis.

The power consumption of these supplies (in different use cases) is provided in Table 2 through to Table 33.

NOTE

Unless stated otherwise, all measurements were taken on a typical process silicon, at a room temperature (approximately 25 °C).

3.1. VDDA_1P8 power

The VDDA_1P8 voltage domain is generated from the PMIC. This domain powers these circuits:

- On-chip oscillators (OSC25M, OSC27M).
- eFuse power supplies.
- Analog part of the PLLs.
- Temperature sensor.

3.2. DDR I/O power

The DDR I/O is supplied from the NVCC_DRAM which provides the power for the DDR I/O pads. The target voltage for this supply depends on the DDR interface used. The target voltages for the different DDR interfaces are:

- 1.35 V for DDR3L.
- 1.2 V for DDR4/LPDDR3.
- 1.1 V for LPDDR4.

The power consumption of the NVCC_DRAM supply is affected by various factors, including these:

- The amount of activity on the DDR interface.
- On-Die Termination (ODT): enabled/disabled, termination value, which is used for the DDR controller and the DDR memories.
- The board termination for the DDR control and the address bus.
- The configuration of the DDR pads (such as the drive strength).
- The board layout.
- The load of the DDR memory devices.

NOTE

Due to the factors specified in the previous paragraph, the measurements provided in the following tables vary from one system to another. The provided data is for guidance only and should not be treated as a specification.

The measured current on the EVK Platform also includes the current of the on-board LPDDR4 memory devices.

3.3. Voltage levels in the measurement process

The voltage levels of all the supplies (except for VDD_ARM, VDD_GPU, and VDD_VPU) are set to the typical voltage levels, as defined in the *i.MX 8M Quad data sheet for consumer products* (document IMX8MDQLQCEC).

The VDD_ARM, VDD_GPU, and VDD_VPU supplies require special explanation. To save power, these power voltages are changed during the run time of the use cases. The voltage levels of these supplies can be changed to standby voltage levels in low-power modes.

3.3.1. VDD_ARM/VDD_GPU/VDD_VPU voltage levels

The target voltage levels of the VDD_ARM may vary for different modes according to the use cases. The modes are the nominal mode and the overdrive mode. There are several factors that contribute to the mode decisions, with the module load being the most important. The other factors are module latency requirements, thermal restrictions, and peripheral I/O performance requirements. The voltage levels used for the measurements are provided in Table 1.

NOTE

See the operating ranges table in the *i.MX 8M Quad data sheet for consumer products* (document IMX8MDQLQCEC) for the official operating points.

Most of the measurements are performed using these voltage levels and the power data that appears in this document is according to these values. If the measurement is done at different voltage levels, the power consumption scales change with the voltage. In real applications, the software (in conjunction with the hardware) automatically adjusts the voltage and frequency values based on the use case requirements.

The voltage used for the power calculation is the average voltage between those set-points. It depends on the amount of time spent at each set-point.

3.3.2. VDD_SOC voltage levels

See the operating ranges table in the *i.MX 8M Quad data sheet for consumer products* (document IMX8MDQLQCEC) for the official operating points.

Table 1. VDDARM/VDDGPU/VDDVPU voltage levels (for reference only)

Power rail	Vmin (V)	Vtyp (V)	Vmax (V)	Description
VDD_ARM	0.810	0.900	1.05	Nominal mode
	0.900	1.000	1.050	Overdrive mode
VDD_GPU	0.810	0.900	1.05	Nominal mode
	0.900	1.000	1.100	Overdrive mode
VDD_VPU	0.810	0.900	1.05	Nominal mode
	0.900	1.000	1.100	Overdrive mode

3.4. Temperature measurements

In some use cases, the die temperature is measured. The temperature measurements were taken using the on-chip temperature sensor. While measuring the temperature, it is recommended to wait until the temperature stabilizes.

NOTE

The measured temperatures are for reference only and vary on different systems due to the differences in the board, enclosure, and heat spreading techniques. When using the same board type, the measured temperature may vary due to factors such as the environment, silicon variations, and measurement errors.

3.5. Hardware and software used

The software versions used for the measurements are:

- Yocto rootfs, Linux Kernel version: L4.9.51 8MQ.
- The board used for the measurements is the i.MX 8M EVK platform.
- The measurements were performed using the 34470A 6½ digital multimeter.

3.6. Measuring points on the EVK platform

To measure the power, you must do the rework first. All the power rails needed to be measured have components named SH*, where * is the designator number of the component. These components are just copper, so you need to split the connect, then solder an 0.025 Ω sensor resistor (shunt). The power data is obtained by measuring the average voltage drop over the measurement points and dividing it by the resistor value to determine the average current. The tolerance of the 0.025 Ω resistors you use should be 1 %. The measuring points for the various supply domains are as follows:

- VDD_ARM: The A53 ARM complex current is measured on SH709. For the low-power measurements, the resistance value is 0.025 Ω.
- VDD_SOC: The chip domain current is measured on SH708. The recommended resistance value for this measurement is 0.025 Ω.
- VDD_GPU: The chip domain current is measured on SH701. The recommended resistance value for this measurement is 0.025 Ω.
- VDD_VPU: The chip domain current is measured on SH702. The recommended resistance value for this measurement is 0.025 Ω.
- VDD_DRAM: The chip domain current is measured on SH704. The recommended resistance value for this measurement is 0.025 Ω.
- LPDDR4 I/O plus memories: The current in this domain includes the NVCC_DRAM current and the overall current of the on-board LPDDR4 memory devices. The current in this domain is measured on SH703 and the recommended resistance value for this measurement is 0.025 Ω.

4. Use cases and measurement results

The main use cases and subtypes, which form the benchmarks for the i.MX 8M Quad internal power measurements on the EVK platform, are described in the following sections.

A 4K TV display was used only for the GPU and Video Playback use cases.

4.1. Low-power mode use cases

The use-case scenarios that have been tested are:

- Deep Sleep Mode with HDMI (DSM_HDMI).
- Deep Sleep Mode with MIPI-DSI (DSM_MIPI)—changed the default ***fdt_file****=fsl-imx8mq-evk-lcdif-adv7535.dtb*.
- IDLE_DDRC_167MHz with HDMI (IDLE with DDR data rate of 667 MT/s with HDMI).
- IDLE_DDRC_167MHz with MIPI-DSI (IDLE with DDR data rate of 667 MT/s with MIPI-DSI).
- IDLE_ DDRC_800MHz with HDMI (DDR data rate of 3200 MT/s with HDMI).
- IDLE_ DDRC_800MHz with MIPI-DSI (DDR data rate of 3200 MT/s with MIPI-DSI).

4.1.1. Deep-Sleep Mode (DSM) with HDMI

Boot up the platform and enter DSM mode after login.

This mode is called either “Dormant mode” or “Suspend-To-RAM” in the Linux BSP. This is the lowest possible power state where the external supplies are still on.

The use case is as follows:

- The ARM platform is power-gated.
- The L2 Cache peripheral are power-gated.
- The M4 is in the reset status.

- All PLL (Phase-Locked Loop) and CCM (Clock Controller Module) generated clocks are off.
- The CKIL (32 kHz) input is on.
- All of the modules are disabled.
- The external high-frequency crystal and the on-chip oscillator are powered down (by asserting the SBYOS bit in the CCM).
- The VDD_ARM is in overdrive mode with 1V rail voltage.

The following table shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 2. Deep-Sleep Mode with HDMI

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.997	**15.101**	15.056
VDD_ SOC	0.895	**67.580**	60.484
VDD_GPU	0.000	**0.000**	0.000
VDD_VPU	0.000	**0.000**	0.000
VDD_DRAM	0.000	**0.000**	0.000
NVCC_DRAM	1.100	**1.586**	1.745
Total power	—	—	**77.285**

1. VDD_ARM power consumption is caused by board design limitation, this power rail can be powered off during this power mode.

For additional details about this use case and settings, see Section 6, “Use Case Configuration and Usage Guidelines”.

4.1.2. Deep-Sleep Mode (DSM) with MIPI-DSI

When powering or rebooting the platform, in U-Boot stage modify default dtb file to *fsl-imx8mq-evk-lcdif-adv7535.dtb*:

```
setenv fdt_file "fsl-imx8mq-evk-lcdif-adv7535.dtb"
saveenv
```

and then proceed just like in HDMI IDLE use case for entering DSM.

Table 3 shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 3. Deep-Sleep Mode with MIPI-DSI

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.997	**15.946**	15.899
VDD_ SOC	0.894	**98.162**	87.806
VDD_GPU	0.000	**0.000**	0.000
VDD_VPU	0.000	**0.000**	0.000
VDD_DRAM	0.000	**0.000**	0.000
NVCC_DRAM	1.100	**1.610**	1.771
Total power	—	—	**105.476**

1. VDD_ARM power consumption is caused by board design limitation, this power rail can be powered off during this power mode.

For additional details on this use case and settings, see Section 6, "Use Case Configuration and Usage Guidelines".

4.1.3. IDLE_DDRC_167MHz with HDMI

DDRC clock frequency was set from 800MHz (default) down to 167MHz using steps in Section 6, "Use Case Configuration and Usage Guidelines".

Power governor was the default one, *conservative*, and CPU clock frequency was 1GHz.

The use case is as follows:

- The ARM A53 CORE is power-gated if the kernel is in the lowest level of idle.
- The ARM L2 cache and PLAT are power on.
- The M4 is in the reset status.
- All the unused PLLs are off, unused clocks are gated.
- The VPU, GPU, and DISPMIX are in low power mode.
- The operating system is on.

Table 4 shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 4. IDLE_DDRC_167MHz with HDMI

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.896	**54.139**	48.492
VDD_SOC	0.893	**182.880**	163.311
VDD_GPU	0.000	**0.000**	0.000
VDD_VPU	0.000	**0.000**	0.000
VDD_DRAM	0.996	**143.893**	143.250
NVCC_DRAM	1.094	**38.855**	42.512
Total power	—	—	**397.565**

1. Die temperature wasn't logged because it impacts default governor and will set CPU clock frequency at 1.5 GHz.
2. DDRC clock frequency in IDLE mode was set to 167MHz instead of 25MHz in GA software release, which may slightly increase the power consumption. Please refer to the chip errata for more details.

4.1.4. IDLE_DDRC_167MHz with MIPI-DSI

For this use case, a MIPI-DSI to HDMI card adapter was connected to the EVK DSI port and no display was attahed to the HDMI port of the card.

Default .dtb file must be changed in U-boot as following:

```
setenv fdt_file "fsl-imx8mq-evk-lcdif-adv7535.dtb"
saveenv
```

After booting up the platform and login, follow the procedure from Section 6, "Use Case Configuration and Usage Guidelines" to change DDRC clock from 800MHz down to 167MHz.

The use case is as follows:

- The ARM A53 CORE is power-gated if the kernel is in the lowest level of idle.
- The ARM L2 cache and PLAT are power on.

- The M4 is in the reset status.
- All the unused PLLs are off, unused clocks are gated.
- The VPU, GPU, and DISPMIX are in low power mode.
- The operating system is on.

Table 5 shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 5. IDLE_DDRC_167MHz with MIPI-DSI

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.896	**35.357**	31.685
VDD_SOC	0.893	**201.114**	179.575
VDD_GPU	0.000	**0.000**	0.000
VDD_VPU	0.000	**0.000**	0.000
VDD_DRAM	0.996	**144.500**	143.871
NVCC_DRAM	1.094	**38.611**	42.239
Total power	—	—	**397.370**

1. Die temperature wasn't logged because it impacts default governor (conservative) and will set CPU clock frequency at 1.5GHz.
2. DDRC clock frequency in IDLE mode was set to 167MHz instead of 25MHz in GA software release, which may slightly increase the power consumption. Please refer to the chip errata for more details.

4.1.5. IDLE_ DDRC_800MHz with HDMI

Boot up the platform with default configuration file (.dtb), log in and check that CPU frequency is 1GHz. After validation, measure power on specific rail.

No display was connected to the HDMI platform's port.

The use case is as follows:

- The ARM A53 CORE is power-gated if the kernel is in the lowest level of idle.
- The ARM L2 cache and PLAT are power on.
- The M4 is in the reset status.
- All the unused PLLs are off, unused clocks are gated.
- The operating system is on.

Table 6 shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 6. IDLE_DDRC_800MHz with HDMI

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.895	65.799	58.921
VDD_SOC	0.892	265.095	236.336
VDD_GPU	0.000	0.000	0.000
VDD_VPU	0.000	0.000	0.000
VDD_DRAM	0.989	439.594	434.713
NVCC_DRAM	1.094	60.438	66.090
Total power	—	—	**796.060**

1. Die temperature wasn't logged because it impacts default governor(conservative) and will set CPU clock frequency at 1.5GHz.

For additional details on this use case and settings, see Section 6, “Use Case Configuration and Usage Guidelines”.

4.1.6. IDLE_DDRC_800MHz with MIPI-DSI

For this use case, a MIPI-DSI to HDMI card adaptor was connected to the EVK DSI port with no display attached to it.

Default .dtb file must be changed in U-boot as following:

```
setenv fdt_file “fsl-imx8mq-evk-lcdif-adv7535.dtb”
saveenv
```

Boot up the platform with the new configuration (.dtb), log in and check that CPU frequency is 1GHz. After validation, measure power on specific rail.

The use case is as follows:

- The ARM A53 CORE is power-gated if the kernel is in the lowest level of idle.
- The ARM L2 cache and PLAT are power on.
- The M4 is in the reset status.
- All the unused PLLs are off, unused clocks are gated.
- The operating system is on.

Table 7 shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 7. IDLE_DDRC_800MHz with MIPI-DSI

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.895	**66.37258**	59.430
VDD_SOC	0.891	**279.6247**	249.223
VDD_GPU	0.000	**0.000**	0.000
VDD_VPU	0.000	**0.000**	0.000
VDD_DRAM	0.993	**253.8376**	252.185
NVCC_DRAM	1.094	**60.52359**	66.196
Total power	—	—	627.034

1. Die temperature wasn’t logged because it impacts default governor(conservative) and will set CPU clock frequency at 1.5GHz.

For additional details on this use case and settings, see Section 6, “Use Case Configuration and Usage Guidelines”.

4.2. Audio_Playback, M4 idle

The use-case scenarios that have been tested are:

- Audio_Playback(gplay)_DDRC_167MHz with HDMI
- Audio_Playback(gplay)_DDRC_167MHz with MIPI-DSI
- Audio+Video_Playback with HDMI
- Audio+Video_Stream with HDMI

4.2.1. Audio_Playback(gplay)_DDRC_167MHz with HDMI

For this use case, *fsl-imx8mq-evk.dtb* configuration file was used.

DDRC clock frequency was set to 167MHz using Section 6, "Use Case Configuration and Usage Guidelines".

The audio file used was an mp3 file with 128kbps bit rate at 44kHz sample rate/s, and played using the following options:

```
gplay-1.0 $audio_file --video-sink=fakesink
```

The use case is as follows:

- The ARM A53 CORE is power-gated if the kernel is in the lowest level of idle.
- The ARM L2 cache and PLAT are power on.
- The M4 is in the reset status.
- The VPU, GPU, and DISPMIX are in low power mode.
- All the unused PLLs are off, unused clocks are gated.
- The operating system is on.

Table 8. Audio_Playback(gplay)_DDRC_167MHz with HDMI

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.896	**65.363**	58.535
VDD_SOC	0.893	**198.930**	177.568
VDD_GPU	0.000	**0.000**	0.000
VDD_VPU	0.000	**0.000**	0.000
VDD_DRAM	0.994	**232.172**	230.858
NVCC_DRAM	1.094	**61.941**	67.742
Total power	—	—	**534.702**

1. Die temperature was logged approx at **38 ^{0}C (**avg.); Ambient temperature is approx. **25 ^{0}C.**
   `cat /sys/class/thermal/thermal_zone0/temp` was used to log temperature, during the audio file play.

For additional details on this use case and settings, see Section 6, "Use Case Configuration and Usage Guidelines".

4.2.2. Audio_Playback(gplay)_DDRC_167MHz with MIPI-DSI

For this use case, .dtb configuration file was changed to `fsl-imx8mq-evk-lcdif-adv7535.dtb`, and DDRC clock frequency was set to 167MHz using Section 6, "Use Case Configuration and Usage Guidelines".

The audio file used was an mp3 file with 128kbps bit rate at 44kHz sample rate/s using the following options:

```
gplay-1.0 $audio_file --video-sink=fakesink
```

The use case is as follows:

- The ARM A53 CORE is power-gated if the kernel is in the lowest level of idle.
- The ARM L2 cache and PLAT are power on.
- The M4 is in the reset status.

- The VPU, GPU, and DISPMIX are in low power mode.
- All the unused PLLs are off, unused clocks are gated.
- The operating system is on.

Table 9. Audio_Playback(gplay)_DDRC_167MHz with MIPI-DSI

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.896	**50.958**	45.653
VDD_SOC	0.893	**211.288**	188.600
VDD_GPU	0.000	**0.000**	0.000
VDD_VPU	0.000	**0.000**	0.000
VDD_DRAM	0.995	**167.814**	167.036
NVCC_DRAM	1.093	**59.317**	64.856
Total power	—	—	**466.144**

2. Die temperature was logged approx at **39 ^{0}C (**avg.); Ambient temperature is approx. **25 ^{0}C.**
   `cat /sys/class/thermal/thermal_zone0/temp` was used to log temperature, during the audio file play.

For additional details on this use case and settings, see Section 6, “Use Case Configuration and Usage Guidelines”.

4.2.3. Audio+Video_Playback with HDMI

For this use case, default dtb configuration file was used and HDMI port was connected to a 4K TV display.

Video file used for playback is mkv file format compressed with HEVC standard with full HD resolution at 60 fps and the audio encoding is AACL with 48kHz samples/s with 6ch configuration.

Video file was locally played with *gst-launch-1.0* play, with the following options:

```
/usr/bin/gst-launch-1.0 playbin uri=file://$PATH/$FILE video-sink="kmssink sync=false"
```

The use case is as follows:

- The ARM A53 CORE is power-gated if the kernel is in the lowest level of idle.
- The ARM L2 cache and PLAT are power on.
- The M4 is in the reset status.
- All the unused PLLs are off, unused clocks are gated.
- The operating system is on.

Table 10. Audio+Video_Playback with HDMI

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.993	**244.523**	242.900
VDD_SOC	0.884	**620.806**	548.539
VDD_GPU	0.000	**0.000**	0.000
VDD_VPU	0.995	**178.130**	177.249
VDD_DRAM	0.990	**459.610**	454.851
NVCC_DRAM	1.088	**346.174**	376.514
Total power	—	—	**1800.054**

1. Die temperature was logged approx at **48 ^{0}C (**avg.); Ambiental temperature is approx. **25 ^{0}C.**
   `cat /sys/class/thermal/thermal_zone0/temp` was used to log temperature, during the video play.

For additional details on this use case and settings, see Section 6, "Use Case Configuration and Usage Guidelines".

4.2.4. Audio+Video_Stream with HDMI

For this use case, default dtb configuration file was used and HDMI port was connected to a 4K TV display.

Video file used for playback is mkv file format compressed with HEVC standard with full HD resolution at 60 fps and the audio encoding is AACL in 6 channels configuration with 48kHz samples/s.

A server was setup for hosting the mkv video file for streaming;

Video streaming was done using Ethernet adapter and the player used is gplay-1.0:

```
gplay-1.0 $FILE
```

The use case is as follows:

- The ARM A53 CORE is power-gated if the kernel is in the lowest level of idle.
- The ARM L2 cache and PLAT are power on.
- The M4 is in the reset status.
- All the unused PLLs are off, unused clocks are gated.
- The operating system is on.

Table 11. Audio+Video_Stream with HDMI

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.993	**253.389**	251.667
VDD_SOC	0.883	**638.592**	564.015
VDD_GPU	0.011	**1.445**	0.016
VDD_VPU	0.995	**172.614**	171.817
VDD_DRAM	0.989	**460.762**	455.849
NVCC_DRAM	1.088	**350.053**	380.686
Total power	—	—	**1824.050**

1. Die temperature was logged approx at **49 ^{0}C (**avg.); Ambient temperature is approx. **25 ^{0}C.**
   `cat /sys/class/thermal/thermal_zone0/temp` was used to log temperature, during the video play.

For additional details on this use case and settings, see Section 6, "Use Case Configuration and Usage Guidelines".

4.3. Core benchmark

The use-case scenarios that have been tested are:

- 4-core Dhrystone
- 4-core Whetstone
- C-Ray
- Coremark

4.3.1. 4-core Dhrystone

Dhrystone is a synthetic benchmark used to measure the integer computational performance of processors and compilers. The small size of the Dhrystone benchmark enables it to fit into the L1 cache and minimizes accesses to the L2 cache and DDR.

In this use case, the Dhrystone test is performed by 4 Cortex-A53 cores (because dhrystone is a single thread benchmark, 4 instances were started). All Cortex-A53 cores run the test in a loop at a frequency of 1496 MHz.

- The DDRC clock is 800 MHz.
- The NOC clock is 800 MHz
- The AXI clock is 333 MHz.
- The AHB clock is 133 MHz.
- The IPG clock is 66 MHz.

Table 12 shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 12. 4-core Dhrystone

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.978	**1117.924**	1092.912
VDD_SOC	0.892	**227.508**	202.977
VDD_GPU	0.000	**0.000**	0.000
VDD_VPU	0.000	**0.000**	0.000
VDD_DRAM	0.995	**175.148**	174.332
NVCC_DRAM	1.094	**39.470**	43.182
Total power	—	—	**1513.403**

1. Die temperature was logged approx at **49 ^{0}C (**avg.); Ambient temperature is approx. **25 ^{0}C.**
   `cat /sys/class/thermal/thermal_zone0/temp` was used to log temperature, during the benchmark run

4.3.2. 4-core Whetstone

Whetstone is a similar benchmark for integer and string operations like Dhrystone. The Whetstone is also a synthetic benchmark which primarily measures the floating-point arithmetic performance.

In this use case, the Whetstone test is performed by 4 Cortex-A53 cores (because Whetstone is a single thread benchmark too, 4 instances were started). All Cortex-A53 cores run the test in a loop at a frequency of 1496MHz.

- CPU frequency governor is set to `performance` (CPU frequency is set to maximum value)
- DDRC frequency is set to 800 MHz

Table 13 shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 13. 4-core Whetstone

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.982	**877.448**	861.579
VDD_SOC	0.892	**225.953**	201.622
VDD_GPU	0.000	**0.000**	0.000
VDD_VPU	0.000	**0.000**	0.000
VDD_DRAM	0.995	**197.666**	196.708
NVCC_DRAM	1.095	**42.221**	46.211
Total power	—	—	**1306.120**

1. Die temperature was logged approx at **46 ^{0}C (**avg.); Ambient temperature is approx. **25 ^{0}C.**
   `cat /sys/class/thermal/thermal_zone0/temp` was used to log temperature, during the benchmark run

4.3.3. C-Ray

C-Ray is an extremely simple ray-tracer which is not representative of any real world raytracing application. In fact, it is essentially a floating point benchmark that runs out the L1-cache. That said, it is not as synthetic and meaningless as Whetstone, as you can actually use the software to do simple raytracing.

This is a multithread benchmark and the default test scene involves only a small amount of data, such that on most systems the CPU does not have to access main RAM to run the test.

- CPU frequency governor is set to `performance` (CPU frequency is set to maximum value)
- DDRC frequency is set to 800 MHz

Table 14 shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 14. C-Ray

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.985	**708.613**	697.953
VDD_SOC	0.891	**281.899**	251.149
VDD_GPU	0.000	**0.000**	0.000
VDD_VPU	0.000	**0.000**	0.000
VDD_DRAM	0.990	**446.821**	442.310
NVCC_DRAM	1.093	**103.461**	113.105
Total power	—	—	**1504.517**

1. Die temperature was logged approx at **48 ^{0}C (**avg.); Ambient temperature is approx. **25 ^{0}C.**
   `cat /sys/class/thermal/thermal_zone0/temp` was used to log temperature, during the benchmark run

4.3.4. Coremark

CoreMark is a modern, sophisticated benchmark that lets you accurately measure processor performance and is intended to replace the older Dhrystone benchmark. ARM recommends using CoreMark in preference to Dhrystone.

For best performances compile with:

```
-O2 -DMULTITHREAD=4 -DUSE_PTHREAD -lpthread -O3 -funroll-all-loops
--param max-inline-insns-auto=550 -ftracer -falign-jumps=16 -ftree-loop-im -fivopts
-ftree-loop-ivcanon -fvect-cost-model -fvariable-expansion-in-unroller
--param max-unrolled-insns=999999 --param max-average-unrolled-insns=99999999
--param iv-max-considered-uses=9999999 --param iv-consider-all-candidates-bound=99999
--param iv-always-prune-cand-set-bound=999999   -fmodulo-sched
-fmodulo-sched-allow-regmoves -fgcse-lm -fgcse-sm -fgcse-las -funsafe-loop-optimizations
-freschedule-modulo-scheduled-loops  -ftree-vectorize -DPERFORMANCE_RUN=1   -lrt
```

- CPU frequency governor is set to *performance* (CPU frequency is set to maximum value)
- DDRC frequency is set to 800 MHz

Table 15 shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 15. Coremark

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.981	**935.448**	917.499
VDD_SOC	0.892	**224.319**	200.122
VDD_GPU	0.000	**0.000**	0.000
VDD_VPU	0.000	**0.000**	0.000
VDD_DRAM	0.995	**176.596**	175.727
NVCC_DRAM	1.094	**41.799**	45.748
Total power	—	—	**1339.095**

1. Die temperature was logged approx at **48 ^{0}C (**avg.); Ambient temperature is approx. **25 ^{0}C.**
   `cat /sys/class/thermal/thermal_zone0/temp` was used to log temperature, during the benchmark run

4.4. GPU

The use-case scenarios that have been tested are:

- MM07
- MM06

MM07 and MM06 are 3D gaming benchmarks. The graphics are loaded from the SD card into the DDR (double data rate) memory, processed by the GPU3D, then copied to display buffer in the DDR. It is then taken by DCSS and displayed on the HDR 4K display (through HDMI).

- CPU frequency governor is set to `performance` (CPU frequency is set to maximum value)
- DDRC frequency is set to 800 MHz

4.4.1. MM07

Table 16 shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 16. GPU_MM07

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.993	**294.260**	292.082
VDD_SOC	0.883	**649.113**	573.052
VDD_GPU	0.796	**439.673**	349.988
VDD_VPU	0.000	**0.000**	0.000
VDD_DRAM	0.989	**523.635**	517.778
NVCC_DRAM	1.086	**384.236**	417.314
Total power	—	—	**2150.213**

1. Die temperature was logged approx at **56 ^{0}C(**avg.); Ambient temperature is approx. **25 ^{0}C.**
   `cat /sys/class/thermal/thermal_zone0/temp` was used to log temperature, during the benchmark run

4.4.2. MM06

Table 17 shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 17. GPU_MM06 mode measurement results

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.992	**316.044**	313.607
VDD_SOC	0.883	**656.363**	579.309
VDD_GPU	0.892	**733.452**	654.578
VDD_VPU	0.000	**0.000**	0.000
VDD_DRAM	0.987	**584.174**	576.590
NVCC_DRAM	1.086	**440.703**	478.423
Total power	—	—	**2602.508**

1. Die temperature was logged approx at **56 ^{0}C(**avg.); Ambient temperature is approx. **25 ^{0}C.**
   `cat /sys/class/thermal/thermal_zone0/temp` was used to log temperature, during the benchmark run

4.5. Heavy load use cases

The use-case scenarios that have been tested are:

- VPU
- 4-core Dhryst + VPU + Taiji
- 4-core Memtest + VPU + Taiji
- 4-core Streamcpy + VPU + Taiji

The purpose of these use cases is to provide the power consumption for heavy load use cases to show the power consumption in extreme conditions.

4.5.1. VPU

This use case has the following features:

- HDR 4K display ON, 3840 x 2160, 60Hz
- 4K file decode via Hantro G2 decoder
- (`g2dec -P -Ers -ibs -N200 -X ../4K_HEVC_80Mbps_brazil_4096x2160.hevc`)
- CPU frequency governor was set to *`performance`* (CPU frequency is set to maximum value)
- DDRC frequency is set to 800 MHz Table 18 shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 18. VPU

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.988	**553.526**	546.728
VDD_SOC	0.884	**592.114**	523.594
VDD_GPU	0.000	**0.000**	0.000
VDD_VPU	0.995	**171.324**	170.535
VDD_DRAM	0.991	**392.080**	388.578
NVCC_DRAM	1.091	**218.685**	238.487
Total power	—	—	**1867.922**

1. Die temperature was logged approx at **48 ^{0}C(**avg.); Ambient temperature is approx. **25 ^{0}C.**
   `cat /sys/class/thermal/thermal_zone0/temp` was used to log temperature, during the benchmark run

4.5.2. 4-core Dhryst + VPU + Taiji

This use case runs in parallel 4.3.1 & 4.5.1 & 4.4.1.

- CPU frequency governor was set to *`performance`* (CPU frequency is set to maximum value)
- DDRC frequency is set to 800 MHz

Table 19 shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 19. 4-core Dhryst + VPU + Taiji

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.976	**1193.359**	1164.748
VDD_SOC	0.882	**697.829**	615.393
VDD_GPU	0.845	**503.930**	425.592
VDD_VPU	0.994	**161.015**	159.982
VDD_DRAM	0.987	**548.142**	541.227
NVCC_DRAM	1.087	**399.451**	434.042
Total power	—	—	**3340.984**

1. Die temperature was logged approx at **62 ^{0}C(**avg.); Ambient temperature is approx. **25 ^{0}C.**
   `cat /sys/class/thermal/thermal_zone0/temp` was used to log temperature, during the benchmark run

4.5.3. 4-core Memtest + VPU + Taiji

This use case runs in parallel memtester (an effective userspace tester for stress-testing the memory subsystem) & 4.5.1 & 4.4.1.

- CPU frequency governor was set to `performance` (CPU frequency is set to maximum value)
- DDRC frequency is set to 800 MHz

Table 20 shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 20. 4-core Memtest + VPU + Taiji

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.980	**981.514**	961.992
VDD_SOC	0.882	**700.569**	617.678
VDD_GPU	0.892	**504.801**	450.426
VDD_VPU	0.993	**154.190**	153.122
VDD_DRAM	0.986	**588.259**	580.164
NVCC_DRAM	1.084	**540.729**	585.990
Total power	—	—	**3349.372**

1. Die temperature was logged approx at **60 ^{0}C(**avg.); Ambient temperature is approx. **25 ^{0}C.**
   `cat /sys/class/thermal/thermal_zone0/temp` was used to log temperature, during the benchmark run

4.5.4. 4-core Streamcpy + VPU + Taiji

This use case run in parallel streamcpy (4.6.3) & 4.5.1 & 4.4.1.

- CPU frequency governor was set to `performance` (CPU frequency is set to maximum value)
- DDRC frequency is set to 800 MHz

Table 21 shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 21. 4-core Streamcpy + VPU + Taiji mode measurement results

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.981	**926.245**	908.766
VDD_SOC	0.882	**691.739**	609.942
VDD_GPU	0.892	**466.743**	416.261
VDD_VPU	0.994	**153.758**	152.760
VDD_DRAM	0.986	**585.019**	577.089
NVCC_DRAM	1.083	**504.122**	546.074
Total power	—	—	**3210.892**

1. Die temperature was logged approx. at **60 ^{0}C(**avg.); Ambient temperature is approx. **25 ^{0}C.**
   `cat /sys/class/thermal/thermal_zone0/temp` was used to log temperature, during the benchmark run

4.6. Memory

The use-case scenarios that have been tested are:

- Memset
- Memcpy
- Stream

Memset and Memcpy are part of perf-bench (a general framework for benchmark suites).

4.6.1. Memset

Suite for evaluating performance of simple memory set in various ways.

- The size of the memory buffers was set to 1000MB
- CPU frequency governor was set to `performance` (CPU frequency is set to maximum value)
- DDRC frequency is set to 800 MHz

Table 22 shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 22. Memset

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.994	**232.940**	231.482
VDD_SOC	0.892	**214.934**	191.778
VDD_GPU	0.000	**0.000**	0.000
VDD_VPU	0.000	**0.000**	0.000
VDD_DRAM	0.994	**247.229**	245.740
NVCC_DRAM	1.088	**323.276**	351.736
Total power	—	—	**1020.736**

1. Die temperature was logged approx at **42 ^{0}C(**avg.); Ambient temperature is approx. **25 ^{0}C.**
   `cat /sys/class/thermal/thermal_zone0/temp` was used to log temperature, during the benchmark run

4.6.2. Memcpy

Suite for evaluating performance of simple memory copy in various ways.

- The size of the memory buffers was set to 1000MB
- CPU frequency governor was set to `performance` (CPU frequency is set to maximum value)
- DDRC frequency is set to 800 MHz

Table 23 shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 23. Memcpy

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.993	**250.935**	249.260
VDD_SOC	0.892	**205.786**	183.655
VDD_GPU	0.000	**0.000**	0.000
VDD_VPU	0.000	**0.000**	0.000
VDD_DRAM	0.994	**224.073**	222.712
NVCC_DRAM	1.091	**196.705**	214.524
Total power	—	—	**870.150**

1. Die temperature was logged approx at **41 ^{0}C(**avg.); Ambiental temperature is approx. **25 ^{0}C.**
   `cat /sys/class/thermal/thermal_zone0/temp` was used to log temperature, during the benchmark run

4.6.3. Stream

The STREAM benchmark is a simple synthetic benchmark program that measures sustainable memory bandwidth (in MB/s) and the corresponding computation rate for simple vector kernels.

- The stream array size was set to 102400000 elements
- All phases were included (Copy, Scale, Add & Triad)
- CPU frequency governor was set to `performance` (CPU frequency is set to maximum value)
- DDRC frequency is set to 800 MHz

Table 24 shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 24. Stream

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.986	**656.804**	647.488
VDD_SOC	0.892	**220.123**	196.375
VDD_GPU	0.000	**0.000**	0.000
VDD_VPU	0.000	**0.000**	0.000
VDD_DRAM	0.993	**227.984**	226.463
NVCC_DRAM	1.089	**291.095**	317.079
Total power	—	—	**1387.406**

1. Die temperature was logged approx at **45 ^{0}C(**avg.); Ambient temperature is approx. **25 ^{0}C.**
   `cat /sys/class/thermal/thermal_zone0/temp` was used to log temperature, during the benchmark run

4.7. Storage – SDHC class10

The use-case scenarios that have been tested are:

- DD_RD_SDCARD
- DD_WRT_SDCARD
- IO_WRT_SDCARD

4.7.1. DD_RD_SDCARD

- CPU frequency governor was set to `performance` (CPU frequency is set to maximum value)
- DDRC frequency is set to 800 MHz

Table 25 shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 25. DD_RD_SDCARD

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.994	**222.779**	221.492
VDD_SOC	0.891	**271.308**	241.775
VDD_GPU	0.000	**0.000**	0.000
VDD_VPU	0.000	**0.000**	0.000
VDD_DRAM	0.989	**445.396**	440.570
NVCC_DRAM	1.092	**151.179**	165.042
Total power	—	—	**1068.879**

1. Die temperature was logged approx at **43 ^{0}C(**avg.); Ambient temperature is approx. **25 ^{0}C.**
   `cat /sys/class/thermal/thermal_zone0/temp` was used to log temperature, during the benchmark run

4.7.2. DD_WRT_SDCARD

- Set the maximum amount of data that the kernel reads ahead for a single file to 512KB
- (`echo 512 > /sys/block/<bdev>/queue/read_ahead_kb`)
- CPU frequency governor was set to `performance` (CPU frequency is set to maximum value)
- DDRC frequency is set to 800 MHz

Table 26 shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 26. DD_WRT_SDCARD

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.996	**143.681**	143.044
VDD_SOC	0.891	**261.289**	232.904
VDD_GPU	0.000	**0.000**	0.000
VDD_VPU	0.000	**0.000**	0.000
VDD_DRAM	0.989	**438.283**	433.658
NVCC_DRAM	1.093	**78.524**	85.857
Total power	—	—	**895.463**

1. Die temperature was logged approx. **42 ^{0}C (**avg.); Ambient temperature is approx. **25 ^{0}C.**
   `cat /sys/class/thermal/thermal_zone0/temp` was used to log temperature, during the benchmark run

4.7.3. IO_WRT_SDCARD

- Set the maximum amount of data that the kernel reads ahead for a single file to 512KB
- (`echo 512 > /sys/block/<bdev>/queue/read_ahead_kb`)
- CPU frequency governor was set to `performance` (CPU frequency is set to maximum value)
- DDRC frequency is set to 800 MHz

Table 27 shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 27. IO_WRT_SDCARD

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.996	**129.495**	0.129
VDD_SOC	0.891	**261.008**	0.233
VDD_GPU	0.000	**0.000**	0.000
VDD_VPU	0.000	**0.000**	0.000
VDD_DRAM	0.990	**438.036**	0.434
NVCC_DRAM	1.094	**77.900**	0.085
Total power	—	—	**0.880**

1. Die temperature was logged approx. **41 ^{0}C(**avg.); Ambient temperature is approx. **25 ^{0}C.**
   `cat /sys/class/thermal/thermal_zone0/temp` was used to log temperature, during the benchmark run

4.8. Storage – eMMC

The use-case scenarios that have been tested are:

- DD_RD_eMMC
- DD_WRT_eMMC
- IO_WRT_eMMC

4.8.1. DD_RD_eMMC

- Set the maximum amount of data that the kernel reads ahead for a single file to 512KB
- (`echo 512 > /sys/block/<bdev>/queue/read_ahead_kb`)
- CPU frequency governor was set to `performance` (CPU frequency is set to maximum value)
- DDRC frequency is set to 800 MHz

Table 28 shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 28. DD_RD_eMMC mode measurement results

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.993	**209.700**	208.175
VDD_SOC	0.891	**278.725**	248.362
VDD_GPU	0.000	**0.000**	0.000
VDD_VPU	0.000	**0.000**	0.000
VDD_DRAM	0.989	**453.833**	448.923
NVCC_DRAM	1.092	**152.416**	166.427
Total power	—	—	**1071.886**

1. Die temperature was logged approx. **41 ^{0}C(**avg.); Ambient temperature is approx. **25 ^{0}C.**
   `cat /sys/class/thermal/thermal_zone0/temp` was used to log temperature, during the benchmark run

4.8.2. DD_WRT_eMMC

- Set the maximum amount of data that the kernel reads ahead for a single file to 512KB
- (`echo 512 > /sys/block/<bdev>/queue/read_ahead_kb`)
- CPU frequency governor was set to `performance` (CPU frequency is set to maximum value)
- DDRC frequency is set to 800 MHz

Table 29 shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 29. DD_WRT_eMMC

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.990	**150.452**	148.942
VDD_SOC	0.891	**271.679**	242.123
VDD_GPU	0.000	**0.000**	0.000
VDD_VPU	0.000	**0.000**	0.000
VDD_DRAM	0.989	**440.038**	435.245
NVCC_DRAM	1.093	**71.516**	78.182
Total power	—	—	**904.492**

1. Die temperature was logged approx. **41 ^{0}C(**avg.); Ambient temperature is approx. **25 ^{0}C.**
   `cat /sys/class/thermal/thermal_zone0/temp` was used to log temperature, during the benchmark run

4.8.3. IO_WRT_eMMC

- Set the maximum amount of data that the kernel reads ahead for a single file to 512 KB
- (`echo 512 > /sys/block/<bdev>/queue/read_ahead_kb`)
- CPU frequency governor was set to `performance` (CPU frequency is set to maximum value)
- DDRC frequency is set to 800 MHz

Table 30 shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 30. IO_WRT_eMMC

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.996	**128.947**	128.367
VDD_SOC	0.891	**274.012**	244.265
VDD_GPU	0.000	**0.000**	0.000
VDD_VPU	0.000	**0.000**	0.000
VDD_DRAM	0.989	**443.600**	438.776
NVCC_DRAM	1.093	**94.647**	103.446
Total power	—	—	**914.854**

1. Die temperature was logged approx. **41 ^{0}C (**avg.); Ambient temperature is approx. **25 ^{0}C.**
   `cat /sys/class/thermal/thermal_zone0/temp` was used to log temperature, during the benchmark run

4.9. Storage – USB 3.0

The use-case scenarios that have been tested are:

- DD_RD_USB3.0
- DD_WRT_ USB3.0
- IO_WRT_ USB3.0

4.9.1. DD_RD_USB3.0

- Set the maximum amount of data that the kernel reads ahead for a single file to 512 KB
- (`echo 512 > /sys/block/<bdev>/queue/read_ahead_kb`)
- CPU frequency governor was set to `performance` (CPU frequency is set to maximum value)
- DDRC frequency is set to 800 MHz

Table 31 shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 31. DD_RD_ USB3.0

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.993	**237.642**	235.864
VDD_SOC	0.891	**302.628**	269.514
VDD_GPU	0.000	**0.000**	0.000
VDD_VPU	0.000	**0.000**	0.000
VDD_DRAM	0.989	**453.811**	448.818
NVCC_DRAM	1.092	**144.866**	158.165
Total power	—	—	**1112.361**

1. Die temperature was logged approx. **47 ^{0}C (**avg.); Ambient temperature is approx. **25.5 ^{0}C.**
   `cat /sys/class/thermal/thermal_zone0/temp` was used to log temperature, during the benchmark run

4.9.2. DD_WRT_ USB3.0

- Set the maximum amount of data that the kernel reads ahead for a single file to 512 KB
- (`echo 512 > /sys/block/<bdev>/queue/read_ahead_kb`)
- CPU frequency governor was set to `performance` (CPU frequency is set to maximum value)
- DDRC frequency is set to 800 MHz

Table 32 shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 32. DD_WRT_USB3.0

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.995	**180.169**	179.271
VDD_SOC	0.891	**305.419**	271.997
VDD_GPU	0.000	**0.000**	0.000
VDD_VPU	0.000	**0.000**	0.000
VDD_DRAM	0.989	**457.098**	452.110
NVCC_DRAM	1.092	**115.935**	126.630
Total power	—	—	**1030.008**

1. Die temperature was logged approx. **46 ^{0}C (**avg.); Ambient temperature is approx. **25 ^{0}C.**
   `cat /sys/class/thermal/thermal_zone0/temp` was used to log temperature, during the benchmark run

4.9.3. IO_WRT_ USB3.0

- Set the maximum amount of data that the kernel reads ahead for a single file to 512 KB
- (`echo 512 > /sys/block/<bdev>/queue/read_ahead_kb`)
- CPU frequency governor was set to `performance` (CPU frequency is set to maximum value)
- DDRC frequency is set to 800 MHz

Table 33 shows the measurement results when this use case is applied on the i.MX 8M Quad processor.

Table 33. IO_WRT_ USB3.0

Supply domain	Voltage (V)	L4.9.51-MX8	
		I (mA)	P (mW)
VDD_ARM	0.995	**176.078**	175.168
VDD_SOC	0.891	**271.009**	241.549
VDD_GPU	0.000	**0.000**	0.000
VDD_VPU	0.000	**0.000**	0.000
VDD_DRAM	0.989	**439.566**	434.815
NVCC_DRAM	1.094	**60.535**	66.195
Total power	—	—	**917.726**

1. Die temperature was logged approx. **45 ^{0}C (**avg.);.; Ambient temperature is approx. **25 ^{0}C.**
   `cat /sys/class/thermal/thermal_zone0/temp` was used to log temperature, during the benchmark run

5. Reducing Power Consumption

The overall system power consumption depends on both the software optimization and how the system hardware is implemented. Below is a list of suggestions that may help to reduce the system power.

- Apply the clock gating whenever the clocks or modules are not used by configuring the CCGR registers in the Clock Controller Module (CCM).
- Reduce the number of operating PLLs: applicable mainly in the Audio_Playback or Idle modes.

Core DVFS and system bus scaling: applying the DVFS for ARM and scaling the frequencies of the NOC, AXI, AHB, and IPG bus clocks can significantly reduce the power consumption of the VDD_ARM and VDD_SOC domains. However, due to the reduced operation frequency, the accesses to the DDR take longer, which increases the power consumption of the DDR I/O and memories. This trade-off must be taken into account for each mode to quantify the overall effect on the system power.

- Put the i.MX 8M Quad into the low-power modes (STOP) whenever possible. See the "Clock Controller Module (CCM)" chapter in the *i.MX 8M Quad Applications Processor Reference Manual* (document IMX8MDQLQRM) for details.
- DDR interface optimization:
  - Employ careful board routing of the DDR memories, maintaining the PCB trace lengths as short as possible.
  - Use as reduced an ODT (On-Die Termination) setting as possible. The termination used greatly influences the power consumption of the DDR interface pins.
  - Use a proper output driver impedance for the DDR interface pins that provide good impedance matching. Select the lowest possible drive strength that provides the required performance to reduce the current flowing through the DDR I/O pins.
  - The use of the DDR memory offerings in the latest process technology can significantly reduce the power consumption of the DDR devices and the DDR I/O.

The various steps are shown below.

NOTE

All the programming steps below are performed in the ARM trusted Firmware from internal RAM.

5.1. Steps to be performed before entering the Suspend (Deep-Sleep) mode

1. Read the DBGCAM register in DDRC to make sure the explicit transaction command queue is empty. Wait until the AXI port is idle.
2. Do the following:
   - a) Put the DDR into self refresh.
   - b) Transition the DDR PHY into LP3/IO retention state by using the DFI frequency operation.
   - c) Set the PwrOkIn signal in SRC to 0, this will enable the data retention feature on the CKE and MEMRESET.

- d) Gate the DDRC's CORE clock and APB clock.
- e) Enable DDRMIX ISO to power gate the DDRC & PHY.

3. Enter the Suspend mode.

5.2. Steps to be performed after exiting the Suspend mode

1. Restore all the settings for the DDRC&PHY to the required values.
2. The system proceeds to the Run mode.

6. Use Case Configuration and Usage Guidelines

6.1. Deep-Sleep mode

In this use case, all clocks and PLLs are turned off, except for the 32 kHz clock which is used for the system wakeup:

1. Boot up the Linux image.
2. Run this command to put the system into the DSM mode:

```
echo mem > /sys/power/state
```

3. Measure the power and record the result.

6.2. System Idle mode

NOTE

No display was connected to the platform!

6.2.1. IDLE_DDRC_167MHz

6.2.1.1. clock configuration

The clock configuration in Table 34 is aligned with release L4.9.51.

Table 34. IDLE_DDRC_167MHz clock configuration

Clock name	Frequency (MHz)
NOC	800
AXI	25
AHB	20
CPU	1000
DDRC	167

6.2.1.2. PLL configuration

The PLL configuration in Table 35 is aligned with release L4.9.51.

Table 35. IDLE_DDRC_167MHz PLL configuration

Clock root	Source selected	Frequency (MHz)
ARM_A53_CLK	PLL_ARM_MAIN_CLK	1000
NOC_CLK	SYS1_PLL_800M	100
MAIN_AXI_CLK	M OSC	25
DISP_AXI_CLK	SYS1_PLL_800M	off
ENET_AXI_CLK	SYS1_PLL_266M	off
NAND_USDHC_BUS_CLK	SYS1_PLL_266M	off
AHB_CLK_ROOT	SYS1_PLL_133M	20
IPG_CLK	AHB_CLK_ROOT	10
DRAM_CLK	DRAM_ALT_CLK	25
PCIE_CTRL_CLK	SYS2_PLL_250M	off
LCDIF_PIXEL_CLK	25M OSC	off
SAIx_CLK	AUDIO_PLL_OUT	off
ENETx_REF_CLK	SYS2_PLL_125M	off
ENETx_TIME_CLK	SYS2_PLL_100M	off
ENET_PHY_REF_CLK	25M OSC	off
NAND_CLK	SYS1_PLL_400M	off
QSPI_CLK	SYS1_PLL_100M	off
USHDCx_CLK	SYS1_PLL_400M	off
I2Cx_CLK	25M OSC	off
UARTx_CLk	25M OSC	25
ECSPIx_CLK	SYS2_PLL_200M	off
PWMx_CLK	25M OSC	off
GPTx_CLK	25M OSC	25
TRACE_CLK	25M OSC	off
WDOG_CLK	25M OSC	25

6.2.1.3. System setup

Disconnect everything except for the SD.

Make sure there are no displays connected to the platform.

1. Boot up the Linux
2. Run the following script to put the system into system idle mode:

```
#!/bin/bash
echo 8 > /proc/sys/kernel/printk
///echo 1 > /sys/class/graphics/fb0/blank -> this won’t work with Weston, so don’t
connect any display
eth_int=`ifconfig -a|grep 'eth\|can\|sit'|awk {'print $1'}`
for eth in $eth_int;do
        ifconfig $eth down
done
```

3. Measure the power and record the result.

6.2.2. IDLE_HDMI_IN_ETH_ON_DDRC_800MHz

6.2.2.1. clock configuration

The clock configuration in Table 36 is aligned with release L4.9.51.

Table 36. IDLE_HDMI_IN_ETH_ON_DDRC_800MHz clock configuration

Clock name	Frequency (MHz)
NOC	800
AXI	333
AHB	133.33
CPU	1000
DDRC	800

6.2.2.2. PLL configuration

The PLL configuration in Table 37 is aligned with release L4.9.51.

Table 37. IDLE_HDMI_IN_ETH_ON_DDRC_800MHz PLL configuration

Clock root	Source selected	Frequency (MHz)
ARM_A53_CLK	PLL_ARM_MAIN_CLK	1000
NOC_CLK	SYS1_PLL_800M	800
MAIN_AXI_CLK	SYS2_PLL_333M	25
DISP_AXI_CLK	SYS1_PLL_800M	off
ENET_AXI_CLK	SYS1_PLL_266M	off
NAND_USDHC_BUS_CLK	SYS1_PLL_266M	off
AHB_CLK_ROOT	SYS1_PLL_133M	133
IPG_CLK	AHB_CLK_ROOT	66

6.2.2.3. System setup

Disconnect everything except for the SD.

Make sure there are no displays connected to the platform;

1. Boot up the Linux,
2. Measure the power and record the result.

6.3. Audio_Playback

6.3.1. Clock configuration

The clock configuration in the following table is aligned with release L4.9.51.

Table 38. Audio_Playback clock configuration

Clock name	Frequency (MHz)
NOC	100
AXI	25
AHB	20
CPU	1000
DDRC	167

Table 39. Audio + Video_Playback clock configuration

Clock name	Frequency (MHz)
NOC	800
AXI	333
AHB	133
CPU	1000
DDRC	800

6.3.2. PLL configuration

The PLL configuration in the following table is aligned with release L4.9.51

Table 40. Audio_Playback PLL configuration

Clock root	Source selected	Frequency (MHz)
ARM_A53_CLK	PLL_ARM_MAIN_CLK	1000
NOC_CLK	SYS1_PLL_800M	100
MAIN_AXI_CLK	25M_OSC	25
DISP_AXI_CLK	SYS1_PLL_800M	800
ENET_AXI_CLK	SYS1_PLL_266M	266
NAND_USDHC_BUS_CLK	SYS1_PLL_266M	266
AHB_CLK_ROOT	SYS1_PLL_133M	20
IPG_CLK	AHB_ROOT_CLK	10
DRAM_CLK	PLL_DRAM_MAIN_CLK	800
PCIE_CTRL_CLK	SYS2_PLL_250M	off
LCDIF_PIXEL_CLK	25M OSC	--
SAIx_CLK	AUDIO_PLL_OUT	36.8
ENETx_REF_CLK	SYS2_PLL_125M	125
ENETx_TIME_CLK	SYS2_PLL_100M	100
ENET_PHY_REF_CLK	25M OSC	25
NAND_CLK	SYS1_PLL_400M	off
QSPI_CLK	SYS1_PLL_100M	off
USHDCx_CLK	SYS1_PLL_400M	392
I2Cx_CLK	25M OSC	25
UARTx_CLk	25M OSC	25
ECSPIx_CLK	SYS2_PLL_200M	Off
PWMx_CLK	25M OSC	25
GPTx_CLK	25M OSC	25
TRACE_CLK	25M OSC	off
WDOG_CLK	25M OSC	off

Table 41. Audio + Video_Playback PLL configuration

Clock root	Source selected	Frequency (MHz)
ARM_A53_CLK	PLL_ARM_MAIN_CLK	1000
NOC_CLK	SYS1_PLL_800M	800
MAIN_AXI_CLK	SYS2_PLL_333M	333
DISP_AXI_CLK	SYS1_PLL_800M	800
ENET_AXI_CLK	SYS1_PLL_266M	266
NAND_USDHC_BUS_CLK	SYS1_PLL_266M	266
AHB_CLK_ROOT	SYS1_PLL_133M	133
IPG_CLK	AHB_ROOT_CLK	66
DRAM_CLK	PLL_DRAM_MAIN_CLK	800
PCIE_CTRL_CLK	SYS2_PLL_250M	off
LCDIF_PIXEL_CLK	25M OSC	--
SAIx_CLK	AUDIO_PLL_OUT	36.8
ENETx_REF_CLK	SYS2_PLL_125M	125
ENETx_TIME_CLK	SYS2_PLL_100M	100
ENET_PHY_REF_CLK	25M OSC	25
NAND_CLK	SYS1_PLL_400M	off
QSPI_CLK	SYS1_PLL_100M	off
USHDCx_CLK	SYS1_PLL_400M	392
I2Cx_CLK	25M OSC	25
UARTx_CLk	25M OSC	25
ECSPIx_CLK	SYS2_PLL_200M	Off
PWMx_CLK	25M OSC	25
GPTx_CLK	25M OSC	25
TRACE_CLK	25M OSC	off
WDOG_CLK	25M OSC	off

6.3.3. Audio_Playback(gplay)_DDRC_167MHz

For this use case, dtb configuration file was used.

The audio file used was an mp3 file with 128 kbit/s bit rate at 44 kHz sample rate/s, and played using the following options:

1. Boot up the Linux,
2. Run the following script to put the system into system idle mode:

```
#!/bin/bash
echo 8 > /proc/sys/kernel/printk
ifconfig eth0 down
systemctl stop weston
echo 1 > /sys/class/graphics/fb0/blank
gplay-1.0 $audio_file --video-sink=fakesink
```

3. Measure the power and record the result.

6.3.4. Audio_Playback(gplay)_DDRC_167MHz with MIPI-DSI

For this use case, a MIPI-DSI to HDMI card adapter was connected to the EVK DSI port and no display was attached to it.

1. Default .dtb file must be changed in U-boot as following:

```
setenv fdt_file "fsl-imx8mq-evk-lcdif-adv7535.dtb"
saveenv
```

2. Boot up the Linux,
3. Run the following script to put the system into system idle mode:

```
#!/bin/bash
echo 8 > /proc/sys/kernel/printk
ifconfig eth0 down
echo 1 > /sys/class/graphics/fb0/blank
gplay-1.0 $audio_file --video-sink=fakesink
```

4. Measure the power and record the result.

6.3.5. Audio+Video_Playback with HDMI

For this use case, default dtb configuration file was used and HDMI port was connected to a 4K TV display.

Video file used for playback is mkv file format compressed with HEVC standard with full HD resolution at 60 fps and the audio encoding is AACL with 48 kHz samples/s with 6ch configuration.

Video file was locally played with *gst-launch-1.0* play, with the following options:

1. Boot up the Linux,
2. Run the following script to put the system into system idle mode:

```
/usr/bin/gst-launch-1.0 playbin uri=file://$PATH/$FILE video-sink="kmssink
sync=false"
```

3. Measure the power and record the result.

6.3.6. Audio+Video_Stream with HDMI

For this use case, default dtb configuration file was used and HDMI port was connected to a 4K TV display.

Video file used for playback is mkv file format compressed with HEVC standard with full HD resolution at 60 fps and the audio encoding is AACL in 6 channels configuration with 48kHz samples/s.

A server was setup for hosting the mkv video file for streaming;

Video streaming was done using Ethernet adapter and the player used is gst-launch-1.0 with the following options:

1. Boot up the Linux,
2. Run the following script to put the system into system idle mode:

```
/usr/bin/gst-launch-1.0 playbin uri=//$PATH/$FILE video-sink="kmssink
sync=false" ($PATH=http://…)
```

3. Measure the power and record the result.

6.4. Dhrystone on 4 Cortex-A53 (1.5 GHz)

NOTE

No display was connected to the platform!

6.4.1. Clock configuration

The clock configuration in Table 42 is aligned with release L4.9.51.

Table 42. Dhrystone on 4 Cortex-A53 clock configuration

Clock name	Frequency (MHz)
NOC	800
AXI	333
AHB	133
CPU	1500
DDRC	800

6.4.2. PLL configuration

The PLL configuration in Table 43 is aligned with release L4.9.51.

Table 43. Dhrystone on 4 Cortex-A53 PLL configuration

Clock root	Source selected	Frequency (MHz)
ARM_A53_CLK	PLL_ARM_MAIN_CLK	1500
NOC_CLK	SYS1_PLL_800M	800
MAIN_AXI_CLK	SYS2_PLL_333M	333
DISP_AXI_CLK	SYS1_PLL_800M	800
ENET_AXI_CLK	SYS1_PLL_266M	266
NAND_USDHC_BUS_CLK	SYS1_PLL_266M	266
AHB_CLK_ROOT	SYS1_PLL_133M	133
IPG_CLK	AHB_ROOT_CLK	66
DRAM_CLK	PLL_DRAM_MAIN_CLK	800
PCIE_CTRL_CLK	SYS2_PLL_250M	off
LCDIF_PIXEL_CLK	25M OSC	—
SAIx_CLK	AUDIO_PLL_OUT	36.8
ENETx_REF_CLK	SYS2_PLL_125M	125
ENETx_TIME_CLK	SYS2_PLL_100M	100
ENET_PHY_REF_CLK	25M OSC	25
NAND_CLK	SYS1_PLL_400M	off
QSPI_CLK	SYS1_PLL_100M	off
USHDCx_CLK	SYS1_PLL_400M	392
I2Cx_CLK	25M OSC	25
UARTx_CLk	25M OSC	25
ECSPIx_CLK	SYS2_PLL_200M	Off
PWMx_CLK	25M OSC	25
GPTx_CLK	25M OSC	25
TRACE_CLK	25M OSC	off
WDOG_CLK	25M OSC	off

6.4.3. Steps

1. Boot up the Linux image and boot the board to the SD rootfs.
2. Run the following script to measure at 1.5 GHz.

```
#!/bin/sh
ifconfig eth0 down
systemctl stop weston
echo  1 > /sys/class/graphics/fb0/blank;
cpufreq-set -g performance
```

3. Run dry2 and measure (dry2 is not included in default GA release Demo image):

```
while  true;  do dry2; done
```

4. Measure the power and record the result.

6.5. Whetstone on 4 Cortex-A53 (1.5 GHz)

NOTE

No display was connected to the platform!

6.5.1. Clock configuration

The clock configuration in Table 44 is aligned with release L4.9.51.

Table 44. Whetstone on 4 Cortex-A53 clock configuration

Clock name	Frequency (MHz)
NOC	800
AXI	333
AHB	133
CPU	1500
DDRC	800

6.5.2. PLL configuration

The PLL configuration in Table 45 is aligned with release L4.9.51.

Table 45. Whetstone on 4 Cortex-A53 PLL configuration

Clock root	Source selected	Frequency (MHz)
ARM_A53_CLK	PLL_ARM_MAIN_CLK	1500
NOC_CLK	SYS1_PLL_800M	800
MAIN_AXI_CLK	SYS2_PLL_333M	333
DISP_AXI_CLK	SYS1_PLL_800M	800
ENET_AXI_CLK	SYS1_PLL_266M	266
NAND_USDHC_BUS_CLK	SYS1_PLL_266M	266
AHB_CLK_ROOT	SYS1_PLL_133M	133
IPG_CLK	AHB_ROOT_CLK	66
DRAM_CLK	PLL_DRAM_MAIN_CLK	800
PCIE_CTRL_CLK	SYS2_PLL_250M	off
LCDIF_PIXEL_CLK	25M OSC	—
SAIx_CLK	AUDIO_PLL_OUT	36.8
ENETx_REF_CLK	SYS2_PLL_125M	125
ENETx_TIME_CLK	SYS2_PLL_100M	100
ENET_PHY_REF_CLK	25M OSC	25
NAND_CLK	SYS1_PLL_400M	off
QSPI_CLK	SYS1_PLL_100M	off
USHDCx_CLK	SYS1_PLL_400M	392
I2Cx_CLK	25M OSC	25
UARTx_CLK	25M OSC	25
ECSPIx_CLK	SYS2_PLL_200M	Off
PWMx_CLK	25M OSC	25
GPTx_CLK	25M OSC	25
TRACE_CLK	25M OSC	off
WDOG_CLK	25M OSC	off

6.5.3. Steps

1. Boot up the Linux image and boot the board to the SD rootfs.
2. Run the following script to measure at 1.5 GHz.

```
#!/bin/sh
ifconfig eth0 down
systemctl stop Weston
echo  1 > /sys/class/graphics/fb0/blank;
cpufreq-set -g performance
```

3. Run dry2 and measure (dry2 is not included in default GA release Demo image):

```
while  true;  do dry2; done
```

4. Measure the power and record the result.

6.6. C-Ray

NOTE

No display was connected to the platform!

6.6.1. Clock configuration

The clock configuration in Table 46 is aligned with release L4.9.51.

Table 46. C-Ray clock configuration

Clock name	Frequency (MHz)
NOC	800
AXI	333
AHB	133
CPU	1500
DDRC	800

6.6.2. PLL configuration

The PLL configuration in Table 47 is aligned with release L4.9.51.

Table 47. C-Ray PLL configuration

Clock root	Source selected	Frequency (MHz)
ARM_A53_CLK	PLL_ARM_MAIN_CLK	1500
NOC_CLK	SYS1_PLL_800M	800
MAIN_AXI_CLK	SYS2_PLL_333M	333
DISP_AXI_CLK	SYS1_PLL_800M	800
ENET_AXI_CLK	SYS1_PLL_266M	266
NAND_USDHC_BUS_CLK	SYS1_PLL_266M	266
AHB_CLK_ROOT	SYS1_PLL_133M	133
IPG_CLK	AHB_ROOT_CLK	66
DRAM_CLK	PLL_DRAM_MAIN_CLK	800
PCIE_CTRL_CLK	SYS2_PLL_250M	off
LCDIF_PIXEL_CLK	25M OSC	—
SAIx_CLK	AUDIO_PLL_OUT	36.8
ENETx_REF_CLK	SYS2_PLL_125M	125
ENETx_TIME_CLK	SYS2_PLL_100M	100
ENET_PHY_REF_CLK	25M OSC	25
NAND_CLK	SYS1_PLL_400M	off
QSPI_CLK	SYS1_PLL_100M	off
USHDCx_CLK	SYS1_PLL_400M	392
I2Cx_CLK	25M OSC	25
UARTx_CLk	25M OSC	25
ECSPIx_CLK	SYS2_PLL_200M	Off
PWMx_CLK	25M OSC	25
GPTx_CLK	25M OSC	25
TRACE_CLK	25M OSC	off
WDOG_CLK	25M OSC	off

6.6.3. Steps

1. Boot up the Linux image and boot the board to the SD rootfs.
2. Run the following script to measure at 1.5 GHz.

```
#!/bin/sh
ifconfig eth0 down
systemctl stop weston
```

```
echo  1 > /sys/class/graphics/fb0/blank;
       cpufreq-set -g performance
```

3. Run c-ray and measure:

```
while  true;  do cat scene | ./c-ray-mt -t 4 > foo.ppm; done
```

4. Measure the power and record the result.

6.7. Coremark

NOTE

No display was connected to the platform!

6.7.1. Clock configuration

The clock configuration in Table 48 is aligned with release L4.9.51.

Table 48. Coremark clock configuration

Clock name	Frequency (MHz)
NOC	800
AXI	333
AHB	133
CPU	1500
DDRC	800

6.7.2. PLL configuration

The PLL configuration in Table 49 is aligned with release L4.9.51.

Table 49. Coremark PLL configuration

Clock root	Source selected	Frequency (MHz)
ARM_A53_CLK	PLL_ARM_MAIN_CLK	1500
NOC_CLK	SYS1_PLL_800M	800
MAIN_AXI_CLK	SYS2_PLL_333M	333
DISP_AXI_CLK	SYS1_PLL_800M	800
ENET_AXI_CLK	SYS1_PLL_266M	266
NAND_USDHC_BUS_CLK	SYS1_PLL_266M	266
AHB_CLK_ROOT	SYS1_PLL_133M	133
IPG_CLK	AHB_ROOT_CLK	66
DRAM_CLK	PLL_DRAM_MAIN_CLK	800
PCIE_CTRL_CLK	SYS2_PLL_250M	off
LCDIF_PIXEL_CLK	25M OSC	—
SAIx_CLK	AUDIO_PLL_OUT	36.8
ENETx_REF_CLK	SYS2_PLL_125M	125
ENETx_TIME_CLK	SYS2_PLL_100M	100
ENET_PHY_REF_CLK	25M OSC	25
NAND_CLK	SYS1_PLL_400M	off
QSPI_CLK	SYS1_PLL_100M	off
USHDCx_CLK	SYS1_PLL_400M	392
I2Cx_CLK	25M OSC	25
UARTx_CLK	25M OSC	25
ECSPIx_CLK	SYS2_PLL_200M	Off
PWMx_CLK	25M OSC	25
GPTx_CLK	25M OSC	25
TRACE_CLK	25M OSC	off
WDOG_CLK	25M OSC	off

6.7.3. Steps

1. Boot up the Linux image and boot the board to the SD rootfs.
2. Run the following script to measure at 1.5 GHz.

```
#!/bin/sh
ifconfig eth0 down
systemctl stop weston
echo  1 > /sys/class/graphics/fb0/blank;
       cpufreq-set -g performance
```

3. Run coremark and measure:

```
while  true;  do coremark,exe; done
```

4. Measure the power and record the result.

6.8. GPU

Three benchmarks were used for GPU power measurements. A 4k TV display was connected to HDMI port.

Platform was booted from SD card with default **dtb** configuration.

Before running any benchmark, governor must be set to **performance**:

```
cpufreq-set -g performance
```

After setting the governor, you run in a loop the respective gpu benchmark and you start power measurements and temperature logging at your desired time interval.

6.8.1. MM07

1. Run in a loop *./fm_oes_vg_player* :

```
while [ "1" == "1" ]
do
./fm_oes2_mobile_player
done
```

2. Start die temperature recording
3. Start power measurement and record the result

6.8.1.1. Clock configuration

The clock configuration in Table 50 is aligned with release L4.9.51.

Table 50. MM07 clock configuration

Clock name	Frequency (MHz)
NOC	800
AXI	333
AHB	133
CPU	1500
DDRC	800

6.8.1.2. PLL configuration

The PLL configuration in Table 51 is aligned with release L4.9.51.

Table 51. MM07 PLL configuration

Clock root	Source selected	Frequency (MHz)
ARM_A53_CLK	PLL_ARM_MAIN_CLK	1500
NOC_CLK	SYS1_PLL_800M	800
MAIN_AXI_CLK	SYS2_PLL_333M	333
DISP_AXI_CLK	SYS1_PLL_800M	800
ENET_AXI_CLK	SYS1_PLL_266M	266
NAND_USDHC_BUS_CLK	SYS1_PLL_266M	266
AHB_CLK_ROOT	SYS1_PLL_133M	133
IPG_CLK	AHB_ROOT_CLK	66
DRAM_CLK	PLL_DRAM_MAIN_CLK	800
PCIE_CTRL_CLK	SYS2_PLL_250M	off
LCDIF_PIXEL_CLK	25M OSC	--
SAIx_CLK	AUDIO_PLL_OUT	36.8
ENETx_REF_CLK	SYS2_PLL_125M	125
ENETx_TIME_CLK	SYS2_PLL_100M	100
ENET_PHY_REF_CLK	25M OSC	25
NAND_CLK	SYS1_PLL_400M	off
QSPI_CLK	SYS1_PLL_100M	off
USHDCx_CLK	SYS1_PLL_400M	392
I2Cx_CLK	25M OSC	25
UARTx_CLK	25M OSC	25
ECSPIx_CLK	SYS2_PLL_200M	Off
PWMx_CLK	25M OSC	25
GPTx_CLK	25M OSC	25
TRACE_CLK	25M OSC	off
WDOG_CLK	25M OSC	off

6.9. Heavy loading use cases

Four use cases were used for power measurements. A 4k TV display was connected to HDMI port. Platform was booted from SD card with default **dtb** configuration. Before running any benchmark, governor must be set to **performance**:

```
cpufreq-set -g performance
```

After setting the governor, you run in a loop the respective use case and you start power measurements and temperature logging at your desired time interval (recommended is 1 minute) using section 6.14

6.9.1. VPU

A 4k TV display was connected to HDMI port. Platform was booted from SD card with default **dtb** configuration. Before running any benchmark, governor must be set to **performance**:

```
cpufreq-set -g performance
```

After setting the governor, you run in a loop the respective use case and you start power measurements and temperature logging at your desired time interval (recommended is 1 minute) using section 6.14

6.9.2. 4-core Dhryst + VPU + Taiji

A 4k TV display was connected to HDMI port. Platform was booted from SD card with default **dtb** configuration. Before running any benchmark, governor must be set to **performance**:

```
cpufreq-set -g performance
```

After setting the governor, you run in a loop the respective use case and you start power measurements and temperature logging at your desired time interval (recommended is 1 minute) using section 6.14

6.9.3. 4-core Memtest + VPU + Taiji

A 4k TV display was connected to HDMI port. Platform was booted from SD card with default **dtb** configuration. Before running any benchmark, governor must be set to **performance**:

```
cpufreq-set -g performance
```

After setting the governor, you run in a loop the respective use case and you start power measurements and temperature logging at your desired time interval (recommended is 1 minute) using section 6.14

6.9.4. 4-core Streamcpy + VPU + Taiji

1. start 4 streamcpy, each bind on separate cpu

```
while [ "1" == "1" ]
do
sudo taskset -c 0 stream -M 200M -N 1000 &
sudo taskset -c 1 stream -M 200M -N 1000 &
sudo taskset -c 2 stream -M 200M -N 1000 &
sudo taskset -c 3 stream -M 200M -N 1000
done
```

2. start Taiji use case in a loop (section 6.8.1)
3. start VPU use case (section 6.9.1)
4. Start die temperature recording (section 6.14)
5. Start power measurement and record data

6.10. Memory

NOTE

No display was connected to the platform!

Two use cases were used for power measurements. Platform was booted from SD card with default **dtb** configuration. Before running any benchmark, governor must be set to **performance** and display turned off:

```
cpufreq-set -g performance
echo 1 > /sys/class/graphics/fb0/blank
```

After setting the governor, you run in a loop the respective use case and you start power measurements and temperature logging at your desired time interval using section 6.14 (recommended is 1 minute).

6.10.1. Memset

```
perf bench -f simple mem memset -s 1000MB
```

6.10.2. Memcpy

```
perf bench -f simple mem memcpy -s 1000MB
```

6.10.3. Stream

Make sure stream libraries are added to *LD_LIBRARY_PATH*

1. start *stream (*you can create a loop for running it)
2. Start die temperature recording (section 6.14)
3. Start power measurement and record data

6.11. Storage – SDHC class10

Make sure stream libraries are added to *LD_LIBRARY_PATH*

1. start *stream (*you can create a loop for running it)
2. Start die temperature recording (section 6.14)
3. Start power measurement and record data

6.11.1. DD_RD_SDCARD

1. Run dd_read script on SD card (see below)
2. Start die temperature recording (section 6.14)
3. Start power measurement and record data

```
#!/bin/bash

# Since we're dealing with dd, abort if any errors occur
set -e

TEST_FILE=${1:-dd_ibs_testfile}
#if [ -e "$TEST_FILE" ]; then TEST_FILE_EXISTS=$?; fi
#TEST_FILE_SIZE=3221225472
#134217728

# Exit if file exists
#if [ -e $TEST_FILE ]; then
#  echo "Test file $TEST_FILE exists, aborting."
#  exit 1
#fi
```

```
#TEST_FILE_EXISTS=1

if [ $EUID -ne 0 ]; then
  echo "NOTE: Kernel cache will not be cleared between tests without sudo. This
will likely cause inaccurate results." 1>&2
fi

# Create test file
#echo 'Generating test file...'
#BLOCK_SIZE=65536
#COUNT=$(($TEST_FILE_SIZE / $BLOCK_SIZE))
#dd if=/dev/urandom of=$TEST_FILE bs=$BLOCK_SIZE count=$COUNT conv=fsync >
/dev/null 2>&1

# Header
PRINTF_FORMAT="%8s : %s\n"
printf "$PRINTF_FORMAT" 'block size' 'transfer rate'

# Block sizes of 512b 1K 2K 4K 8K 16K 32K 64K 128K 256K 512K 1M 2M 4M 8M 16M 32M
64M
for BLOCK_SIZE in 512 1024 2048 4096 8192 16384 32768 65536 131072 262144 524288
1048576 2097152 4194304 8388608 16777216 33554432 67108864
do
  # Clear kernel cache to ensure more accurate test
  [ $EUID -eq 0 ] && [ -e /proc/sys/vm/drop_caches ] && echo 3 >
/proc/sys/vm/drop_caches

  # Read test file out to /dev/null with specified block size
  DD_RESULT=$(dd if=$TEST_FILE of=/dev/null bs=$BLOCK_SIZE 2>&1 1>/dev/null)

  # Extract transfer rate
  TRANSFER_RATE=$(echo $DD_RESULT | \grep --only-matching -E '[0-9.]+
([MGk]?B|bytes)/s(ec)?')

  printf "$PRINTF_FORMAT" "$BLOCK_SIZE" "$TRANSFER_RATE"
done
```

6.11.2. DD_WRT_SDCARD

1. Run dd_write script on SD card (see below)
2. Start die temperature recording (section 6.14)
3. Start power measurement and record data

```
#!/bin/bash

# Since we're dealing with dd, abort if any errors occur
set -e

TEST_FILE=${1:-dd_obs_testfile}
TEST_FILE_EXISTS=0
if [ -e "$TEST_FILE" ]; then TEST_FILE_EXISTS=1; fi
TEST_FILE_SIZE=3221225472
#134217728
```

```
if [ $EUID -ne 0 ]; then
  echo "NOTE: Kernel cache will not be cleared between tests without sudo. This
will likely cause inaccurate results." 1>&2
fi

# Header
PRINTF_FORMAT="%8s : %s\n"
printf "$PRINTF_FORMAT" 'block size' 'transfer rate'

# Block sizes of 512b 1K 2K 4K 8K 16K 32K 64K 128K 256K 512K 1M 2M 4M 8M 16M 32M
64M
for BLOCK_SIZE in 512 1024 2048 4096 8192 16384 32768 65536 131072 262144 524288
1048576 2097152 4194304 8388608 16777216 33554432 67108864
do
  # Calculate number of segments required to copy
  COUNT=$(($TEST_FILE_SIZE / $BLOCK_SIZE))

  if [ $COUNT -le 0 ]; then
    echo "Block size of $BLOCK_SIZE estimated to require $COUNT blocks, aborting
further tests."
    break
  fi

  # Clear kernel cache to ensure more accurate test
  [ $EUID -eq 0 ] && [ -e /proc/sys/vm/drop_caches ] && echo 3 >
/proc/sys/vm/drop_caches

  # Create a test file with the specified block size
  DD_RESULT=$(dd if=/dev/zero of=$TEST_FILE bs=$BLOCK_SIZE count=$COUNT conv=fsync
2>&1 1>/dev/null)

  # Extract the transfer rate from dd's STDERR output
  TRANSFER_RATE=$(echo $DD_RESULT | \grep --only-matching -E '[0-9.]+
([MGk]?B|bytes)/s(ec)?')

  ## Clean up the test file if we created one
  #if [ $TEST_FILE_EXISTS -ne 0 ]; then rm $TEST_FILE; fi

  # Output the result
  printf "$PRINTF_FORMAT" "$BLOCK_SIZE" "$TRANSFER_RATE"
done
```

6.11.3. IO_WRT_SDCARD

1. Run iozone on SD card (you may create a loop for continuous power measurement)
   `./iozone -i 0 -b /tmp/iozone.xls -r 128k -s 3G -l 1 -u 1`
2. Start die temperature recording (section 6.14)
3. Start power measurement and record data

6.12. Storage – eMMC

A partition was created on eMMC and benchmarks were run on it.

6.12.1. DD_RD_eMMC

1. Run dd_read script on eMMC partition card
2. Start die temperature recording
3. Start power measurement and record data

6.12.2. DD_WRT_eMMC

1. Run dd_write script on eMMC partition card
2. Start die temperature recording
3. Start power measurement and record data

6.12.3. IO_WRT_eMMC

1. Run iozone on SD card (you may create a loop for continuous power measurement)
   ```
   ./iozone -i 0 -b /tmp/iozone.xls -r 128k -s 3G -l 1 -u 1
   ```
2. Start die temperature recording
3. Start power measurement and record data

6.13. Storage – USB3.0

A USB 3.0 was used for running the benchmarks.

6.13.1. DD_RD_USB3.0

1. Run dd_read script on USB 3.0 partition card
2. Start die temperature recording
3. Start power measurement and record data

6.13.2. DD_WRT_USB3.0

1. Run dd_write script on USB 3.0 partition card
2. Start die temperature recording
3. Start power measurement and record data

6.13.3. IO_WRT_USB3.0

1. Run iozone on USB 3.0 card (you may create a loop for continuous power measurement)
   ```
   ./iozone -i 0 -b /tmp/iozone.xls -r 128k -s 3G -l 1 -u 1
   ```
2. Start die temperature recording
3. Start power measurement and record data

6.14. Important commands

In the U-boot console:

- `printenv`: displays the environment variables.
- `setenv`: updates the environment variables.
  - setenv <name> <value> ...
  - Sets the environment variable “name” to “value ...”.
  - setenv <name>
  - Deletes the environment variable “name”.
- `saveenv`: saves the updates to the environment variables.
- `bootargs`: passes to the kernel, which are called kernel command lines.

In the Linux OS console:

- `cat /proc/cmdline:` displays the command line.
- `cat /sys/devices/virtual/thermal/thermal_zone0/temp:` prints the temperature to the screen(the chip should be calibrated).
  `cat /sys/kernel/debug/clk/clk_summary:` prints all clks to the screen.

7. Revision history

Table 52 summarizes the changes done to this document since the initial release.

Table 52. Revision history

Revision number	Date	Substantive changes
0	02/2018	Initial release
1	05/2018	Updated the power numbers based on test result using GA software release
2	08/2018	Fixed bugs

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