# MPC8560/E PowerQUICC™ III Processor

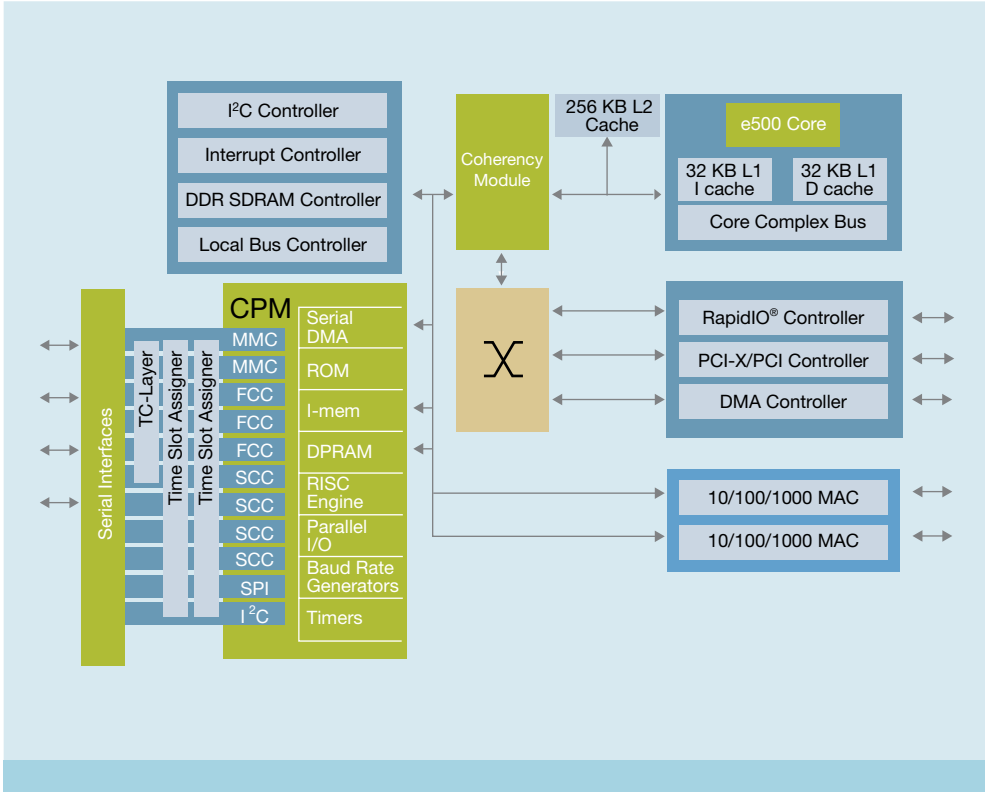
## Overview

The PowerQUICC™ III is a versatile integrated communications processor designed for a variety of compute-intensive applications, excelling particularly in communications and networking products. Freescale's PowerQUICC III processor family is the next generation of Freescale's industry-leading PowerQUICC line of integrated communications processors. PowerQUICC III processors provide higher performance in all areas of device operation, including greater flexibility, extended capabilities and higher integration.

## Product Highlights

Freescale's leading PowerQUICC III architecture integrates two processing blocks. One block is a high-performance embedded e500 core. With 256 KB of Level 2 cache, the e500 core built on Power Architecture™ technology provides unprecedented levels of hardware and software debugging support. The second block is the Communications Processor Module (CPM). The CPM of the PowerQUICC III can support three fast serial communications controllers (FCCs), two multi-channel controllers (MCCs), four serial communications controllers (SCCs), one serial peripheral interface (SPI) and one $I^2C$ interface. The PowerQUICC III also offers two integrated 10/100/1000 Ethernet controllers, a DDR SDRAM memory controller, a 64-bit PCI-X/PCI controller and a RapidIO® interconnect. This high level of integration helps simplify board design and offers significant bandwidth and performance for high-end control plane and data plane applications.

MPC8560 Block Diagram




## RapidIO Interconnect Technology

As a founding member of the RapidIO Trade Association, Freescale has been driving the industry's adoption of this high-performance switch fabric control plane interconnect. RapidIO technology offers significantly greater bandwidth, scalability and reliability than other interconnects in use today, yet is compatible with existing PCI and CPU architectures. It has a flexible architecture that can easily adapt to changing industry needs without affecting existing infrastructure. RapidIO technology is an open standard governed by an industry body, designed specifically for embedded, networking and communications applications.

| PowerQUICC™ III Processor Family | MPC8541E | MPC8540 | MPC8555E | MPC8560 |
|---|---|---|---|---|
| **Core** | e500 | e500 | e500 | e500 |
| **Frequency** | 533 MHz–1 GHz | 667 MHz–1 GHz | 533 MHz–1 GHz | 667 MHz–1 GHz |
| **I-Cache/D-Cache (KB)** | 32/32 | 32/32 | 32/32 | 32/32 |
| **Integrated L2 Cache (KB)** | 256 | 256 | 256 | 256 |
| **Integrated Security Engine** | Yes | - | Yes | - |
| **Fast Communications Controllers** | - | - | 2 | 3 |
| **Serial Communications Controllers** | - | - | 3 | 4 |
| **Ethernet (10/100 only)** | 2 | 1 | Up to 2 | Up to 3 |
| **Ethernet (10/100/1000)** | 2 | 2 | 2 | 2 |
| **I²C Controller** | 2 | 1 | 2 | 2 |
| **UTOPIA Level II Ports** | - | - | 2 | 2 |
| **Multi-Channel HDLC** | - | - | Up to 64 (QMC) | Up to 256 |
| **PCI Interface** | 2x 32-bit or 1x 64-bit | 1x 32/64-bit | 2x 32-bit or 1x 64-bit | 1x 32/64-bit |
| **PCI-X Interface** | - | Yes | - | Yes |
| **RapidIO® Interface** | - | Yes | - | Yes |

## Typical Applications

- Remote access concentrators/servers
- Regional office routers
- Wireless infrastructure equipment
- Telecommunications switching and transmission equipment
- Ethernet switches
- T1/E1 and T3/E3 line cards
- OC-3 line card
- LAN-to-WAN router
- DSLAMs
- Multi-service access platforms
- Optical networking
- IP networking
- SONET transmission controller
- Media gateways
- IP Virtual Private Networks (VPN)

## Technical Specifications

- High-performance embedded e500 core available from 667 MHz to 1 GHz
  - 32-bit, dual-issue, superscalar, seven-stage pipeline
  - 2310 MIPS at 1 GHz (estimated Dhrystone 2.1)
  - 32 KB L1 data and 32 KB L1 instruction cache with line locking support
  - 256 KB on-chip L2 cache with direct mapped capability
  - Enhanced hardware and software debug support
  - Memory management unit (MMU)
  - SIMD extension with single precision floating point
- Two TSECs supporting 10/100/1000 Mbps Ethernet with two GMII/TBI/RGMII interfaces
- High-performance CPM
  - 32-bit RISC architecture running up to 333 MHz
  - One instruction per clock
  - Software compatible with other CPM-based offerings
  - 32 KB dual-port RAM
  - Three full-duplex FCCs supporting:
    - ATM at up to 155 Mbps
      - Support for two UTOPIA interfaces
      - AAL0, AAL1, AAL2, AAL3/4, AAL5
    - 10/100 Mbps Ethernet
      - Support for up to three MII/RMII interfaces
    - HDLC/transparent up to 45 Mbps
  - ATM transmission convergence layer capabilities (eight channels)
  - Integrated inverse multiplexing for ATM (IMA) functionality
  - Two MCCs
    - Up to 256 HDLC/transparent channels at 64 Kbps each
    - Eight TDM interfaces
  - Four full-duplex SCCs that support the following protocols:
    - High level/synchronous data link control (HDLC/SDLC)
    - LocalTalk (HDLC-based local area network protocol)
    - Universal asynchronous receiver transmitter (UART)
    - Synchronous UART (1x clock mode)
    - Binary synchronous communication
    - Totally transparent operation
  - Serial peripheral interface support for master or slave
  - I²C bus controller
  - Time-slot assigner (TSA) supports multiplexing of data from any of the SCCs and FCCs onto eight time-division multiplexed (TDM) interfaces
- DDR SDRAM memory controller
  - 166 MHz, 64-bit, 2.5V I/O
  - Full ECC support
- RapidIO controller—500 MHz, 8-bit, LVDS I/O
  - PCI, PCI-X controller
  - PCI 2.2 and PCI-X 1.0 compatible
  - 64- or 32-bit PCI from 16 to 66 MHz
- 64-bit PCI-X support up to 133 MHz
- Host and agent mode support
- Integrated 4-channel DMA controller
- Local bus with memory controller—166 MHz, 32-bit, 3.3V I/O
- Interrupt controller
- IEEE® 1149.1 JTAG test access port
- 1.2V core power supply (1.3V for 1 GHz operation) with 3.3V and 2.5V I/O
- 783-pin FC-BGA package

**Learn More:** For current information about Freescale products and documentation, please visit **www.freescale.com**.



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