Fact Sheet

MPC8240

INTEGRATED HOST PROCESSOR

The MPC8240 Integrated Host Processor implementing the PowerPC architecture fits applications where cost, space, power consumption, and performance are critical requirements. This device provides a high level of integration, reducing chip count from five discrete chips to one, thereby significantly reducing system component cost. High integration results in a simplified board design, less power consumption, and a faster time-to-market solution. This cost-effective, general-purpose integrated processor targets systems using PCI interfaces in networking infrastructure, telecommunications, and other embedded markets. It can be used for control processing in applications such as routers, switches, network storage applications, and image display systems.

PROCESSOR CORE

The MPC8240 Integrated Host Processor takes advantage of a small, yet powerful, 32-bit, superscalar G2 processor core implementing the PowerPC architecture. The processor core provides floating-point support, memory management, 16 KB instruction and data caches, and power management features with five independent execution units. This full-featured high-performance processor core is software-compatible with the Freescale microprocessor families implementing the PowerPC architecture.

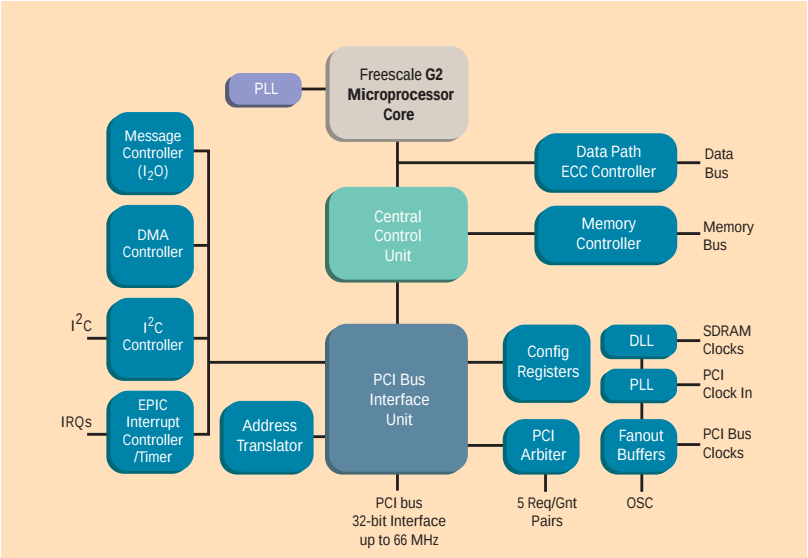
PRODUCT HIGHLIGHTS

- Up to 250 MHz processor core
- 32-bit PCI interface operating at up to 66 MHz
- Memory controller offering SDRAM support up to 100 MHz operation
- General purpose I/O and ROM interface support
- Two-channel DMA controller that supports chaining
- Messaging unit with I_2O messaging support capability
- Industry-standard I^2C interface
- Programmable interrupt controller with multiple timers and counters

TYPICAL APPLICATIONS

- Routers/switches
- Multichannel modems
- Network storage
- Image display systems
- Enterprise I/O processor
- Internet access device (IAD)
- Disk controller for RAID systems
- Copier/printer board control

FREESCALE ***MPC8240 BLOCK DIAGRAM***



FEATURES

Processor Core

- High-performance, superscalar processor core
- Floating-point unit, integer, load/store, system register, and branch processing unit
- 16 KB instruction cache, 16 KB data cache
- Lockable portion of L1 cache
- Dynamic power management

ON-CHIP PERIPHERAL LOGIC

- Memory interface
  - 100 MHz memory bus capability
  - Programmable timing supporting either FPM DRAM, EDO DRAM, or SDRAM
  - High-bandwidth bus (32/64-bit data bus) to DRAM
  - Supports one to eight banks of 4-, 16-, 64-, or 128-bit DRAM
  - Supports 1 MB to 1 GB DRAM memory
  - Contiguous memory mapping
  - 16 MB of ROM space
  - 8-bit, 32-bit, or 64-bit ROM
  - Supports bus-width writes to Flash
  - Read-modify-write parity support (selectable)
  - ECC support (selectable)
  - SDRAM, DRAM buffer data path
  - Error injection/capture on data path
  - LVTTL compatible
  - PortX: 8-, 32- or 64-bit general-purpose I/O port uses ROM controller interface with address strobe
- 32-bit PCI interface operating up to 66 MHz
  - PCI 2.1 compatible
  - PCI 5.0V tolerant
  - Support for PCI locked accesses to memory
  - Support for accesses to all PCI address spaces
  - Selectable big- or little-endian operation
  - Store gathering of processor-to-PCI writes and PCI-to-memory writes
  - Memory prefetching of PCI read accesses
  - Parity support (selectable)
  - Selectable hardware-enforced coherency
  - PCI bus arbitration unit (5 request/grant pairs)
- PCI agent mode capability
  - Address Translation Unit (ATU)
  - Run-time register access
  - PCI configuration register access
- Two-channel integrated DMA controller
  - Supports direct or chaining modes
  - Scatter gather
  - Interrupt on completed segment, chain, and error
  - Local to local memory
  - PCI to PCI memory
  - PCI to local memory
  - Local to PCI memory

MPC8240 Integrated Host Processor	
CPU Speeds - Internal	200, 250 MHz
CPU Bus Dividers	x2, x2.5, x3, x3.5, x4, x4.5, x5, x5.5, x6
Memory Bus Dividers	1.0, 1.5, 2.0, 2.5, 3.0
PCI Interface	32-bit (up to 66 MHz)
Memory Interface	64-bit (up to 100 MHz) + 8-bit parity
Instructions per Clock	3 (2 + branch)
L1 Cache	16 KB instruction 16 KB data
Typical Power Dissipation (est.)	3.0W @ 200 MHz (with FPU on and @ 2.5V)
Package	352 TBGA
Process	0.29µ 5LM CMOS
Voltage	3.3V I/O, 2.5V internal
SPECint95 (estimated)	6.2 @ 250 MHz
SPECfp95 (estimated)	5.2 @ 250 MHz
Dhrystone (2.1) MIPS	352 @ 250 MHz
603e Processor Core Functional Units	Integer, Floating-Point, Branch Processing Load/Store, PCI, DMA, Memory Control
Peripheral Logic Functional Units	(I_2O), I^2C, EPIC, ATU, PCI & Memory clocks, ECC controller

- Message Unit
  - (I_2O) Intelligent Input/Output Message Controller
  - Two door-bell registers
  - Inbound and outbound messaging registers
- (I^2C) Inter-Integrated Circuit Controller
  - Full master/slave support
- Embedded programmable interrupt controller (EPIC)
  - Five hardware interrupts (IRQs) or 16 serial interrupts
  - Four programmable timers
- Integrated PCI bus and SDRAM clock generation
- Programmable memory and PCI bus drivers
- Debug Features
  - Watchpoint monitor
  - Memory attribute and PCI attribute signals
  - JTAG/COP – Common On-board Processor for in-circuit hardware debugging

CONTACT INFORMATION

For more information on Freescale processors, point your Web browser to: http://freescale.com/smartnetworks

For all other inquiries about Freescale products, please contact the Freescale Customer Response Center at: Phone: 800-521-6274 or http://www.freescale.com

freescale™ semiconductor