

High-Performance Processors

MPC7448 Host Processor Built on Power Architecture[™] Technology

The MPC7448 is the first discrete high-performance processor, built on Power Architecture™ technology, manufactured on 90 nanometer silicon-on-insulator (SOI) process technology and continues Freescale Semiconductor's strong legacy of providing products with significant processing performance at very low power. The MPC7448 is designed to exceed 1.7 GHz processing performance and offers enhanced power management capabilities. Running at 1.4 GHz, the MPC7448 uses less then 11 watts of power. MPC7448 processors are ideal for leading-edge computing, embedded network control and signal processing applications.

Key architectural features include a MPX bus that scales to 200 MHz, 1 MB of on-chip L2 cache with support for error correcting codes (ECC), and full 128-bit implementation of Freescale's AltiVec[™] technology with the added feature of supporting out-of-order transactions. The MPC7448 is pin-compatible with Freescale's MPC7447 and MPC7447A Power Architecture products, offering an easy upgrade path to better system performance.

Caching In

L2 cache helps keep the processor pipeline full, enabling faster and more efficient processing—and the increase in the MPC7448's L2 cache to 1 MB provides an even greater opportunity for performance gains. The L2 cache is fully pipelined for two-cycle throughput in the MPC7448. It responds with an 11-cycle load latency for an L1 miss that hits in L2 with ECC disabled

Instruction Fetch Branch Unit Completion Unit 32 KB Instruction Cache Dispatch Unit BHT/BTIC AltiVec™ Issue GPR Issue FPR Issue CFX SFXO SFX1 SFX2 Rename Buffers LSU Rename FPU Buffers COMPLEX SIMPLE PERMUTE VRs Rename 60x/MPX Bus Interface

and 12 cycles when ECC is enabled. In the MPC7448, as many as six outstanding cache misses are allowed between the L1 data cache and L2 bus. In addition, the MPC7448 supports a second cacheable store miss. The processors also provide cache locking to the L1 caches so that key performance algorithms and code can be locked in the L1 cache.





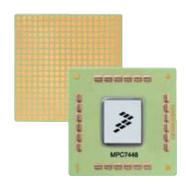
MPC7448 Processor Highlights	
CPU Speeds (internal)	Up to 1.7 GHz
Instructions per Clock	4 (3 + Branch)
L1 Cache (integrated)	32 KB instruction, 32 KB data
L2 Cache (integrated)	1 MB with optional ECC
Typical Power Consumption	21 watts @ 1700 MHz, 11 watts @ 1400 MHz, 8.4 watts @ 1267 MHz
Execution Units	Integer(4), Floating Point Unit, AltiVec [™] (4), Branch, Load/Store
Performance (est.)	2.3 MIPS per MHz (using Dhrystone 2.1 method)
Bus Protocol	MPX/60x
Bus Frequency	200 MHz
Bus Interface	64-bit
Package	360 HICTE BGA LGA
Process Technology	90 nm SOI, Multi-Vt, Triple Gate Oxide, Low-K Dielectric, 10 Year Reliability at 105°C

^{*}Note: The e600 core is identical to the G4 core in previous 7xxx products.

Power Management

Continuing to pursue lower power consumption is a keen focus with the Freescale family of processors, and the MPC7448 is no exception. Power management features include:

- Expanded Dynamic Frequency Switching (DFS) capability enabling improved power savings (divide-by-two and divide-by-four modes are provided)
- Voltage scales down to 1.0V
- Added benefits of 90 nanometer technology include:
 - Multi-Vt and triple gate oxide integrated transistors for low standby power
 - Low-K dielectric for high performance with reduced power and noise
- Temperature sensing diodes included to monitor die temperature



Superscalar Core

The MPC7448 processor features a high-frequency superscalar e600 core, built on Power Architecture technology, capable of issuing four instructions per clock cycle (three instructions plus one branch) into 11 independent execution units:

- Four integer units (three simple plus one complex)
- Double-precision floating point unit
- Four AltiVec technology units (simple, complex, floating and permute)
- · Load/store unit
- · Branch processing unit

AltiVec Acceleration

The MPC7448 includes the same powerful 128-bit AltiVec vector execution unit as found in previous MPC7xxx devices. AltiVec technology may dramatically enhance the performance of applications such as voice-over-Internet Protocol (VoIP), speech recognition, multi-channel modems, virtual private network servers, high-resolution 3-D graphics, motion video (MPEG-2, MPEG-4) and high fidelity audio (3-D audio, AC-3). AltiVec computational instructions are executed in the four independent, pipelined AltiVec execution units. A maximum of two AltiVec instructions can be issued in order to any combination of AltiVec execution units per clock cycle. In the MPC7448, a maximum of two AltiVec instructions can be issued out-of-order to any combination of AltiVec execution units per clock cycle from the bottom two AltiVec instruction queue entries. For example, an instruction in queue one destined for AltiVec integer unit one does not have to wait for an instruction in queue zero that is stalled behind an instruction waiting for operand availability.

Compatibility and Support

The MPC7448 can be a drop-in upgrade for MPC7447 and MPC7447A processors because it is pin-for-pin compatible. In addition, as with all processors, the MPC7448 is fully software compatible with the MPC7xxx family of processors. The Freescale family of processors, built on Power Architecture technology, continues to enjoy the support of a broad set of operating systems, compilers and development tools from third-party vendors.

To learn more, please visit www.freescale.com/powerarchitecture.

Learn More:

For current information about Freescale products and documentation, please visit **www.freescale.com**.



