

Body Control Module based on MPC574xB/C/G Series Microcontrollers

Power Architecture®-based MCU for Automotive and Industrial Applications

Application One-Sheet

Overview

NXP MPC5748G family introduces highly flexible MCUs suitable for advanced central body control application (BCM) in vehicles. The MPC5748G solves five main topics for the BCM:

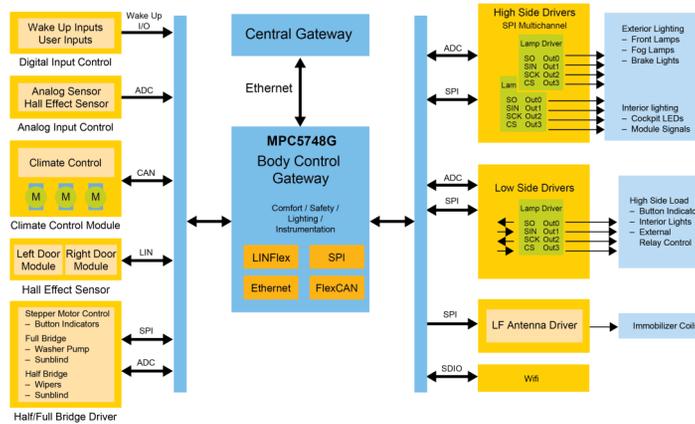
- ▶ A low power architecture that enables pretended networking and cyclic power profiles, with high levels of functionality, at very low power consumption
- ▶ High integration of CPUs and memory, plus timer, communications and ADC interfaces critical for BCM connectivity
- ▶ Programmable hardware security module (HSM), supporting EVITA-mid and SHE Automotive Security levels
- ▶ ISO 26262 ASIL-B architecture, enabling the integration of safety critical applications into the BCM
- ▶ The Flash architecture has virtual remapping functionality enabling seamless Firmware over-the-air updates (FOTA) of the MCU with zero ECU downtime

The MPC5748G MCU is a device with a diverse set of communication protocols such as Ethernet, FlexRay™, CAN FD, USB, MLB, etc., making this device

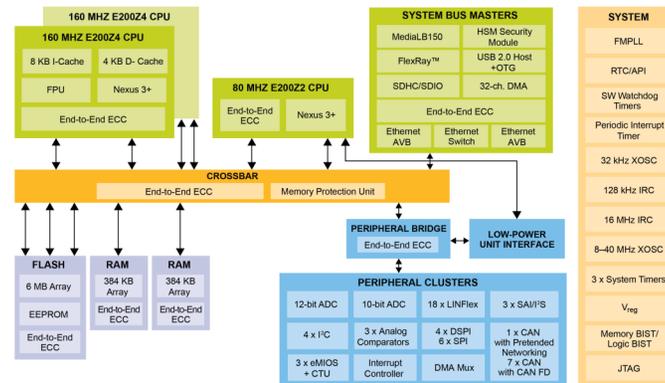
MPC574xB/C/G Specifications

Flash	Up to 6 MB	Timer/PWM	Up to 96 ch., eMIOS
RAM	Up to 768 KB	Other Timer	Up to 16 PIT, 3 STM, 4 SWT
Core	Up to 2 x Z4, 1 x Z2	Analog	Up to 2 ADC (10 & 12 bit), 3 Comparators, CTU
Speed	2 x 160 MHz 1 x 80 MHz	Communications	Up to 4 DSPI, 6 SPI, 18 LIN, 8 CAN FD, 4 I ² C, 1xUSB, 2 x ENET, 1xSDHC
Op Range	3.3 to 5.5 V	Safety & Security	HSM, PASS and TDM, FCCU
Temp	-40 to 125 °C	Low Power	LPU_SLEEP, LPU_STOP, LPU_STANDBY mode sup-
Package	176LQFP 256/324BGA		

Application Block Diagram



MCU Block Diagram



Features

- ▶ Automotive peripherals:
 - CAN FD, many LINs
 - Ethernet, with IEEE® 1588 & AVB
- ▶ ADC and timer channels:
 - 2 ADCs, ADC0 (10 bit) and ADC1 (12 bit)
 - Cross trigger unit to synchronize timers and ADCs
 - eMIOS
- ▶ Advanced low power architecture:
 - Power island with Z2 CPU, RAM and peripheral subset, providing low power consumption for key-off functionality
 - Analog comparators to enable wake-up from deepest low power modes on analog threshold detection
- ▶ Security:
 - Hardware security module, physically isolated from the application resources
- ▶ Supporting asymmetric, hardware accelerated and symmetric crypto operations
 - Product life-cycle scheme, locking down features
- ▶ Functional Safety:
 - ASIL-B, use system level to achieve higher level (e.g., for lighting)
- ▶ Firmware Over-The-Air update:
 - Zero performance impact for FOTA updates (flexible read-while-write partitions, multi-ported Flash)
 - Simplified software complexity for FOTA updates, using flash remapping mechanism
 - Flash programming protection and logging

Enablement Tools

- ▶ Development hardware:
 - MPC574XG-MB family motherboard
 - MPC574XG-256DS, MPC574XG-176DS or MPC574XG-324DS daughterboard
 - DEVKIT-MPC5748G
- ▶ Runtime software: Flash and EEPROM driver
- ▶ Compiler: Green Hills®, Wind River®, HighTec®
- ▶ Debugger: Lauterbach®, iSystem®, PLS®, Green Hills®, P&E®
- ▶ Software Enablement:
 - S32 Design Studio with SDK
 - AUTOSAR 4.0 MCAL + OS

www.nxp.com/MPC5748G

NXP and the NXP logo are trademarks of NXP B.V. All other product or service names are the property of their respective owners. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org. All rights reserved. © 2017 NXP B.V.

Document Number: BCMAPPFS REV 1

