



*32-Bit Controllers*

**Class Room Training – CT503**

## **MPC5500 Family Workshop**

***Target Applications: Automotive, Commercial, Industrial, and Aerospace***

To learn more: Visit [www.freescale.com](http://www.freescale.com) and type document number MPC5500FS in the Key Word Search, located in the upper right hand corner.

**Course Description:** A 3-day workshop that covers e200z6 Power Architecture core, memory protection and memory controller, cross-bar switch and all internal/external buses. Also included are details of all on-chip peripherals with hands-on provided on most modules.

After completing the workshop, the participant will understand the basic concepts of the Power Architecture and all major functional blocks of the MPC5500 devices. With hands-on examples and development tools, the participant will be able to program on-chip peripherals and optimize system design.

**Who Should Attend:** Software and system engineers who need to come up to speed quickly on how to program and with the MPC5500 family.

**Participants will be provided:** A hard copy of the workshop notes, lab book and textbook. A CDROM of all the lab experiments and demo version of the development tools is also provided.

**Prerequisite:** Knowledge/experience of some microprocessor/microcontroller is necessary.

**Course Fees:** \$1,000 USD per participant

**Course Date and Location:** August 19 - 21, 2008, Phoenix, Arizona

## Course Enrollment

**Open Enrollment:** To view a list of open enrollment workshops for the MPC5500 Family:

1. Navigate to:  
[http://www.freescale.com/webapp/sps/site/training\\_information.jsp?code=CT\\_503\\_MPC5500\\_Family](http://www.freescale.com/webapp/sps/site/training_information.jsp?code=CT_503_MPC5500_Family)
2. Select **View Scheduled Events** Button (if button is missing, no classes are currently offered).
3. Select the **Register Link** for the class you wish to attend.

**On-Site Enrollment:** As with any of our Technical Training courses, the MPC5500M Family workshop can be taught at your facility and customized to fit your needs. The cost of a customer on-site class is dependent on the customer's training requirements.

**Contact:** [techtraining@freescale.com](mailto:techtraining@freescale.com) for more information.

### MPC5500 Family Workshop Agenda

Day 1	Day 2	Day 3
<p><b>MPC5500 Overview</b></p> <ul style="list-style-type: none"> <li>• Main Features and Road Map</li> <li>• Compatibility and Scalability</li> </ul> <p><b>Power Architecture Core</b></p> <ul style="list-style-type: none"> <li>• Programming Model</li> <li>• Classic PowerPC Instruction Set</li> <li>• Power Architecture Exceptions and Interrupts</li> <li>• Interrupt Controller</li> <li>• Memory Management Unit (MMU)</li> <li>• Unified Cache</li> </ul>	<p><b>System Initialization</b></p> <ul style="list-style-type: none"> <li>• PLL and System Clock Generation</li> <li>• Pad (Pin) Assignment and Configuration</li> <li>• Boot-assist Module (Boot Sequence)</li> <li>• Device Configuration</li> <li>• System Reset Sources and Reset Handling</li> <li>• Software Initialization Checklist</li> </ul> <p><b>Peripherals</b></p> <ul style="list-style-type: none"> <li>• Enhanced DMA (eDMA)</li> <li>• Modular I/O System (eMIOS)</li> </ul>	<p><b>Peripherals continued...</b></p> <ul style="list-style-type: none"> <li>• Enhanced Timer Processor Unit (eTPU)</li> <li>• Queued A/D Converter (eQADC)</li> <li>• Enhanced Serial Communication</li> <li>• Interface (eSCI) and LIN Bus</li> <li>• DSPI</li> <li>• FlexCAN</li> </ul> <p><b>System Memory</b></p> <ul style="list-style-type: none"> <li>• Error Correction Code</li> <li>• SRAM</li> <li>• Flash</li> </ul> <p><b>Tools</b></p> <ul style="list-style-type: none"> <li>• Nexus Summary</li> <li>• Calibration</li> </ul>

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