i.MX93_1P87f

Mask Set Errata

Rev. 1 — 27 February 2025 Errata

1 Mask Set Errata for Mask 1P87f

1.1 Revision History

This report applies to mask 1P87f for these products:

- MIMX935xxxxxxAB
- MIMX933xxxxxxAB
- MIMX932xxxxxxAB
- MIMX931xxxxxxAB
- MIMX930xxxxxxAB

Table 1. Revision History

Revision	Release Date	Significant Changes
1	2/2025	The following errata were added. • ERR052357 • ERR051588 • ERR052674 • ERR052675 • ERR052438 • ERR009156 • ERR052122 • ERR052348 • ERR052198 • ERR052292 The following errata were revised. • ERR051725 • ERR051186
0	12/2023	Initial Revision

1.2 Errata and Information Summary

Table 2. Errata and Information Summary

Erratum ID	Erratum Title
ERR051390	CCM: CCGR doesn't wait for stop ack from the peripherals in low power sequence.
ERR051051	Core: A partially completed VLLDM might leave Secure floating-point data unprotected
ERR050505	Core: Access permission faults are prioritized over unaligned Device memory faults
ERR050504	Core: Sorting of pending interrupts might be wrong when high latency IRQs are pending
ERR050875	CoreSight: AHB-AP can issue transactions where HADDR[1:0] is not aligned to HSIZE on the AHB

Table 2. Errata and Information Summary*...continued*

Erratum ID	Erratum Title
ERR050839	Cortex-A55: Speculative AT instruction using out-of-context translation regime could cause subsequent request to generate an incorrect translation
ERR050838	Cortex-A55: Update of DBM or AP bits without break-before-make might result in incorrect hardware dirty bit update
ERR051220	DDRC: DDRC Register Access Not Allowed In Half-Speed Mode
ERR051252	DDRC: Memory controller may not operate properly when per-bank refresh is enabled
ERR051301	DDRC: Memory controller Performance Degraded During Write Traffic
ERR052292	DDRC: Memory controller Performance Degraded when using certain values for Read-to-Precharge time
ERR051691	DDRC: Memory Select Error Can Cause DDRC Failure
ERR051554	DDRC: The DDR Controller idle status is not accurate when using PLL bypass mode with data rate ≤ 533MT/s.
ERR051219	DDRC: The DDRC does not automatically apply derated timing values to some timing parameters
ERR051241	eDMA4: Channel preemption feature can operate incorrectly
ERR051776	eDMA4: DMA may fail to catch request when Flexio Root Clock is over 50 MHz
ERR051336	eDMA4: Swap feature with 8-bit swap size and 16-bit transfer size does not work
ERR051325	eDMA4: The feature of cancelling the remaining data transfer is not working effectively
ERR051337	eDMA4: transfer will fail in one certain case.
ERR051326	eDMA4:TCDn_CSR[ESDA] and TCDn_CSR[EEOP] are not functional
ERR051683	ENET_QOS: EQOS SWR cannot be self cleared in RMII mode.
ERR051029	ENET_QOS: Gate Control List Switching is Incorrect for Intermediate Cycles When CTR is Less Than GCL Execution Time
ERR052348	ENET_QoS: IEEE 802.1Qav CBS Algorithm Does Not Include Minimum IPG of Packet in Credit Computation
ERR052438	FlexCAN: CAN frame may drop when using Enhanced RX FIFO
ERR051205	FLEXIO: Both PCLK and FCLK must be enabled when it is as a wakeup source.
ERR011377	FlexSPI: DLL lock status bit not accurate due to timing issue
ERR051612	Fuse: Limitations for accessing fuse-disabled features
ERR052675	I/O: High frequency operation impacted due voltage stress when operating at 3.3V
ERR052674	I/O: Potential IO pad failure when configured for 3.3V operation
ERR052122	I3C : Data size limitation in Message mode DDR transfer
ERR051186	I3C: Extended data will be lost when sent after timestamp in async mode 0 in I3C target mode
ERR051120	I3C: The Not Acknowledge Error bit in the Master Errors and Warnings register (MERRWARN[NACK]) is not set when slave does not acknowledge High Data Rate - Double Data Rate (HDR-DDR) read.
ERR009156	LDB: OpenLDI 18-bit SPWG mode does not work correctly
ERR051608	LPSPI: PRESCALE bits in TCR Register has limitation
ERR051588	LPSPI:Reset transmit FIFO after FIFO underrun by LPSPI Slave.

Table 2. Errata and Information Summary*...continued*

Erratum ID	Erratum Title
ERR051421	SAI: Synchronous mode with bypass is not supported
ERR051709	TRDC: OSC24M cannot be the clock reference selected accessing MEDIAMIX TRDC DAC
ERR051725	USB: With the USB controller configured as device mode, Clearing the RS bit of USBCMD register fails to cause USB device to be detached
ERR052021	uSDHC: Sometimes uSDHC does not work under VDD_SOC low drive mode and nominal mode
ERR052198	uSDHC: eMMC CQE may timeout due to a HW logic issue
ERR052357	uSDHC: Low probability get stale data during read transfer.
ERR051302	WDOG: Reset delay does not work

2 Known Errata

ERR051390: CCM: CCGR doesn't wait for stop ack from the peripherals in low power sequence.

Description

In the low power sequence, once CCGR receive the request of LPCG step from GPC to gate off IP clocks, the CCGR will provide lpcg_done to GPC without waiting for IP's stop ack. Then, GPC will execute next low power step, such as shutoff PLLs, which may result in gating off the peripheral IP clock without finishing handshake between ccm and IP.

Workaround

SW need guarantee these peripheral IP (I2C1~8/CAN1/eDMA1/CAN2/ENET1/eDMA2/FlexSPI.) in idle status before system enter low power mode, which can be guaranteed in the linux mechanism.

ERR051051: Core: A partially completed VLLDM might leave Secure floating-point data unprotected

Description

Arm errata 2219175

Affects: Cortex-M33

Fault Type: Programmer Category B

Fault Status: Present in r0p0, r0p1, r0p2, r0p3, r0p4, r1p0. Open.

The VLLDM instruction allows Secure software to restore a floating-point context from memory. Due to this erratum, if this instruction is interrupted or it faults before it completes, then Secure data might be left unprotected in the floating point register file, including the FPSCR.

Configurations affected:

This erratum affects all configurations of the Cortex-M33 processor configured with the Armv8-M Security Extension and the Floating-point Extension.

Conditions:

This erratum occurs when all the following conditions are met:

• There is no active floating-point context, (CONTROL.FPCA==0)

• Secure lazy floating-point state preservation is not active, (FPCCR_S.LSPACT==0)

• The floating-point registers are treated as Secure (FPCCR_S.TS==1)

• Secure floating-point state needs to be restored, (CONTROL_S.SFPA == 1)

• Non-secure state is permitted to access to the floating-point registers, (NSACR.CP10 == 1)

• A VLLDM instruction has loaded at least one register from memory and does not complete due to an interrupt or fault

Implications:

If the floating-point registers contain Secure data, a VLSTM instruction is usually executed before calling a Non-secure function to protect the Secure data. This might cause the data to be transferred to memory (either

directly by the VLSTM or indirectly by the triggering of a subsequent lazy state preservation operation). If the data has been transferred to memory, it is restored using VLLDM on return to Secure state. If the VLLDM is interrupted or it faults before it completes and enters a Non-secure handler, the partial register state which has been loaded will be accessible to Non-secure state.

Workaround

To avoid this erratum, software can ensure a floating-point context is active before executing the VLLDM instruction by performing the following sequence:

• Read CONTROL_S.SFPA

• If CONTROL_S.SFPA==1 then execute an instruction which has no functional effect apart from causing context creation (such as VMOV S0, S0)

ERR050505: Core: Access permission faults are prioritized over unaligned Device memory faults

Description

Cortex-M33 1080541-C :

A load or store which causes an unaligned access to Device memory will result in an UNALIGNED UsageFault exception. However, if the region is not accessible because of the MPU access permissions (as specified in MPU_RBAR.AP), then the resulting MemManage fault will be prioritized over the UsageFault.

Workaround

There is no workaround.

However, it is expected that no existing software is relying on this behavior since it was permitted in Armv7-M.

ERR050504: Core: Sorting of pending interrupts might be wrong when high latency IRQs are pending

Description

Cortex-M33 1540599-C:

The NVIC contains a pending tree which sorts all pending and enabled interrupts based on priorities. If DHCSR.C_DEBUGEN and DHCSR.C_MASKINTS are 1, DHCSR.S_SDE is 0 and halting debug is allowed, then Nonsecure PendSV, Non-secure SysTick, and Non-secure IRQs should be masked off and they should not affect the sorting of pending and enabled secure interrupts. If multiple high latency IRQs are pending and enabled with different security targets and priorities, then Non-secure IRQs which should be masked off might cause the pending tree output to be a pending Secure nterrupt without highest priority. This is because of incorrect masking before doing priority comparisons in the tree.

Workaround

There is no workaround for this erratum.

ERR050875: CoreSight: AHB-AP can issue transactions where HADDR[1:0] is not aligned to HSIZE on the AHB

Description

ARM errata 1624041

This erratum affects the following components:

• AHB Access Port.

The ARM Debug Interface v5 Architecture Specification specifies a TAR (Transfer Address Register) in the MEM-AP that holds the memory address to be accessed.

TAR[1:0] is used to drive HADDR[1:0] when accesses are made using the Data Read/Write register DRW.

When the AHB-AP is programmed to perform a word or half-word sized transaction the AHB-AP does not force HADDR[1:0] to be aligned to the access size. This can result in illegal AHB transactions that are not correctly aligned according to HSIZE if HADDR[1:0] is programmed with an unaligned value.

Conditions:

1) TAR[1:0] programmed with a value that is not aligned with the size programmed in the CSW register of the AHB-AP.

2) An access is initiated by an access to the Data Read/Write Register (DRW) in the AHB-AP.

Implications:

As a result of the programming conditions listed above, AHB-AP erroneously initiates an access on the AHB with HADDR[1:0] not aligned to the size on HSIZE. This might initiate an illegal AHB access.

Workaround

TAR[1:0] must be b00 for word accesses, TAR[0] must be b0 for half-word accesses.

Software program should program TAR with an address value that is aligned to transaction size being made.

ERR050839: Cortex-A55: Speculative AT instruction using out-of-context translation regime could cause subsequent request to generate an incorrect translation

Description

Arm errata 1530923

Fault Type: Programmer Category B

Fault Status: Present in r0p0, r0p1, r1p0, and r2p0. Open.

A speculative Address Translation (AT) instruction translates using registers that are associated with an out-of-context translation regime and caches the resulting translation in the TLB. A subsequent translation request that is generated when the out-of-context translation regime is current uses the previous cached TLB entry producing an incorrect virtual to physical mapping.

Configurations Affected:

This erratum affects all configurations.

Conditions:

1. A speculative AT instruction performs a table walk, translating a virtual address to a physical address using registers associated with an out-of-context translation regime.

2. Address translation data that is generated during the walk is cached in the TLB.

3. The out-of-context translation regime becomes current and a subsequent memory access is translated using previously cached address translation data in the TLB, resulting in an incorrect virtual to physical mapping.

Implications:

If the above conditions are met, the resulting translation would be incorrect.

Workaround

When context-switching the register state for an out-of-context translation regime, system software at EL2 or above must ensure that all intermediate states during the context-switch would report a level 0 translation fault in response to an AT instruction targeting the out-of-context translation regime. A workaround is only required if the system software contains an AT instruction as part of an executable page.

ERR050838: Cortex-A55: Update of DBM or AP bits without break-before-make might result in incorrect hardware dirty bit update

Description

Arm errata 1024718

Affects: Cortex-A55

Fault Type: Programmer Category B

Fault Status: Present in r0p0, r0p1, r1p0, and r2p0. Open.

If the hardware dirty bit update is enabled, and the DBM or AP bits in the translation table descriptor are updated by software without using break-before-make, then it is possible for hardware to incorrectly update the AP bits based on the old value of those bits.

Configurations Affected:

This erratum affects all configurations of the Cortex-A55 processor.

Conditions:

1. The hardware dirty bit update is enabled for stage1 (TCR_ELx.HA and TCR_ELx.HD are both set) or stage2 (VTCR_EL2.HA and VTCR_EL2.HD are both set).

2. A store instruction is executed, which causes a hardware dirty bit update for the translation table descriptor which has DBM=1 and no write permission because of either AP[2]=1 or S2AP[1]=0.

3. At the same time as the store, the OS or hypervisor writes to the same translation table descriptor to update the AP, S2AP, or DBM bits, without using a break-before-make procedure.

4. The new translation table descriptor is a valid translation, but does not require the dirty bit update for the store because either the DBM bit is now clear, or the AP/S2AP bits would still cause a permission fault to occur even after a dirty bit update.

Implications:

The permission checking of the store is performed on the old version of the translation table descriptor, while the AP/S2AP bit is updated in the new version of the translation table descriptor. This could lead to an inconsistent situation where the store is executed but the OS or hypervisor is not expecting the store to have permission to execute.

Workaround

The OS or hypervisor can use a break-before-make procedure if it needs to update the DBM or AP/S2AP bits.

Alternatively, it can use software management of the dirty bit update.

ERR051220: DDRC: DDRC Register Access Not Allowed In Half-Speed Mode

Description

After issuing a Hardware Fast Frequency Change (HWFFC) request, the DDRC operates in half-speed mode. While operating in this mode, if a DDRC register read or write is requested, the internal state counters may get corrupted. In addition, some of the fields of TIMING_CFG_12/13/14 are not used during half-speed operation.

Workaround

If a DDRC register access is required while operating at half-frequency after an HWFFC switch, first switch to full-speed via HWFFC before accessing the register.

ERR051252: DDRC: Memory controller may not operate properly when per-bank refresh is enabled

Description

When the DDRC is in per-bank refresh mode, it may violate the tRFCpb timing by issuing a per-bank refresh to the same bank or an all-bank refresh after a prior per-bank refresh. The memory controller guarantees that TIMING_CFG_9[REFTOREF_PB] (programmed to tpbR2pbR) is met between any two per-bank refreshes. However, it does not guarantee the TIMING_CFG_9[REFREC_PB] (tRFCpb) when issuing a per-bank refresh to the same bank or when issuing an all-bank refresh after a per-bank refresh. Per bank refresh is an optional feature.

Workaround

While using per-bank refresh (TIMING_CFG_9[REFREC_PB] != 0x0), program both TIMING_CFG_9[REFTOREF_PB] and TIMING_CFG_9[REFREC_PB] to meet the maximum of (tRFCpb, tpbR2pbR). tRFCpb is expected to be the maximum of those two timing specs.

Another workaround is to disable per-bank refresh by programming TIMING_CFG_9 to 0x0.

ERR051301: DDRC: Memory controller Performance Degraded During Write Traffic

Description

During processing of certain write transactions, the write performance is degraded.

Workaround

To prevent the write performance degradation, set bit 7 (value of 0x80) to register offset 0xf04 within the DDRC register space.

Note: The "*_timing.c" file generated by DDR tool implements the workaround.

ERR052292: DDRC: Memory controller Performance Degraded when using certain values for Read-to-Precharge time

Description

The following settings in TIMING_CFG_2[RD_TO_PRE] (Read-to-Precharge time) will result in a memory performance degradation: 11, 12, 13, and 14 clock cycles.

Workaround

In cases where the calculated tRTP clock cycle setting results in any of these values (11, 12, 13, 14), it is necessary to round up this setting to 15 clock cycles (0_1111). This allows the interface to meet the minimum JEDEC specification timing requirement for tRTP of “max(7.5ns, 8nCK)“ while also avoiding the performance degradation and to achieve optimal performance.

Note: The "*_timing.c" file generated by DDR tool implements the workaround.

ERR051691: DDRC: Memory Select Error Can Cause DDRC Failure

Description

A memory select error (ERR_DETECT[MSE]) can be detected by the DDRC if a memory transaction is received by the DDRC that is outside the programmed CSn_BNDS register(s). This is considered a programming error. Under the most conditions, the DDRC will detect this condition, report the memory select error and continue operating normally. However, if configuring the DDRC for open-page mode and all-bank refresh mode and dynamic refresh rate all at once, a memory select error may cause a DDRC failure. The memory select error will also be reported as expected also in this condition.

Workaround

Occurrence of memory select errors is not expected in production software as system developers should ensure that memory transactions do not occur outside the programmed CSn_BNDS register(s). In the event where a memory access is attempted outside of the programmed CSn_BNDS register(s) the possibility of a DDRC failure condition can be eliminated by applying any of the following settings:

* Auto pre-charge mode is set (DDR_SDRAM_INTERVAL[BSTOPRE] = 0)

* The per bank refresh mode is set (TIMING_CFG_9)

* The dynamic refresh rate is disabled (DDR_SDRAM_CFG_3[DYN_REF_RATE_EN] = 0)

* Disable the memory select error (ERR_DISABLE[MSED] = 1)

If none of the above settings are used to avoid the potential failure condition, then the DDRC can be tested after a memory select error is detected. If it is non-functional, then a reset is required.

ERR051554: DDRC: The DDR Controller idle status is not accurate when using PLL bypass mode with data rate ≤ 533MT/s.

Description

The DDR Controller idle status flag is not accurate when using the PLL bypass mode with data rates ≤ 533MT/s. As a result when using the Software Fast Frequency Change(SWFFC) routine to switch from the PLL bypass mode with data rates ≤ 533MT/s, instead of polling for the DDRC idle state, a timeout should be used to make sure that the DDR Controller has finished all transactions and can enter self-refresh mode.

In addition, when in PLL bypass mode with data rates ≤ 533MT/s, the automatic clock gating feature cannot be enabled

Workaround

If the Software Fast Frequency Change(SWFFC) routine is used to switch from the PLL bypass mode, a delay timeout is required to ensure the DDR controller is idle.

Before resetting the DDRC;

3 micro second delay; //this delay to ensure DDRC is in Idle state.

then Reset the DDRC (DDR_SDRAM_CFG_3[31]= 1);

ERR051219: DDRC: The DDRC does not automatically apply derated timing values to some timing parameters

Description

While using the dynamic refresh rate feature (via DDR_SDRAM_CFG_3[DYN_REF_RATE_EN], the DDRC automatically adjusts the refresh rate based on the temperature of the DRAM. This works correctly. When the LPDDR4/4X MR4 provides a refresh rate of the value 3'b110 to the controller, the DDRC should use the values in TIMING_CFG_2[DERATE_VAL] to derate the following timing parameter configurations:

- {TIMING_CFG_3[EXT_PRETOACT], TIMING_CFG_1[PRETOACT]}
- {TIMING_CFG_3[EXT_ACTTOPRE], TIMING_CFG_1[ACTTOPRE]}
- {TIMING_CFG_3[EXT_ACTTORW], TIMING_CFG_1[ACTTORW]}
- {TIMING_CFG_3[EXT_ACTTOACT], TIMING_CFG_1[ACTTOACT]}
- TIMING_CFG_8[PRE_ALL_REC]

However, the derating for these specs are not applied correctly within the DDRC. Note that this erratum does not affect the dynamic refresh interval updates.

Workaround

1. If the application is specified to operate at a temperature less than 85 °C, you can enable or disable DDR_SDRAM_CFG_3[DYN_REF_RATE_EN]. In this case, no timing parameters require derating and if DDR_SDRAM_CFG_3[DYN_REF_RATE_EN] is enabled, the refresh rate will automatically adjust per feedback from the LPDDR4/4X device.

2. If the application is specified to operate at a temperature higher than 85 °C, apply the derating value as a fixed delay for all temperatures and also enable DDR_SDRAM_CFG_3[DYN_REF_RATE_EN] to ensure that the refresh rate is automatically adjusted based on the temperature of the DRAM.

While using the workaround #2, apply the derated timing values to the following register configurations when programming the DDRC:

- {TIMING_CFG_3[EXT_PRETOACT], TIMING_CFG_1[PRETOACT]}
- {TIMING_CFG_3[EXT_ACTTOPRE], TIMING_CFG_1[ACTTOPRE]}
- {TIMING_CFG_3[EXT_ACTTORW], TIMING_CFG_1[ACTTORW]}
- {TIMING_CFG_3[EXT_ACTTOACT], TIMING_CFG_1[ACTTOACT]}
- TIMING_CFG_8[PRE_ALL_REC]

Note that the derating for these is typically 1.875 ns, but the DRAM vendor datasheet should be referenced.

Note: Verify with DRAM vendor about the high temperature, which is 85 °C

Note: The "*_timing.c" file generated by DDR tool implements the workaround.

ERR051241: eDMA4: Channel preemption feature can operate incorrectly

Description

Channel preemption can cause incorrect behavior under the following conditions:

• The preempted channel has CHx_PRI[ECP]=1

• The preempting channel has a higher priority than the preempted channel based on the setting of CHx_PRI[APL]

• The preempting channel is activated while the preempted channel has an active transfer on the AXI bus

Workaround

Do not use the preemption feature. For all channels, the TCD register CHn_PRI[31:30] must have at least one of the two settings:

1. Keep CHn_PRI[ECP] = 1'b0 - The channel cannot be suspended by a higher priority channel's service request (default).

2. Set CHn_PRI[DPA] = 1'b1 - The channel can be temporarily suspended by the service request of a higher priority channel.

ERR051776: eDMA4: DMA may fail to catch request when Flexio Root Clock is over 50 MHz

Description

The working sequence of a use case is as follows:

1. The eDMA4 moves data to shifter buffer

2. Once the shifter buffer is full, the timer0 (for example) is detected

3. Then, the timer0 sends pulse to the shifter

4. The pulse triggers the data loading from shifter buffer to the corresponding shifter

5. Since the shifter buffer is empty, the request to DMA goes high. But if the Flexio Root Clock is too fast, the eDMA4 may miss the request.

Workaround

Use an extra timer2 (for example) between buffer and timer0 to add delay:

1. The eDMA4 moves data to shifter buffer

2. Once the shifter buffer is full, the timer2 is detected

3. Timer2 generates pulses to timer0

4. Timer0 sends pulse to the shifter. The delay is added here

5. The pulse triggers the data loading from shifter buffer to the corresponding shifter

6. Since the shifter buffer is empty, the request to DMA goes high and the eDMA4 catches the request.

ERR051336: eDMA4: Swap feature with 8-bit swap size and 16-bit transfer size does not work

Description

The DMA SWAP function that allows software to select data portions to be swapped between the read data to the write data is not working in the following cases:

1. CHn_CSR[15:12]=0001 and SSIZE=001

2. CHn_CSR[15:12]=1001 and DSIZE=001

Workaround

Do not use SWAP function for the described cases.

ERR051325: eDMA4: The feature of cancelling the remaining data transfer is not working effectively

Description

eDMA4 does not cancel the current bus activity. Bus transactions will continue normally and complete the transfer size requested by the NBYTES parameter.

Workaround

Do not use the cancel feature.

ERR051337: eDMA4: transfer will fail in one certain case.

Description

eDMA4 transfer can go wrong if both of the following conditions are true:

1. If the transfers are unaligned with the transfer sizes for Transfer Control Descriptor (TCD) source or destination addresses.

2. If the minor loop crosses the 4K bytes boundary.

Workaround

Make sure TCD source and destination addresses alignment.

ERR051326: eDMA4:TCDn_CSR[ESDA] and TCDn_CSR[EEOP] are not functional

Description

If Store Destination Address is enabled (ESDA = 1) and End of Packet Processing is enabled (EEOP = 1), the address stored will be invalid if the EOP signal is triggered. It will not correspond correctly to the last address transferred when EOP is signalled.

Workaround

TCDn_CSR[EEOP] must be disabled.

ERR051683: ENET_QOS: EQOS SWR cannot be self cleared in RMII mode.

Description

After EQOS SWR bit is set, EQOS should start reset procedure, and clear the SWR bit itself after reset is finished.

However, due to the defect, part of the reset procedure remains unfinished and the SWR bit cannot be cleared automatically.

Workaround

Setting PS and FES bits after the SWR bit was set, and polling SWR to ensure the reset procedure is finished.

ERR051029: ENET_QOS: Gate Control List Switching is Incorrect for Intermediate Cycles When CTR is Less Than GCL Execution Time

Description

Impacted Configurations:

DWC_ether_qos configurations in which you select Enable Enhancements to Scheduling Traffic (EST) feature.

Parameter:

DWC_EQOS_AV_EST == 1

Versions Affected: 5.00a and later

Defect Summary:

The EST (Enhancements to Scheduled Traffic) scheduler switches to the next Gate Control List (GCL) after executing the current Gate-Control List (GCL) regardless of the difference between the Cycle Time Register (CTR) value, and sum of the Base Time Register (BTR) and Time Intervals (TI) of the GCL rows whose execution is complete. If the GCL execution takes longer than the cycle time, the GCL is truncated at the cycle time, and the subsequent loop begins at

BTR + N * Cycle Time, where N represents the iteration number, an integer.

However due to the defect, in the following situations, the GCL incorrectly updates the internal BTR twice. As a result, the GCL skips the execution of the next GCL loop:

CTR value is less or greater than GCL loop execution time.

The difference between the CTR and the sum of the BTR and Time Intervals of completely executed GCL rows is less than 8 PTP clock periods expressed in ns.

Impacted Use Cases:

The CTR value that you programmed is not equal to GCL execution time. GCL execution time is as follows:

BTR + N * sum of time intervals of valid GCL rows.

Workaround

Program the CTR, BTR, and Time Intervals of the GCL rows such that the difference between the CTR and the sum of the BTR and time intervals of fully executed GCL rows is greater than 8 PTP clock periods expressed in ns.

Alternatively, the CTR must be equal to the sum of the BTR and Time Intervals of the fully executed GCL rows.

ERR052348: ENET_QoS: IEEE 802.1Qav CBS Algorithm Does Not Include Minimum IPG of Packet in Credit Computation

Description

MAC decrements the credit only up to the last byte of the packet data (that is, the last byte of the Frame Check Sequence (FCS) transfer) and increments the credit during the subsequent nominal IPG period that is associated with that packet.

Workaround

You must compute the additional/extra bandwidth that the TXQ consumes due to the defective algorithm. For this, you must use the abovementioned formula and example, substituting the values with the average length of the packets that are transmitted for the use case. Then, you must program the parameters that determine the fractional bandwidth for this TXQ to reflect the lesser percentage, such that the effective programmed fractional bandwidth is closer to the desired one.

ERR052438: FlexCAN: CAN frame may drop when using Enhanced RX FIFO

Description

An incoming CAN frame will be lost (i.e not latched into its expected Enhanced Rx FIFO data element), if both following two conditions are met simultaneously. There will be no indication that the frame was lost.

Conditions:

1. A write access is made to the message buffer Control and Status word (MB_CS) of a specific message buffer corresponding to the expected Enhanced Rx FIFO data element. Each Enhanced Rx FIFO data element corresponds to different message buffers impacted by this erratum and cannot be determined by software.

2. Depending on the timestamp configuration, the write access is made when receiving a frame at one certain Controller Host Interface (CHI) clock cycle either:

a. Around the time between the seventh bit of EOF and the second bit of IFS if timestamp is disabled (CTRL2[TSTAMPCAP] = 00b) or

b. Around the time between the fifth bit of EOF and seventh bit of EOF if timestamp is enabled (CTRL2[TSTAMPCAP] = 01b or 10b or 11b)

Workaround

To avoid the potential for dropped CAN frames, one of the following options may be implemented:

Workaround #1 : Disable Enhanced RX FIFO feature.

Workaround #2 : If the Enhanced RX FIFO feature is enabled, restrictions apply to certain Message Buffer (MB) numbers. Either do not use these MB's at all or at minimum, avoid updating the Control and Status word of these MBs when any reception to the Enhanced Rx FIFO could occur. This means, it would be safe to update

the Control and Status word of these MBs when the FlexCAN is for example in Freeze mode or when it is ensured against frame reception from the CAN bus. Below are the MB numbers that have these restrictions:

ERR051205: FLEXIO: Both PCLK and FCLK must be enabled when it is as a wakeup source.

Description

FlexIO has two channel interfaces, and FlexIO can support low power modes with bus clock (PCLK) disabled and functional clocks (FCLK) enabled. It requires the two channels to assert based on the mode being entered, but currently the two channels are driven the same. So, both PCLK and FCLK have to be enabled when FLEXIO is a wakeup source.

Workaround

Both PCLK and FCLK should be enabled when it is as a wakeup source.

ERR011377: FlexSPI: DLL lock status bit not accurate due to timing issue

Description

After configuring DLL and the lock status bit is set, still may get wrong data if immediately read/write from FLEXSPI based external flash due to timing issue

Workaround

Adding a delay time (equal or more than 512 FlexSPI root clock cycle) after the DLL lock status is set.

ERR051612: Fuse: Limitations for accessing fuse-disabled features

Description

When the system tries to access those modules on parts that disable the NPU, USB2, PXP, CSI, DSI, or LVDS fuse, it results into the following behavior:

• Parts with the NPU and PXP fuses are disabled; accessing them causes the core to hang.

• Parts with the CSI and DSI fuses are disabled; accessing them causes the read register to return all 0x00000000.

• Parts with the USB2 and LVDS (LVDS register is in mediamix GPR) fuses are disabled; accessing them still lets the register to be accessible.

Workaround

Do not access the IP that is fuse disabled or use the TRDC SW workaround to block register access for a disabled IP.

ERR052675: I/O: High frequency operation impacted due voltage stress when operating at 3.3V

Description

When IO interfaces are powered by 3.3V supplies, they are limited in speed to no faster than 56MHz for commercial qualified parts and 52MHz for standard industrial, extended industrial and automotive qualified parts. This potentially impacts interfaces such as FlexSPI/XSPI, Parallel display (LCDIF) and Parallel camera (ISI) etc.

Workaround

To achieve operational frequencies higher than specified above for impacted IO pads, connect the respective IO power supplies to 1.8V instead. No Silicon fix is planned.

ERR052674: I/O: Potential IO pad failure when configured for 3.3V operation

Description

Three GPIO pads ENET1_MDIO, SD2_CLK and I2C1_SDA and their corresponding MUXed functions may fail to operate correctly if their respective SoC power rails NVCC_WAKEUP, NVCC_SD2 and NVCC_AON are configured to 3.3V operation. The IO pad failure occurs regardless of pad configuration or usage and can further progress to impact other IO circuitry in a variety of ways that could result in failure in operation of the entire 3.3V power domain. During this specific configuration it is possible that the lifetime of the part will be degraded.

Workaround

To prevent this failure the SoC power rails NVCC_WAKEUP, NVCC_SD2 and NVCC_AON should instead be configured to 1.8V operation, while adding external level shifters to interface with any peripherals requiring 3.3V operation.

This issue will be addressed in next silicon revision. With the revised silicon no additional software, hardware or end user board design changes will be necessary.

ERR052122: I3C : Data size limitation in Message mode DDR transfer

Description

The message length in DDR message (DMA) mode is defined in MWMSG_DDR_CONTROL2 [9:0].LEN field. Bits [9:8] of this field are ignored. Only bits [7:0] of this field are taken into account to define the transfer length in number of Half words. This limits the maximum amount of data transferred depending on the operation type. For Read operations the maximum amount of data is (255 - 2) = 253 half-words (506 bytes). For write operations it is (255 -1) = 254 halfwords (508 bytes)

Workaround

The application software needs to limit the data size for Write and Read operation in message (DMA) mode of DDR transfer to a maximum of 506 bytes for reads, and 508 bytes for writes.

ERR051186: I3C: Extended data will be lost when sent after timestamp in async mode 0 in I3C target mode

Description

When the I3C module is in target mode, and async mode 0 (TIMECTRL bits in SSTATUS register) and EXTDATA (EXTDATA bit in SCTRL register) are both set, the data transmission appears to end after the async mode 0 timestamp, but it will continue on.

The T bit will go to 0 after the 3rd item (timestamp) while it should stay 1/High-Z . The I3C module will continue emitting the extended data, however the I3C controller considers that the transmission is done after T bit goes to zero, so the IBI extended data will be lost.

Workaround

Do not use EXTDATA (data past the MDB) and enable async mode 0 at the same time.

ERR051120: I3C: The Not Acknowledge Error bit in the Master Errors and Warnings register (MERRWARN[NACK]) is not set when slave does not acknowledge High Data Rate - Double Data Rate (HDR-DDR) read.

Description

I3C: The Master Errors and Warnings register (MERRWARN) is used to debug I3C/I2C errors and warnings in Master mode. The MERRWARN[NACK] bit does not set when slave does not accept read while HDR-DDR mode is used. This bit is set to 1 in Single Data Rate (SDR) mode when slave does not acknowledge.

Workaround

If a slave does not accept HDR-DDR read and master side is not able to debug, the slave availability/readiness can be checked by sending SDR read request. The MERRWARN[NACK] will reflect the slave response.

ERR009156: LDB: OpenLDI 18-bit SPWG mode does not work correctly

Description

When the device is configured to work in 18 bit SPWG Mode, the LVDS Display Bridge (LDB) incorrectly selects the least significant 18 bits of the output bus rather than the 6 most significant bits from each color component.

Workaround

Configure the Module in 24 bit JEIDA mode and do not use the last line (TX3) from the OpenLDI module. By doing this the module behaves exactly as required in SPWG 18-bit mode.

ERR051608: LPSPI: PRESCALE bits in TCR Register has limitation

Description

LPSPI TCR[PRESCALE] can only be configured to be 0 or 1, other values are not valid and will cause LPSPI to not work.

All 8 LPSPI instances are the same.

Workaround

Driver can use CCR1 register to divide SCK, whose biggest div rate is 512. Software workaround integrated in Linux BSP codebase starting in release imx_5.15

ERR051588: LPSPI:Reset transmit FIFO after FIFO underrun by LPSPI Slave.

Description

Transmit FIFO pointers are corrupted when a transmit FIFO underrun occurs (SR[TEF]) in slave mode.

Workaround

When clearing the transmit error flag (SR[TEF] = 0b1) following a transmit FIFO underrun, reset the transmit FIFO (CR[RTF] = 0b1) before writing any new data to the transmit FIFO.

ERR051421: SAI: Synchronous mode with bypass is not supported

Description

The SAI does not receive or transmit when:

Scenario 1. The transmitter is configured for synchronous mode (TCR2[SYNC] = 0b1), in the Transmit Configuration 2 register, and the receiver is in bypass (RCR2[BYP]=0b1), in the Receiver Configuration 2 register, then there will not be a bit clock as it is the source of the BCLK.

Scenario 2. The receiver is configured for synchronous mode (RCR2[SYNC] = 0b1) in the Receiver Configuration 2 register and the transmitter is in bypass (TCR2[BYP]=0b1), in the Transmit Configuration 2 register, then there will not be a bit clock as it is the source of the BCLK.

Workaround

If scenario 1, then set the TCR2[BCI] = 0b1, in the Transmit Configuration 2 register.

If scenario 2, then set the RCR2[BCI] = 0b1, in the Receiver Configuration 2 register.

ERR051709: TRDC: OSC24M cannot be the clock reference selected accessing MEDIAMIX TRDC DAC

Description

When programming the Media Subsystem’s TRDC components, OSC24M cannot be the clock reference selected for "media_axi_clk_root" or "media_apb_clk_root" during TRDC parameter programming, which will introduce unpredictable results.

Workaround

"media_axi_clk_root" or "media_apb_clk_root" should be sourced from "sys_pll_pfd1" and "sys_pll_pfd1_div2" respectfully.

ERR051725: USB: With the USB controller configured as device mode, Clearing the RS bit of USBCMD register fails to cause USB device to be detached

Description

1. USB controller working as high speed device mode with USB gadget function enabled

2. Cable plugged into USB host

3. Use case is software-controlled detach from USB device side

The expected result is device side terminations removed, increase in USB signal amplitude, USB host detect device is detached. But the issue is that the clear RS bit of USBCMD register cannot cause device detach event.

Workaround

Use the below steps to detach from the host:

write CTRL2[7:6] = 01b

write USBCMD.RS = 0b

write CTRL2[8] = 1b

As CTRL2[8] is set at detach case, so attach the steps should add clear CTRL2[8]:

write CTRL2[8] = 0b

write USBCMD.RS = 1b

ERR052021: uSDHC: Sometimes uSDHC does not work under VDD_SOC low drive mode and nominal mode

Description

uSDHC PADs have an integration issue.

When the direction of CMD/DATA lines changes from output to input, the uSDHC controller begins sampling, the integration issue makes input enable signal from uSDHC propagated to the PAD with a long delay. Thus the new input value on the pad comes to uSDHC lately. The uSDHC samples the old input value and the sampling result is wrong.

Workaround

Set uSDHC CMD/DATA PADs iomux register SION bit to 1, then PADs will propagate input to uSDHC with no delay, so correct value is sampled.

Linux BSP patch has been integrated into release.

ERR052198: uSDHC: eMMC CQE may timeout due to a HW logic issue

Description

To facilitate command queuing in eMMC, uSDHC supports CQE (Command Queue) so that the host can queue data transfer tasks. In some cases where the CQDPT (Device Pending Task) bit is being set and cleared at

the same time, the CQDPT bit is not cleared even after the task has completed execution, resulting in a CQE timeout.

Workaround

There are two possible workarounds:

1.Disable CQE feature using CQCFG register

2. Before sending a DCMD (Direct Command) request, SW must manually clear the CQDPT[bit n] by setting CQTCLR[bit n] if DPT[bit n] != CQTDBR[bit n], in order to clear the pending task.

ERR052357: uSDHC: Low probability get stale data during read transfer.

Description

During read transfer, uSDHC assert interrupt will not wait bus response. So it is possible that part of data has not been fully written to DDR memory, which may result in part of data in memory not correct.

This is impacted by hardware/software latency. If latency is enough, there will no such issue.

Workaround

In Linux OS, since software latency is enough, this issue will not be observed, no need extra workaround.

In real time OS, extra delay time should be added to avoid this issue. So in u-boot, 10μs delay is added for uSDHC read transfer since Linux 6.6.36_2.1.0.

ERR051302: WDOG: Reset delay does not work

Description

The WDOG reset delay does not work in either warm reset or cold reset (WDOG_ANY pin), this gives no time to WDOG interrupt for execution.

Workaround

Board level reset (cold reset) should guarantee delay time after WDOG_ANY pin assert.

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