

Errata for the WCT-15W1CFFPD

This document details all known errata for the WCT-15W1CFFPD. This table provides a revision history for this document.

Table 1. Document revision history

Rev. number	Date	Substantive change(s)
0	05/09/2019	Initial release.

Description:

The U7 and U8 power stages are not the same chip with the SCH MP86901D.

Workaround:

The function and performance is similar, so you can use the demo board to evaluate all features of the WCT-15W1CFFPD.

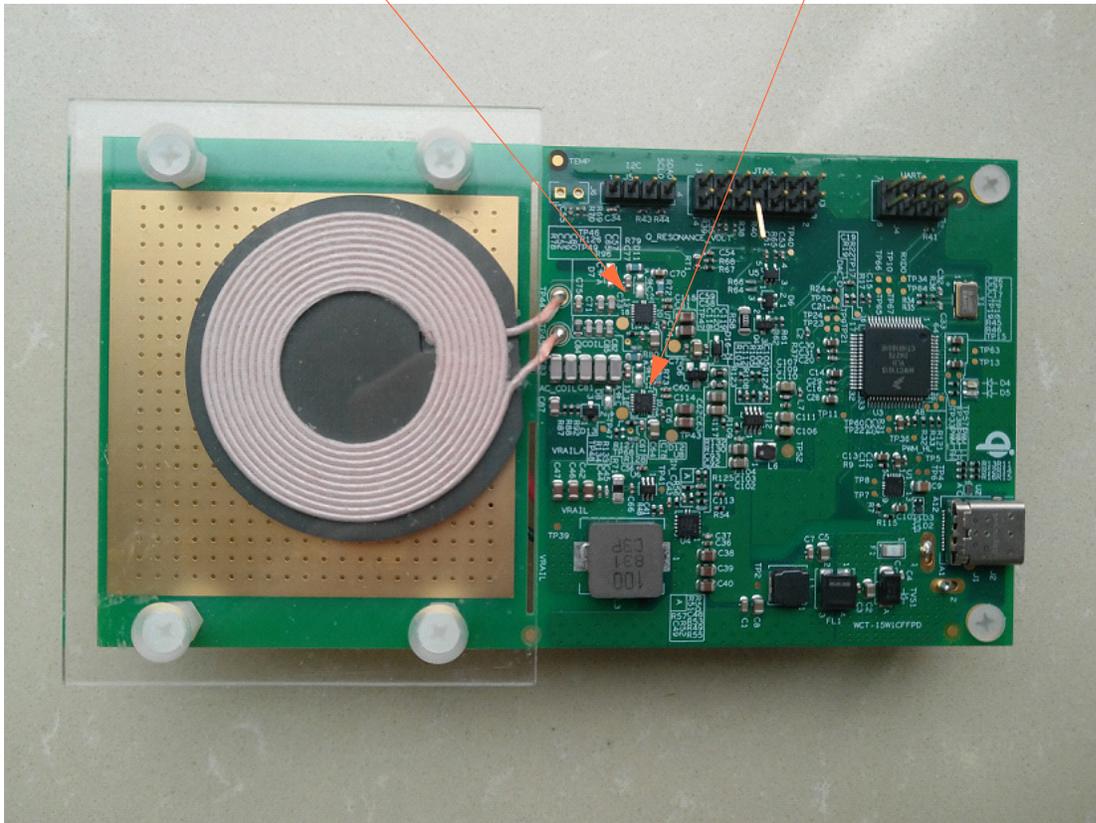
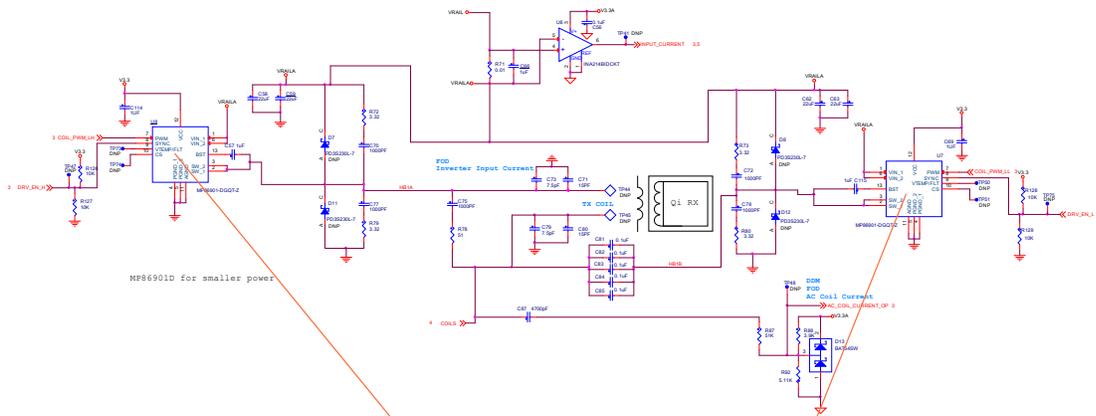


Figure 1.

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Document Number: WCT15W1CFFPDCE

Rev. 0

05/2019