ES_QN9090

Errata for QN9090 QN9090T QN9030 QN9030T

Rev. 3.0 — 24 December 2024 Errata

1 Errata for QN9090 QN9090T QN9030 QN9030T

This report applies to the product list of QN9090, QN9090T, QN9030 and QN9030T which have the following marking information of Line C: s * D *** 2

- s: diffusion center global foundry
- AP: assembly plant, X (ASEN manufacturing, Suzhou), S (NXP manufacturing Kaohsiung, Taiwan)
- D: RoHs Dark Green chemical content of molding
- ***: YWW, assembly data code in year and week
- 2: die version

Errata ID	Errata Title
SE300	JTAG: IDE loses communication with device
SE301	UART: Cannot detect error on second stop when 2 stop configuration is used
SE302	AES crypto possible corruption using USART/SPI/ADC DMA mode consecutively
SE303	ADC precision will degrade when using synchronous clock source as functional clock

SE300: **JTAG: IDE loses communication with device**

Errata type: Errata

Description: MCUXpresso debug cannot be used for applications with the watchdog enabled. During the debug session, the watchdog fires cause the IDE to lose connection, which prevents further debug in the session.

Workaround: Disable the watchdog during debug sessions.

SE301: UART: Cannot detect error on second stop when 2 stop configuration is used

Errata type: Errata

Description: When UART is configured to use 2 Stop bit protocol, the device does not detect error on second stop bit.

Workaround: No workaround is available. It is recommended not to use 2 stop bit protocol.

SE302: **AES crypto possible corruption using USART/SPI/ADC DMA mode consecutively**

Errata type: Errata

Description: The hardware AES crypto engine may not be safely executed while DMA write operations are performed by USART0/1, SPI0/1 and ADC. This is because the AES corruption happens under special data sequence on AHB port 7 when AES access is followed consecutively with a DMA write access to USART, SPI and ADC.

Workaround: The application software should avoid using hardware AES when write operation is required for USART/SPI/ADC DMA mode. The customer can use software AES encryption/decryption when USART/SPI/

ADC DMA write operation is needed. NXP provides suggestions (from SDK 2.6.6 or later) on how to switch between hardware and software AES dynamically depending on the USART/SPI/ADC DMA usage.

SE303: **ADC precision will degrade when using synchronous clock source as functional clock**

Errata type: Errata

Description: In user manual chapter 27.6.5 Optional Operating Modes for ADC, it mentions that “Two clocking modes are available, synchronous mode and asynchronous mode. The synchronous clocking mode uses the system clock in conjunction with an internal programmable divider. The main advantage of this mode is determinism”. But this statement is not correct, and it is inconsistent with the description for the ASYNMODE filed in ADC Control Register, under user manual chapter 17.1 ADC register, where it says “Synchronous mode is Not Supported”. In fact, QN9090,QN9090T,QN9030 and QN9030T don’t support ADC synchronous mode because ADC precision will degrade due to the synchronous clock source.

Workaround: User should configure the ADC to use asynchronous clock source as functional clock.

2 Revision History

Table 1. Revision History

Document ID	Release Date	Description
ES_QN9090 v3.0	24 December 2024	Add SE303 and revision history, update legal information

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