PFR4200MAE40, Mask 1L60X

Introduction

This errata sheet applies to the following devices:

- PFR4200MAE40

MCU Device Mask Set Identification

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 1K79X. All standard devices are marked with a mask set number and a date code.

MCU Device Date Codes

Device markings indicate the week of manufacture and the mask set used. The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code "0201" indicates the first week of the year 2002.

MCU Device Part Number Prefixes

Some MCU samples and devices are marked with an SC, PC, or XC prefix. An SC prefix denotes special/custom device. A PC prefix indicates a prototype device which has undergone basic testing only. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC or SC prefix.

Errata System Tracking Numbers

MUCtsXXXXX is the tracking number for device errata. It can be used with the mask set and date code to identify a specific erratum.

Errata Summary

Errata Number	Module affected	Brief Description	Work-around
MUCts01871	pim_mfr4200	Low-Voltage and Power-On Status bits are never set in the VREGSR.	NO
MUCts02145	flexray	ARL and AYTG bits of MCR1 register have read-only access.(FPR97_98)	NO
MUCts02155	flexray	ISR0.TXIF is not constantly updated. (MPR41)	NO
MUCts02157	flexray	A non-sync frame ID1 is not always transmitted at rate 2.5Mbit/s.(MPR39)	YES
MUCts02158	flexray	No symbol transmission with SSAPOR set to 0x0002. (MPR35)	YES
MUCts02159	flexray	Incorrect byte ordering of data fields in the buffer layout. (FPR39)	YES
MUCts02160	flexray	Reintegrating CC partly sends null frames in the normal mode. (MPR7)	YES
MUCts02161	flexray	CC does not enter one state if one channel is never idle. (FPR100)	NO
MUCts02162	flexray	CC does not reset Symbol Window Status Register bits. (FPR103)	NO
MUCts02163	flexray	CC transmits no WUS's with 1 bit period of the WUS idle-time. (FPR106)	YES
MUCts02164	flexray	CC indicates no SERR for one additional byte at the frame end. (FPR78)	NO
MUCts02165	flexray	CC changes its PSR state in even cycles. (FPR91)	NO
MUCts02166	flexray	CC does not set the PLFIF bit in the SISR. (FPR99)	NO
MUCts02167	flexray	A CHI error is indicated if the NMVector is longer than 4 bytes.(FPR104)	YES
MUCts02168	flexray	Frames exceeding slot boundaries are not signaled correctly. (FPR32)	NO
MUCts02169	flexray	The content of a locked static/dynamic receive buffer changes. (FPR81)	YES
MUCts02170	flexray	External offset correction value is not applied. (FPR92)	YES
MUCts02171	flexray	DATUPD bit is not reset in the normal passive operation state. (FPR102)	YES
MUCts02172	flexray	No startup with pdTSSReceiver > 16 bit. (FPR105)	YES
MUCts02173	flexray	CC does not perform majority voting correctly. (FPR51)	NO
MUCts02174	flexray	First startup frame on channel B not correctly received. (FPR73)	YES
MUCts02175	flexray	CC does not transmit dynamic frames in a large dynamic segment. (FPR89)	NO
MUCts02176	flexray	Large ext offset/rate correction values lead to 3 startup trials.(FPR93)	YES
MUCts02177	flexray	SSAPOR has limited range. (MPR10)	NO
MUCts02178	flexray	CC does not generate debug strobe signals correctly. (MPR2)	NO

s02179	flexray	Startup problems caused by certain length of TSS. (MPR4)	YES
MUCts02180	flexray	Startup problem with configured symbol window of 1 MT. (MPR9)	YES
MUCts02181	flexray	CC generates too long minislots if MSLR is bigger than 32 MT. (MPR27)	YES
MUCts02182	flexray	Late SYNC frame during initialize_schedule not tolerated. (MPR25)	YES
MUCts02183	flexray	2-star cluster topology does not work with minislot duration=2MT. (MP28)	YES
MUCts02184	flexray	Latest dynamic transmission start must be less than 8192 MT. (MPR30)	NO
MUCts02185	flexray	Glitches are not tolerated. (MPR31)	NO
MUCts02186	flexray	Incorrect Sync Frame IDs displayed in (O/E)SFIDnR	YES
MUCts02870	flexray	Usage of bit 7 of the ATBCCPLR causes CRC errors in dynamic frames	YES

Low-Voltage and Power-On Status bits are never set in the VREGSR. MUCts01871

Description

The Low-Voltage and Power-On Status bits in the Voltage Regulator Status Register (VREGSR) are always '0' regardless of the reset initiator.

Workaround

Not available.

ARL and AYTG bits of MCR1 register have read-only access.(FPR97_98) MUCts02145

Description

The CC has read-only access to the ARL and AYTG bits of the MCR1 register instead of read/write as it was intended and described in the MFR4200 Block Guide.

Therefore they are always 0's which means that the protocol error handling level red is prohibited and the MFR4200 cannot enter the green state from the yellow one.

Workaround

Not available.

ISR0.TXIF is not constantly updated. (MPR41) MUCts02155

Description

The chapter 4.2.6.6 of the Block Guide states: TXIF - This read-only bit will be set when any of the enable (IENAn = 1) transmit message buffers is empty (IFLG = 1). But, when at a given time, two transmit buffers are empty, after reading one of the buffers - using lock/unlock - TXIF bit is low for a certain time although one IFLG is still set. Therefore, the ISR0.TXIF is not a constantly updated by the MFR4200.

Workaround

Not available.

A non-sync frame ID1 is not always transmitted at rate 2.5Mbit/s.(MPR39) MUCts02157

Description

A cluster configuration is following: communication cycle = 16ms, baudrate = 2.5Mbit/s. Node A is a following coldstart node, MFR4200 is a leading coldstart node, MFR4200 is configured to transmit the static non-sync frame in the first static slot (ID1), the sync frame in the last static slot (ID898) and one dynamic frame at the end of the dynamic segment. The network idle time is configured to least possible size. NITCR is configured to least valid size. *****Expected behaviour: the MFR4200 transmits the static non-sync frame (ID1), the sync frame (ID898) and the dynamic frame successfully and receives all frames transmitted by the Node A. *****Observed behaviour:

the MFR4200 transmits the sync frame, thus the startup is successful. Also the dynamic frame is transmitted correctly but no frame is transmitted in Slot ID1. the MFR4200 receives correctly all frames transmitted by the Node A.

Workaround

Changing the slot of the static non-sync frame to slot2 enables the MFR4200 to transmit all frames correctly. Enlarging the network idle time by 1MT enables the MFR4200 to transmit all frames correctly.

No symbol transmission with SSAPOR set to 0x0002. (MPR35) MUCts02158

Description

Cluster configuration: A MFR4200 is a leading coldstart node. It is programmed as following: SSAPOR = 0x0002 (2MT static slot action point offset and 2MT symbol window action point offset), MSAPOR = 0x0001 (1MT minislot action point offset), MSLR = 0x0003 (3MT minislot length), SWCR = 0x0211 (symbol window start at 529MT), NITCR = 0x021B (network idle time start at 539 MT). Thus the symbol window length is 10MT. ****Expected behaviour: the MFR4200 transmits configured MTS symbols in configured communication cycles on configured channels. *****Observed behaviour: the MFR4200 does not transmit MTS symbols in any cycle. Therefore the MFR4200 does not transmit MTS symbols with SSAPOR = 0x0002 and MSAPOR = 0x0002.

Workaround

The MFR4200 transmits MTS symbols only if SSAPOR = 0x0001.

Incorrect byte ordering of data fields in the buffer layout. (FPR39) MUCts02159

Description

The tables of Receive Message Buffer Layout (Section 5), the Receive FIFO Message Buffer Layout (Section 5), the Transmit Message Buffer Layout (Section 5), and the register table of the Active Transmit Buffer Data n Register (Section 4.2.7.6), the Active Receive Buffer Data n Register (4.2.7.11) and the Active FIFO Buffer Data n Register (4.2.7.16) contain non-ProtoclSpecification-compliant byte ordering of the data elements.

Precisely: the CC transmits the most significant byte of the message transmit buffer before the least significant byte (big endian) on the physical layer. In the block guide, the most significant byte is named as the data1, the least significant byte - the data0. Consequently, the data1 is transmitted before the data0 on the physical layer.

This is not compliant to the Protocol Specification V1.1: in the frame format chapter, the figure 3-1 "FlexRay frame format" shows following transmission order of data bytes: data0, data1, data2, data3 and so on.

Workaround

No workaround is needed when the cluster contains only MFR4200 devices, as receivers of those devices perform the same swapping as the transmitters.

If a cluster containes not only MFR4200 devices then the following workaround is possible in the host software:

- Data0 should be treated as the most significant byte of the first data word.
- Data1 should be treated as the least significant byte of the first data word.
- similar for second data word (Data2 and Data3), and so on.

The same procedure should be applied to the message ID and the Network management vector fields.

Reintegrating CC partly sends null frames in the normal mode. (MPR7) MUCts02160

Description

In the configuration without symbol window configured the following behavior is observed. The coldstart CC after the reintegration procedure does not send a valid first frame during its first communication cycle in the normal active state. This CC send a null frame instead. At the same time this CC does not store valid frames received from other nodes and, therefore, does not update DATUP bits in its appropriate receive message buffers. It sends valid (non-null) frames in subsequent communication cycles and receives frames from other nodes. This issue does not occur in the configurations with the symbol window of 2MT configured.

Workaround

The problem does not occur with the symbol window of 2MT configured.

CC does not enter one state if one channel is never idle. (FPR100)

MUCts02161

Description

The controller starts the startup procedure in the listen_coldstart state. Due to noise the controller enters the coldstart_collision_resolution state after the listen timeout with noise (tStartupNoise) whereas both channels has to be idle at this time. If one channel is never idle the controller stays in the coldstart_listen state and does not start to send its CAS symbols and its startup frames. This is not compliant to the Protocol Specification v1.1 because at least one channel has to be idle at this time (see Protocol Specification V1.1 figure "Transitions from the coldstart_listen state.": tStartupNoise event, whereas zChannelIdle(A) OR zChannelIdle(B) has to be true).

Workaround

Not available.

CC does not reset Symbol Window Status Register bits. (FPR103)

MUCts02162

Description

In the normal active state, the CC does not reset the SYMB, CH and VCE bits in SWSAR and SWSBR status registers when no symbol is received during the symbol window.

Workaround

Not available.

CC transmits no WUS’s with 1 bit period of the WUS idle-time. (FPR106) MUCts02163

Description

The CC is a leading coldstart node and performs a wakeup with the following configuration: WMCTRLR = 0x0042 (send 2 wakeup-symbol (WUS) on channel B), WUSTXLR = 0x003F (WUS low-phase is maximum (63 bits)) and WUSTXIR = 0x0001 (WUS idle-phase is minimum (1 bit)).

It is expected that the CC will perform wakeup by sending 2 WUS with 63 bits of logic 0 level and 1 bit of logic 1 level each. Instead of this the CC performs wakeup by sending 2 WUS with 63 bits of logic 0 level and 257 bits of logic 1 level each.

Workaround

The WUS idle-phase must be configured in the WUSTXIR to at least 2 bits.

CC indicates no SERR for one additional byte at the frame end. (FPR78) MUCts02164

Description

If the CC receives a frame with an erroneous additional byte at the frame end (without that byte the frame is semantically valid and syntactically correct), the CC does not discard it and stores it in a configured receive message buffer or in the configured FIFO. The CC does not set the SERR bit in the MBSS register of the receive message buffer or the FIFO.

Workaround

Not available.

CC changes its PSR state in even cycles. (FPR91) MUCts02165

Description

In case of a large external clock correction values (please see ECCR, EOCR and ERCR registers in the MFR4200 BG), the CC may change the protocol state to the normal_passive not only at the end of an odd but also at the end of an even communication cycle.

Workaround

Not available.

CC does not set the PLFIF bit in the SISR. (FPR99) MUCts02166

Description

The CC never set the PLFIF bit in the SISR register during startup procedure while the consistency check of the CC within the startup sequence has failed.

Workaround

Not available.

A CHI error is indicated if the NMVector is longer than 4 bytes.(FPR104) MUCts02167

Description

The CC indicates the CHI error in the CHIER register NMEFTS bit (network management error, frame too short) when NMVLR register value > 0x0004. However, the CC correctly generates the global network management vector (please see GNMVnR) using all network management vector bytes from received frames.

Workaround

To avoid the CHI error in the CHIER register NMEFTS bit (network management error, frame too short), the NMVLR register value should be NMVLR <= 0x0004.

Frames exceeding slot boundaries are not signaled correctly. (FPR32) MUCts02168

Description

The message buffer slot status vector of the last static slot in the static segment does not indicate a boundary violation correctly. Frames exceeding the last static slots boundary are received as if they were correct (no Boundary Violation in the BVIOL bit indicated, while the VCE bit is set to 1, which means that a valid communication element has been received). Please see ARBMBSSVR.

Workaround

Not available.

The content of a locked static/dynamic receive buffer changes. (FPR81) MUCts02169

Description

The CC does not show the old content of a receive buffer which has been locked before the upcoming message was received for that buffer.

The problem occurs only if the receive buffer is locked within a time frame of 15 microticks after the slot boundary from slot n (containing the received frame) to slot n+1.

Workaround

The following workarounds are available:

- don't lock a receive buffer within 15 microticks after the slot boundary.
- check IFLG before locking the buffer.
- use IFLG to trigger an interrupt when a frame has been received.

External offset correction value is not applied. (FPR92) MUCts02170

Description

If the Host sets the EOCE bit (ECCR register) in an even communication cycle, then the CC calculates the offset correction value in the even communication cycle and clears this bit also in the even communication cycle. In the subsequent odd communication cycle, there is no external offset correction value (because EOCE is already cleared). Consequently the external offset correction is not applied in the odd communication cycle as it is specified in the Protocol Specification v1.1.

Workaround

The Host must explicitly set the EOCE bit in an odd cycle so that CC applies the external offset correction value at the end of the odd cycle.

DATUPD bit is not reset in the normal passive operation state. (FPR102) MUCts02171

Description

The CC does not update the DATUPD bit in the BUFCSnR register of receive message buffers in the normal_passive_operation state.

Workaround

Data update must be checked by the host application based on the receive message buffer content.

No startup with pdTSSReceiver > 16 bit. (FPR105) MUCts02172

Description

The CC does not perform startup sequence with gdTSSTransmitter = 15bit and pdTSSReceiver > 16bit. Please see the TSSLR register.

Workaround

The pdTSSReceiver shall not exceed 16bits.

CC does not perform majority voting correctly. (FPR51) MUCts02173

Description

PS 1.1 chapter 3.3.1.2 "Bit clock alignment and bit strobing" states:

The current value of Voted_RxD at the strobe offset is taken as the current bit value.

The voting window consists of 5 samples, beginning with the first sample of the bit. Therefore a "0" bit with the following samples should not be voted as "0": 0111 0111 - this should be "1".

The observed behavior is, that the CC does not report a syntax error for a frame with this pattern of samples.

Further investigations show:

The sample pattern "1111 0111" is taken as a valid "0" bit. The sample pattern "0000 1000" is taken as a valid "1" bit. Both sample patterns should be not valid, because 4 of the 5 samples in the voting window are wrong.

Therefore, the value of a bit is taken directly from the RxD and not from the Voted_RxD.

Workaround

Not available.

First startup frame on channel B not correctly received. (FPR73) MUCts02174

Description

The CC is configured as a coldstart node. The TSS is set to 8 bits for transmission and reception (Transmit Start Sequence Length Register, TSSLR=0x0808). During the startup, with the first startup frame reception, the CC sets the channel status error counter of channel B to 1 and performs transition to normal operation as expected. The CC increments the channel status error counter of channel B because the first startup frame on channel B, which was send by the another node, was received with a syntax error. If the TSS for reception is configured to 9 bits (TSSLR = 0x0908) then there is no syntax error on channel B.

Workaround

The TSS value should be one bit bigger for reception than for transmission. Please see TSSLR register.

CC does not transmit dynamic frames in a large dynamic segment. (FPR89) MUCts02175

Description

The CC configuration is the following: number of static slots = 2, static slot length = 30 us, dynamic slot length = 2 us, cycle length = 8.3 ms. Dynamic part = 8.157 ms but with the given 11 bit identifier (frame ID = [1:2047])and the configured static part only 2045 of dynamic slots can be used for communication. Buffer configuration: 3 frames are configured for transmission with frame ID 1, 1023 and 2047, 3 another frames are configured for reception with frame ID 2, 1022 and 2046. The CC in the normal_active state does not transmit frames in the dynamic part (with ID = 1023 and 2047).

Workaround

Not available.

Large ext offset/rate correction values lead to 3 startup trials.(FPR93) MUCts02176

Description

The CC is configured as a leading coldstart node. The Host sets the EOCE bit and the ERCE bits once in order to apply external offset and rate correction values in the startup phase (even cycle of coldstart consistency check state).

Expected CC behavior: 1st startup - both, the external offset and external rate correction values are applied in the odd cycle of coldstart consistency check state. The CC sets zClockState to LIMIT_REACHED due to large correction values and makes the state transition to coldstart listen. 2nd startup - after the timeout, the CC starts up again without an error into normal_active state.

Observed behavior: 1st startup - only the external offset correction value is applied in the even communication cycle of coldstart consistency check state. The CC sets zClockState to LIMIT_REACHED due to large offset correction value and makes the state transition to coldstart listen. 2nd startup - after the timeout, the CC starts up again into coldstart consistency check state. Only the rate correction value is applied in the odd communication cycle. The CC sets zClockState to LIMIT_REACHED due to large offset correction value and makes the state transition to coldstart listen. 3rd startup - after the timeout, the CC starts up again without an error into normal_active. The CC performs the additional startup attempt due to the problem reported in the MUCts01616 (External offset correction value is not applied).

Workaround

Please see the workaround for the MUCts01616 (External offset correction value is not applied).

SSAPOR has limited range. (MPR10) MUCts02177

Description

Known constraint: the CC SSAPOR register has the range [1-15] MT while according to the Protocol Specification v1.1, chapter B.2.1 "Communication Controller", the range of gdActionPointOffset (action point in the static slot) is [1-31] MT.

Workaround

Not available.

CC does not generate debug strobe signals correctly. MUCts02178

2)

Description

If a debug strobe pin is configured for "slot start in static segment" (BG p.52 Table 4-48), the signal "slot start in static segment" is correctly generated within the static segment, however, wihtin the other segments instead of this signal the default signal of the debug strobe pin (BGT or ARM_BG) is generated. Similarly, if the debug strobe pins are configured for "dynamic slot start on channel A" and "dynamic slot start on channel B", these signals are produced correctly within the dynamic segment, however, within other segments instead of these signals the default signals of the debug strobe pins (BGT and ARM_BG) are generated.

Workaround

Not available.

Startup problems caused by certain length of TSS. (MPR4) MUCts02179

Description

The CC does not always startup with only one channel (A or B) configured due to the problem reported in the MUCts01620 (First startup frame on channel B not correctly received).

Workaround

Please see the workaround reported in the MUCts01620 (First startup frame on channel B not correctly received).

Startup problem with configured symbol window of 1 MT. MUCts02180

9)

Description

After leaving the configuration state, the nodes do not startup to the normal_active state, but reach and remain in the intermediate states (coldstart_consistency_check or integration_coldstart_check states for the startup nodes, integration_consistency_check state for non-startup nodes) under the following conditions: they are configured with pure static segment (no dynamic segment) and a symbol window of 1 MT.

Workaround

Workarounds:

- use a mixed configuration (static and dynamic segment).

- use a pure static configuration (no dynamic segment) without a symbol window configured, or with a symbol window of at least 2MT i.e do not configure a symbol window of 1 MT in a pure static configuration.

CC generates too long minislots if MSLR is bigger than 32 MT. (MPR27)

MUCts02181

Description

Minislots have correct sizes for MSLR values in range from 2MT to 32MT (please see MFR4200 BG section 4.2.3.12 Minislot Length Register (MSLR)). If any bigger slots are configured in the MSLR, the controller generates minislots according to the formula: MSLR value (MT) + 192MT.

Workaround

Use minislots with the length from 2 MT up to 32 MT.

Late SYNC frame during initialize_schedule not

MUCts02182

Description

There is a running network with two nodes transmitting frame ID 0x01 (Node1) and frame ID 0x29 (Node2) on both channels. The CC tries to integrate into the network. The network has the following characteristics: Macrotick length = 1us, Static slot length = 30us, Message length = 6words => 21.1 us, MOCR = 0x0016, MRCR = 0x0016, SSAPOR = 0x0001. As soon as the CC is in the initialize_schedule the Node1 transmits a sync message with frame ID 0x01 5 bit times later than nominal. Expected behavior: The CC continues integration (i. e. initialize_schedule -> integration_consistency_check -> normal_active operation) because 5 bit times < pdAcceptedStartupRange. Observed behavior: the CC remains in the initialize_schedule_state and executes the transition to the integration_consistency_check. Then the CC falls back into the integration_listen state. The same behavior has been observed with 10 and 35 bit times. ***** 1. MOCR and SSAPOR adapted to 5 bit times: MOCR = 0x0050, MRCR = 0x012C, SSAPOR = 0x0002. The Node1 sends a sync message 5 bit times late => during the integration_consistency_check state the CC performs a successful offset correction. The CC continues integration. ***** 2. MOCR and SSAPOR adapted to 10 bit times: MOCR = 0x00A0, MRCR = 0x012C, SSAPOR = 0x0004. The Node1 sends a sync message 10 bit times late => during the integration_consistency_check state the CC performs a successful offset correction. The CC continues integration. ***** 3. MOCR and SSAPOR adapted to 20 bit times: MOCR = 0x0140, MRCR = 0x012C, SSAPOR = 0x0008. The Node1 sends a sync message 20 bit times late => the CC falls back into the integration_listen state.

Workaround

Adapt the MOCR, MRCR register values to allow larger corrections and the SSAPOR register value to allow larger window.

2-star cluster topology does not work with minislot duration=2MT. (MP28) MUCts02183

Description

Cluster topologies with 2 stars do not operate with a minislot duration of 2 MT: the cluster starts up correctly, the communication in the static segment works correctly, the communication in the dynamic segment is erroneous, approximately one third of the dynamic frames is lost, some dynamic frames are received with a syntax error indication some with a content error indication. The end-to-end communication works correctly for a minislot duration of 3 MT up to 32 MT (see MUCts01729) for the 2-star topology. The configured TSS length for receiver and transmitter is 9 and 8 bit cells, respectively (TSSLR = 0x0908).

Workaround

For the 2-star topology, the minislot must be configured to value >= 3MT or the dynamic segment must not be used.

Latest dynamic transmission start must be less than 8192 MT. (MPR30) MUCts02184

Description

The Protocol Specification V1.1 configures LDTS (latest dynamic transmission start) in minislots and allows a range of 1 to7990 minislots. In the MFR4200, the LDTSR, which is expressed in MT, may only be set to a maximum value of 8191 MT. If bigger LDTSR values are specified the controller does not send dynamic frames at all.

Workaround

Not available.

Glitches are not tolerated. (MPR31) MUCts02185

Description

If a network is configured to 10Mbps bitrate and glitches hit transmitted 0 bits surrounded by 1's then the MFR4200 does not tolerate all of these glitches during reception. The glitch position in the 0-bit is represented by the '1' in the glitch pattern: glitch length 12.5 ns: 0100 0000 or 0010 0000 or ... or 0000 0010 (6 positions); glitch length 25 ns: 0110 000 or 0011 0000 or ... or 0000 0110 (5 positions); glitch length 37.5 ns: 0111 0000 or 0011 1000 or ... or 0000 1110 (4 positions); glitch length 50 ns: 0111 1000 or 0011 1100 or ... or 0001 1110 (3 positions). ***** Expected behavior: the number of syntax errors depends on the glitch length. The number of syntax errors does NOT depend on the glitch position. The MFR4200 receives messages with glitches: glitch length = 12.5 ns => Ok; glitch length = 25 ns => Ok; glitch length = 37.5 ns => 5000/10000 syntax errors; glitch length = 50 ns => 10000/10000 syntax errors. ***** Observed behavior: the number of syntax errors depends on the glitch length. AND on the glitch position. Glitches near the center of the 0-bit show typical values. Glitches near the edges of the 0-bit lead to 0 - 15/10000 syntax errors. The MFR4200 receives messages with ID 0x05: glitch length = 12.5 ns, near center => 3/10000 syntax errors; glitch length = 25 ns, near center => 8/10000 syntax errors; glitch length = 37.5 ns, near center => 9834/10000 syntax errors; glitch length = 50 ns, near center => 10000/10000 syntax errors.

Workaround

Not available.

Incorrect Sync Frame IDs displayed in (O/E)SFIDnR MUCts02186

Description

The Sync Frame ID Registers (OSFIDnR, ESFIDnR) show incorrect IDs: the nodes owns sync frame can be read by the host as frameID*2, other nodes sync frames are stored as: frameID*2+1.

Workaround

The host software should process the frams IDs stored in the Sync Frame ID Registers (OSFIDnR, ESFIDnR) accordingly.

Usage of bit 7 of the ATBCCPLR causes CRC errors in dynamic frames MUCts02870

Description

Setting of bit7 in ATBCCPLR registers causes the Frame CRC errors when using dynamic frames. This specific bit is defined as RESERVED within the MFR4200 Block Guide. When setting it to zero the error does not appear. When using static frames, setting of bit7 does not have an impact on functionality.

Workaround

Do not set bit 7 of ATBCCPLRs to 1 for dynamic frames.