Mask Set Errata for Mask 0M11J

Introduction

This report applies to mask 0M11J for these products:

- MC9S08QE128

SE184-FLVD-STOP3: False low voltage detect when exiting stop3

Errata type: Silicon

Affected component: SoC level behavior

Description: If the low voltage detect (LVD) is enabled (LVDE = 1) but not in stop mode (LVDSE = 0), on some devices the low voltage detect flag (LVDF) will occasionally be set when exiting stop3 mode. If the LVD interrupt is enabled (LVDIE = 1) the interrupt vector will be fetched. If the LVD reset is enabled, the part will reset, and the LVD bit in the System Reset Status (SRS) register will be set. The correct operation of the device is to wake and execute the code immediately after the STOP instruction.

If the LVD is not enabled (LVDE = 0) or if LVD is also enabled during stop mode (LVDSE = 1) then this issue will not occur. If the LVD is enabled during stop mode the stop3 current will increase.

Workaround: A software level change to reliably eliminate the issue is to use only the LVD interrupt (LVDE = 1, LVDIE = 1, and LVDRE = 0). Inside the LVD interrupt service routine, a short state of health check can be made to verify the supply level before proceeding. In this routine, the LVDF should be cleared and then read to determine whether a true low voltage event is present. If the LVDF is set when it is read, then a true LVD condition exists and the MCU can be reset by forcing the execution of an illegal op-code.

SE157-ADC-INCORRECT-DATA: Boundary case may result in incorrect data being read in 10- and 12-bit modes

Errata type: Silicon

Affected component: ADC

Description: In normal 10-bit or 12-bit operation of the ADC, the coherency mechanism will freeze the conversion data such that when the high byte of data is read, the low byte of data is frozen, ensuring that the high and low bytes represent result data from the same conversion.

In the errata case, there is a single-cylce (bus clock) window per conversion cycle when a high byte may be read on the same cycle that subsequent a conversion is completing. Although extremely rare due to the precise timing required, in this case, it is possible that the data transfer occurs, and the low byte read may be from the most recently completed conversion.

In systems where the ADC is running off the bus clock, and the data is read immediately upon completion of the conversion, the errata will not occur. Also, in single conversion mode, if the data is read prior to starting a new conversion, then the errata will not occur.

The errata does not impact 8-bit operation.

Introducing significant delay between the conversion completion and reading the data, while a following conversion is executing/pending, could increase the probability for the errata to occur. Nested interrupts, significant differences between the bus clock and the ADC clock , and not handling the result register reads consecutively, can increase the delay and therefore the probability of the errata occuring.

Workaround: Using the device in 8-bit mode will eliminate the possibility of the errata occuring.

Using the ADC in single conversion mode, and reading the data register prior to initiating a subsequent conversion will eliminate the possibility of the errata occuring.

Minimizing the delay between conversion complete and processing the data can minimize the risk of the errata occuring. Disabling interrupts on higher priority modules and avoiding nested interrupts can reduce possible contentions that may delay the time from completing a conversion and handling the data. Additionally, increasing the bus frequency when running the ADC off the asynchronous clock, may reduce the delay from conversion complete to handling of the data.

SE156-ADC-COCO: COCO bit may not get cleared when ADCSC1 is written to

Errata type: Silicon

Affected component: ADC

Description: If an ADC conversion is near completion when the ADC Status and Control 1 Register (ADCSC1) is written to (i.e., to change channels), it is possible for the conversion to complete, setting the COCO bit, before the write instruction is fully executed. In this scenario, the write may not clear the COCO bit, and the data in the ADC Result register (ADCR) will be that of the recently completed conversion.

If interrupts are enabled, then the interrupt vector will be taken immediately following the write to the ADCSC1 register.

Workaround: It is recommended when writing to the ADCSC1 to change channels or stop continuous conversion, that you write to the register twice. The first time should be to turn the ADC off and disable interrupts, and the second should be to select the mode/channel and re-enable the interrupts.

SE143-ICS: ICS Internal Reference Can Remain Enabled in Stop3 Mode

Errata type: Silicon

Affected component: ICS

Description: When transitioning from FEI or FBI modes to FEE or FBE modes, the internal reference clock may remain active in stop3 mode if the STOP instruction is executed soon after the IREFST bit in the ICSSC register clears. This can lead to elevated stop3 I_{DD}.

Workaround: To ensure the internal reference clock is disabled before entering stop3, wait three internal reference clock periods after the IREFST bit has cleared before entering stop3. On a device with a trimmed internal reference, one period will be between 25.6 µs and 32 µs, therefore waiting 100 µs is adequate for all trimmed devices.

Or

To ensure the internal reference clock is disabled before entering stop3, transition into FEE mode and wait until the LOCK status bit indicates the FLL has attained lock before entering stop3 or transitioning into FBE mode and entering stop3.

SE138-ICS: Limited ICS Frequency Range When High Range DCO Selected

Errata type: Silicon

Affected component: ICS

Description: In some cases, when the high range DCO is selected, the ICSOUT frequency cannot be trimmed to all frequencies in the specified 48–50.33 MHz range. When the issue occurs, the ICSOUT frequency will default to a higher frequency, typically above the 50.33 MHz maximum for the device. The issue typically occurs when the reference frequency is trimmed for a 48–49 MHz ICSOUT.

Workaround: When a 32768 Hz reference is used, either by trimming the internal reference or using an external clock, this issue has not been observed. Using this frequency as the reference clock allows proper operation of the DCO in high range. The ICSOUT in this case will be 50.33 MHz.

SE133-FLASH: Unexpected Flash Block Protection Errors

Errata type: Silicon

Affected component: Flash

Description: If a portion of the nonvolatile memory (NVM) is block protected, unexpected flash block protect violation (FPVIOL) errors can result. These errors can occur during an attempt to program or erase locations in areas of the NVM that are not block protected. Software methods can be used to avoid this potential problem. The problem is more likely to be seen on devices that have multiple nonvolatile blocks, including devices with two or more separate flash blocks or with flash plus EEPROM. If block protection is not enabled, no errors occur.

This error is related to logic that compares current block protection settings to an internally latched address. This internal address is written (latched) at reset, at the end of most flash commands, and whenever there is a write to a location in NVM. If a read access to the partially protected NVM is performed immediately before the write to unprotected memory that starts a new flash command, the erroneous address that was previously in the internal latch can cause a false indication of a protection violation. A short sequence of instructions can be performed before starting normal flash commands to ensure that the address in the internal latch is not a protected address.

Workaround: The preferred workaround starts a command to a known unprotected address (which internally latches the known-unprotected address), forces an access error to abort that command, and then clears the resulting error flags before starting any new flash command. This workaround assumes the H:X index register points to the location or sector you want to program or erase, and accumulator A has the data value you plan to write to that location. Start your program or erase routine with the following instructions.

```
 STA    ,X     ;latch the unprotected address from H:X
               NOP          ;brief delay to allow the command
 state machine to start
                STA    ,X     ;intentionally cause an access
error to abort this command
                PSHA          ;temporarily save data value
                LDA    #$30   ;1's in PVIOL and ACCERR bit
positions
                STA    FSTAT  ;clear any error flags
                PULA          ;restore data value
                STA    ,X     ;STEP 1 write data to start new
command
```

The only new instructions compared to the normal routine for flash commands are the first three instructions, which take three bytes of code space and five bus cycles. These instructions may be located anywhere in memory, including in the protected area of the flash memory.

SE131-WaitIDD:

Errata type: Silicon

Affected component: SoC

Description: An error in the flash memory access logic results in higher than specified wait currents. At slower CPU frequencies (e.g., 32 kHz), there is little difference between run and wait currents. At higher CPU frequencies (e.g., 25 MHz), wait currents are 70–75% of run currents under the same conditions. Wait currents are expected to be in the range of 30% to 50% of run currents under the same conditions.

Workaround: none

SE120-IIC: Incorrect Clocking in 10-Bit Addressing Mode

Errata type: Silicon

Affected component: IIC

Description: This erratum is relevant only for applications using 10-bit addressing mode and does not affect 7-bit addressing mode operations.

When hexidecimal values E0,E1,E4,E5,E8,E9,EC,ED,F0,F2,F4, or F6 are used as data in master receive slave transmissions from the IIC module using 10-bit addresses, the IIC clock may produce an incorrect number of pulses. This will result in IIC communication errors.

Workaround: Avoid using the values listed in the erratum description as data in any master receive slave transmission from the IIC module while in 10-bit addressing mode.

SE118-RTC: LPO Enabled in Stop Modes When RTC is in Reset State

Errata type: Silicon

Affected component: RTC

Description: The RTC module comes out of reset with the low power oscillator (LPO) as the selected clock source (RTCLKS = 0:0), but with the RTC module itself disabled (RTCPS = 0:0:0:0). This configuration signals the LPO to be enabled in all modes including stop2 and stop3.

This results in higher than expected stop currents due to the LPO stop mode current adder.

Workaround: To disable the LPO when not needed in the stop modes, set the RTCLKS bits in the RTCSC register to any value other than 0:0. This will select an alternative clock source for the RTC, either the external clock (ERCLK) or the internal clock (IRCLK). Unlike the LPO, the RTC module does not automatically enable either of these clocks to run in stop modes. ERCLK or IRCLK enable is determined by other MCU control bits, not the RTC's. Before entering stop mode, one period of the LPO must expire after setting the RTCLKS bits to ensure that the change has been processed.

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