Mask Set Errata for Mask 0M84P

Introduction

This report applies to mask 0M84P for these products:

- MC9S08MP16
- MC9S08MP12

MCU Device Mask Set Identification

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 0J27F. All standard devices are marked with a mask set number and a date code.

MCU Device Date Codes

Device markings indicate the week of manufacture and the mask set used. The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code "0301" indicates the first week of the year 2003.

MCU Device Part Number Prefixes

Some MCU samples and devices are marked with an SC, PC, or XC prefix. An SC prefix denotes special/custom device. A PC prefix indicates a prototype device which has undergone basic testing only. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC or SC prefix.

SE164-HSCMP1-OUTPUT-DELAY: HSCMP1 Output Delay

Errata type:	Silicon
Affected component:	PMC
Description:	The output from HSCMP1 will be delayed much longer than the specification allows (up to 4 ms) if both the COP and the internal 1 kHz clock are disabled.

Workaround: Enable the COP or the 1 kHz internal clock to enable the current reference that drives the HSCMP1 and eliminates the issue.

SE161-FTM: FTM Coherency Issues in MP16 Flextimer Module (FTM)

Errata type: Silicon

Affected component: FTM

Description: The coherency mechanism on the timer was compromised due to a clock integration issue on this device.

Flextimer IP was integrated in MP16 in an unusual way to meet an extended input filter performance requirement. A faster clock (core_clk) was used in place of the originally intended IP design clock, ipg_clk (half core_clk frequency). As a consequence, the signals that go in and out of the IP see/generate non-standard timing, and the higher clock makes IP logic to work faster. Although the interface timing was adapted by integration, one unexpected IP internal window allowed a premature contents change in 16-bit data reads, breaking the data coherency mechanism. Below are the 2 different ways when such bug will manifest.

There are two cases discussed in this errata:

- Cases 1 — 16-bit coherency mechanism of direct counter read is not operational.
- Cases 2 — Read of Input Capture 16-bit register when a capture override occurs.

Workaround:

Case 1: 16-bit coherency mechanism of direct counter read is not operational.

Description

Reading the 16-bit counter will return the free running value instead of the intended 16-bit coherency latch.

A potential issue occurs when there is a transition in the 16-bit while the 2-byte read is in course. In that case, the first byte read will extract data from one 16-bit value and the second byte will extract from the transitioned 16-bit value. This effect is specially seen in High byte transitions.

Example

0x02FF byte H reads 0x02.

0x0300 byte L reads 0x00 => Result is 0x0200, while coherency would read 0x02FF - delta -0xFF

Reading L first (0xFF) then H next (0x03) would result 0x03FF - again far from 0x02FF - delta +0x100

Workaround

This workaround assumes that the application allows enough time to read the H byte twice without transitioning the counter H byte. Ideally, the twice reads of H should occur as close as possible to each other - disabling interrupts between reads is recommended. The twice H byte read speed will define the maximum FTM frequency with respect to bus clock.

1. Read H and L bytes.
2. Read H byte again.
3. If H did not change, then HL bytes of Step 1 are correct.
4. If H changed, then read HL bytes again and done.

Case 2: Read of Input Capture 16-bit register when a capture override occurs.

Description

Reading the 16-bit Input Capture register will return an incorrect value if a new capture occurs between the first and second bytes read.

Example

Example of overriding Input Capture events:

Event Input Capture value: 0xAABB .

Read H byte : 0xAA .

New event occurs Input Capture value updated: 0xEEFF. Read L byte: 0xFF > should have read 0xBB => Result 0xAAFF - with correct coherency should be 0xAABB

Same Input Capture events, now reading L first:

Event Input Capture value: 0xAABB .

Read L byte : 0xBB .

New event occurs Input Capture value updated: 0xEEFF. Read H byte: 0xEE > should have read 0xAA => Result 0xEEBB - with correct coherency should be 0xAABB

Workaround

With the bug, there is no identified procedure that can prevent reading an incorrect second byte from the Input Capture register. However, there is a way to tell if the 16-bit just read is correct or not.

By using the CHnF flag, it is possible to know if a new Input Capture occurred between the first and second bytes read. If flag is set between reads, the 16-bit just read must be discarded. A subsequent register read will return the newly captured value.

1. Clear CHnF flag.
2. Read H or L of Input Capture register.
3. (...) may have unrelated code executed, including interrupts.
4. Read the complementary IC byte.
5. Check CHnF flag.
6. If reset, then HL read from IC reg is correct as it is.
7. If CHnF set, then discard HL and go to Step 1.

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