DEVICE ERRATA

February 27, 1997

68PM302 INTEGRATED MULTIPROTOCOL PROCESSOR DEVICES

This document covers the MC68PM302 Revision C.1, Mask 1F85S. Errata listed in italics and which have change bars are new since the last published errata.

1. 16650 Break Indication

The 68PM302 16550 emulation of the following sequence is incorrect.

1. long break -> BRK bit in LSR is set
2. idle (during this period, the PC reads the LSR register and BRK bit is reset)
3. long break -> BRK bit in LSR is set again.

The actual 16550 will indicate break twice.

This sequence is emulated on the 68PM302 by the following sequence:

1. Stop Transmit Command by the 68k -> BRK bit in LSR is set
2. Restart Transmit Command by the 68k but no data to transmit -> wait idle period (during this period the PC reads the LSR register and BRK bit is reset)
3. Stop Transmit Command -> BRK bit in LSR is NOT set again !

The 68PM302's16550 emulator will indicate break only once. That's because between the two Stop Transmit Commands no data was transmitted. The 68PM302 "sees" this sequence as one long Stop Transmit Command (break).

This feature will not be changed in any future revisions.

2. Very Short Frames in Synchronous Protocols

If a 68PM302 SCC is used in a synchronous protocol mode (HDLC, BISYNC, or Transparent), AND the transmit frame is stored in just one data buffer, AND the transmit frame is only 1 or 2 bytes in total length (i.e. 1 or 2 bytes stored in the data buffer) AND more than one 68PM302 SCC is operating simultaneously, it is possible after some amount of time (minutes, hours, or days) for a frame to be reported as being transmitted successfully (i.e. the Tx BD shows that it has been transmitted without errors), but in reality, the frame was not transmitted over the TXD pin.

Workarounds:

1. In the case of transmitting a two byte frame, simply split the frame into 2 one-byte buffers. This will eliminate the problem, and will not affect serial performance.
2. Do nothing. Since the problem occurs very rarely, wait for the missing frame to be detected by the higher layers of the software, and a retransmission requested.

This errata will not be changed in any future revisions.

3. Use of 32KHz crystal with on-chip PLL (a change, not an errata)

On previous versions of the PM302 (Rev A and B), users were unable to use a 32KHz crystal with the on-chip PLL due to excessive jitter. This has been fixed on Rev C by rerouting the pins, **ONLY** when using 32KHz mode. When using any other mode, the PM302 pinout does not change, and remains as it was on Rev B. When using the 32KHz mode on Rev C, follow these instructions::

1. Signal PC_A4 from the PCMCIA connector is connected to pin NC1.
2. Signal PC_A5 from the PCMCIA connector is connected to pin NC2.
3. Pin PC_A4 (next to EXTAL) on the chip should be grounded.
4. Pin PC_A5 (next to EXTAL) on the chip should be grounded.
5. The serial resistor between XTAL and the Crystal changes to 1K Ohms. Capacitors between the Crystal and GND are 10 pf.

Notes: Changes 3,4 (grounding the pins) are not mandatory, but helped a lot in our enviornment. Changes 5,6 (different caps and resistors) helped in our envioronment, but they depend on the layout of the board and the crystal used. Once again, these changes only occur when using the 32KHz crystal mode of the PLL.