DEVICE ERRATA

April 15,1999

68EN302 INTEGRATED MULTIPROTOCOL PROCESSOR WITH ETHERNET DEVICE

This document covers the XC68EN302 Mask H74P(Rev B). Errata which have change bars are new since the last published errata.

1. V_{iH} sensitivity

The following pin has out of spec V_{iH} behavior:

TRST (JTAG Reset pin)
V_{iH} Min = 3.4 V

This bug exists in Rev 0.1 (1G97C), Rev A.1 (1H56B), and Rev B (H74P) silicon. The fix is under investigation.

2. Bus Arbitration in CPU Enabled Mode

When the MC68EN302 has the CPU enabled and the Ethernet Controller on that chip has just gotten the bus, the Module Bus Controller (MBC) will put out externally the Ethernet Controller's Bus Grant in response to a Bus Request coming in externally. The Bus Request is an input just at the moment when the Ethernet takes the bus and begins to assert Bus Grant Acknowledge. Then, about 1 clock later, the MBC will put out externally the negation of the Ethernet Controller's Bus Grant, finally the MBC will output the proper Bus Grant to the external request coming in.

This bug exists in the Rev A.1 (1H56B) and Rev B (H74P) masks of the MC68EN302. There is not going to be a fix.

WORKAROUND:

The user should mask the erroneous Bus Grant with Bus Grant Acknowledge, so that the external Bus Master doesn't see Bus Grant until the MC68EN302 has released the bus by negating Bus Grant Acknowledge.

3. Bus Arbitration in CPU Disabled Mode

When the MC68EN302 has the CPU Disabled, the Module Bus Contoller always negates Bus Grant Acknowledge to the internal 68302 slave, independent of the state of the external Bus Grant Acknowledge. So when the MC68EN302 Core's SDMA or IDMA has to use the bus, it will take the bus as soon as it sees Bus Grant. This will cause a conflict if an external bus master still has Bus Grant Acknowledge asserted.

This bug exists in the Rev A.1 (1H56B) and Rev B (H74P) masks of the MC68EN302. There is not going to be a fix.

WORKAROUND:

1. Mask the Bus Grant with Bus Grant Acknowledge, so that the slave MC68EN302 doesn't see Bus Grant until the other master has released the bus by negating Bus Grant Acknowledge.

2. If the other master is a MC68EN302 or a MC68302 and if their access is not more than 4 Clocks long (0 wait states), then the slave MC68EN302 will probably work since bus arbitration takes 2.5 to 4.5 clocks. By that time, the MC68302 or MC68EN302 bus master, since it only holds the bus for 1 memory cycle, should be finished. This workaround is not guaranteed for all Master cycles.

4. Transmit collision on last clock cycle of frame

NOTE THIS PROBLEM WILL NOT OCCUR WITH LEGALLY CONFIGURED ETHERNET.

If an illegal late collision occurs during the last clock cycle (last bit of CRC), the transmit block treats it as an early collision instead of a late collision. However, since the collision window has passed and the frame is no longer in the transmit FIFO, the transmit FIFO will send the next frame as retry data. This results in a loss of synchronization for the descriptor ring.

WORKAROUND:

This state is detectable if the node has not been transmitting for a long time and a frame remains in the transmit descriptor ring (the frame has been sent, but the status word is waiting for the next transmission). If this condition is detected, Ethernet_Enable must be deasserted and the transmit and receive buffer descriptors reinitialized.

If a second illegal late collision occurs during the last clock cycle of a subsequent frame, and the descriptor ring has not been resynchronized, the transmit block will hang and not allow any further frames to be sent.

This bug exists in Rev 0.1 (1G97C), Rev A.1 (1H56B), and Rev B (H74P) silicon. A fix is not planned at this time.

5. Mapping DRAM base address to 0

BUG DESCRIPTION

If one of the 68EN302 DRAM controller DBA0/1 registers are setup such that the DRAM base address is 0 there will be a conflict between the interrupt vector space (in DRAM) and the internal MOBAR, BAR, SCR and CKCR registers located at $EE, $F0, $F4, and $F8 respectively.

When RAM or EEPROM is mapped to address 0 and controlled via one of thechip select lines, the chip select does not assert when one of theseinternal registers is accessed. However the DRAM controller does not check for this special case, resulting in a simultaneous access to both DRAM and internal register.

WORKAROUND

Since these registers (with the possible exception of SCR) are used for configuration control, they can be set up at initialization time (beforeDRAM is mapped to $0) and copies of the register values stored elsewhere. After DRAM is mapped to $0, the copies of the registers may be accessed instead of reading the registers themselves.

6. Address Recognition - PA_REJ Control bit

In the device errata for the EN302 dated September 10, 1997, This function was reported not fixed on the Rev B part. This was a mistake. The PA_REJ Control bit was tested in more detail and was found to work in all documented configurations.