MC68331 DEVICE INFORMATION
(Issue 6 - 17 August, 1995)
Rev. A and B Silicon
E95B, E93N and F43E Mask Set

The following information and errata pertain to Revision A and B samples of the 68331 microcontroller. This revision contains the following module versions: CPU32V11, SIMV12, GPTV02, QSMV08. The phrase “This is an erratum” following each item below identifies characteristics of the current silicon which are expected to be improved. “This is information only” refers to enhancements, clarifications, and changes to the documented descriptions of the microcontroller and the modules within.

GENERAL INFORMATION:

1. On 20.97 MHz versions of this device, the following errata applies: IM:79 - If a Chip Select is synchronized with the E-clock by setting the MODE bit to a “1” in the Chip Select Option Register, then the MCU may stop normal operation. This is an erratum.

WORKAROUND: Do not synchronize Chip Select operation with E-clock.

CSOR[10:0] “MODE” bit must be “O”.

MODULE DETAILS:

68331:001

INTEGRATION: After power-up (Vdd Vdd min.) of the MCU, input/output and output-only port pins on modules other than the integration module may be in an indeterminate state for up to 15 ms (depends on ramp up conditions). Input/output pins on these modules may be in output mode (instead of high impedance) for a short time, which may create a conflict with external drive logic. This is information only.

68331:001

WORKAROUND: If a known state is required on these pins, before the 15 ms port initialization period, external reset control logic must condition these lines.

CPU32:045

CPU32: If an IACK cycle (with AVEC asserted) is terminated by a normal BERR, a Spurious Interrupt exception will be taken as expected. If the BERR of the IACK cycle is a LATE BUS ERROR (BERR asserted after AVEC), then a Type 4 bus error exception (Faults during exception processing) will be taken, in this case the Status Register in the stack frame will be corrupted and there can be no recovery from the exception. This is an erratum.

CPU32:045

Workaround: Do not allow LATE BERR during IACK cycles that are terminated with AVEC.

CPU32:046

CPU32: An incorrectly timed prefetch bus cycle may occur when there is a change of flow type of instruction (e.g. BRA, JSR) in progress when an interrupt request is recognized. With external DSACK logic, the effect is to make the minimum bus cycle time 5 clocks instead of the normal 3 clocks. With chip selects enabled, the effect is that the bus cycle is stretched by two clocks, regardless of the number of wait states selected. The incorrect bus cycle will not usually happen with zero wait states, however, a bus request (BR asserted) can cause the problem for any number of wait states. If external timing circuits expect the prefetch cycle to end when it should, i.e. a specific number of clocks after the assertion of DSACK, there may be a conflict. The extended cycle will be either immediately before or immediately after the IACK cycle. Some customers have reported that their logic appears to interpret the extra long bus cycle as a normal bus cycle followed by the start of an abnormally short bus cycle. This item usually causes harm when the external logic is “counting clocks” after a DSACK. This item is fixed on CPU32V12. This is an erratum.

CPU32:046

Workaround: External logic should wait for the rising edge of AS or DS to terminate the cycle. If external logic asserts DSACK and it is timed for 2 or more wait states, operation should occur correctly, since DSACK will assert at the proper time for the normal cycle termination point. Products using chips selects alone should not experience a problem, although the bus cycle will be stretched by two clocks.

CPU32:051

CPU32: If the internal bus is arbitrated away just before the last cycle of a MOVEM to memory, and the MOVEM is followed by other instructions which write to external memory (known problem instructions are: MOVE Rn,-(An) and LINK), then the data written by the last cycle of the MOVEM will be the same data as for the subsequent instruction (ex: MOVE). In other words, the next instruction (MOVE) started execution too early. Internal bus arbitration can occur in the following situations:

1. An external bus request occurs with the SHEN[1:0] = %11 or
2. If an on-chip alternate master (ex: DMA) module takes mastership of the IMB or
3. An external bus request occurs when Factory Test (Slave) mode is enabled.

This is an erratum.

CPU32:051

Workaround:

1. If external bus requests may occur, ensure SHEN[1:0] are anything except %11.
2. If an alternate master (DMA) is present on-chip, and operating, arrange instruction sequences to prevent the occurrence of MOVEM followed by another instruction which writes to external memory (MOVE Rn,-(An) or LINK). It is recommended to place a NOP after the MOVEM.
3. Factory Test (Slave) mode should not be used.

CPU32:053

CPU32: When there is a bus error on the second word of a released longword write cycle immediately before a TAS instruction, then the RR and RM bits in the special status word (SSW) are incorrect. The RR and RM bits represent the TAS cycle instead of the released write cycle. The bus cycle which had the error will not be re-run on the return from exception. Most applications do not experience this problem since software is not usually designed to interpret and recover from bus errors. The common reaction to a bus error is to abort the program flow, report the error occurrence, and then attempt to restart the application. Applications designed that way need not be concerned with this problem. This is an erratum.

CPU32:053

Workaround: Sometimes it is not possible to determine this fault condition from the stack and program contents. When the released write happens to be a byte write to supervisor space, the SSW looks exactly like a bus error on the TAS write cycle, and if the released write address is the same as the TAS address, the fault address is not different between the two cases. The bus error exception handling software may be able to resolve the situation in most cases by: (a) looking at the size, R/W, and function code information, or when that fails; (b) examining the faulted address and determining whether it is the same as the address that would be generated by the TAS instruction at the return program counter. When it is the case of a released write bus error, then setting RR and clearing RM should be the correct action (with RTE), after resolving the original cause of the bus error.

CPU32:056

CPU32: When a jump or branch to an odd address occurs and there is a pending bus error, the address error exception is incorrectly taken and the bus error exception is not taken. This is an erratum.

CPU32:056

Workaround: Do not jump or branch to odd addresses when bus errors can occur.

CPU32:058

CPU32: If IRQ7 is asserted and is released just before the IACK cycle and is then reasserted, only one IRQ7 interrupt is taken. This is information only.

CPU32:058

CPU32:062

CPU32: When exiting BDM, FREEZE is negated after to the DSI/IFETCH signal turns around from a input to an output. This means that an external development system could be driving DSI while the MCU is still driving IFETCH. This is information only.

CPU32:062

WORKAROUND: None

CPU32:069

CPU32: If the AVEC and DSACK signals are asserted simultaneously to terminate an IACK cycle, then the DSACK signal has higher priority. This is information only.

CPU32:069

IM:077

INTEGRATION: The loss of clock reference feature is not supported. Disregard bit position 4 in the SYNCR register (previously the SLIMP bit), this bit is now reserved. Insure that the bit position 2 in the SYNCR register is always written to it’s RESET state of %0 (previously the RSTEN bit). This is information only.

IM:077

IM:082

INTEGRATION: If PIT is used in either PLL mode or external clock mode with the PIT prescalar enabled (PTP bit in PITR register set), the PIT clock is 32 KHz (crystal or EXTAL/512 if in external clock mode). If the PITM field of the PITR register is written to zero, followed immediately by a nonzero value, and then LPSTOP is entered before 1 full period of the 32 KHz PIT clock source, the PIT timer will never decrement which may prevent exiting LPSTOP using the PIT timeout. This is an erratum.

IM:082

WORKAROUND: If the user wishes to stop the PIT and restart with a new time value by writing zero followed by the new value to the PITM field, the user should delay entering LPSTOP by at

least one 32kHz PIT clock period after writing the new value. Alternatively, the user can update the PITM field with the new value without first stopping the counter (writing zero to the PITM field). In this case, the timer will continue counting down to the original time value before updating to the new value.

IM:085

INTEGRATION: At power-up, chip select pins may drive low (asserted) until the first CLKOUT edge occurs. False writes may result on power up if the R/W pin does not have a pull-up resistor. The R/W line is in a high impedance state at power up and while reset is asserted. This is an erratum.

IM:085

WORKAROUND: Insure external writes cannot occur on power up by pulling up the R/W pin.

IM:086

INTEGRATION: At power-up, integration module I/O pins should initialize to the high impedance state. The following pins may, however, drive as outputs until the first CLKOUT edge occurs to initialize the internal logic into the high impedance state. Port E, D[15:0] and HALT (open Drain). This is an erratum.

IM:086

WORKAROUND: If external conflicts result in system problems on these pins, isolate these pins from external devices using a series resistor or buffer on the offending pin.

IM:088

INTEGRATION: If E-Clock synchronized chip selects (MODE=1) are used in combination with peripherals which can retry bus cycles an addressing problem may occur. Chip selects can be set up for synchronous E-clock support, configured for an 8 bit port and used with a peripheral connected to the upper data bus (D15:8 and BYTE = upper). A problem occurs during a word access of the 8 bit peripheral, in combination with a retry (terminate cycle with BERR and HALT) being requested by the device on the second cycle of the access. Under this condition, the second cycle will be retried, but [A0] will be incorrect. This is information only.

IM:088

WORKAROUND: Do not attempt retry of chip selects supporting synchronous E-clock cycles on 8 bit ports.

IM:092

Integration: Unusual system operation may occur when bus arbitration is used in combination with additional system configuration settings and timing. As an example of the behavior, chip selects may assert while the external bus is granted away (if they are programmed to respond to the interrupt stack addresses) and interrupt stack may get corrupted. Reset is the only way to recover once this occurs.

Conditions to initiate:

1. SHEN bits of MCR set to %00 or %10.

and

2. BR is asserted coincident with the AS of an IACK cycle. (BR assertion is within the range of before and after 1 clock relative to the falling edge of CLKOUT when AS asserts.)

and

3. IACK cycle is terminated with external AVEC.

This is an erratum.

IM:092

WORKAROUND:

1. Use SHEN=%11 to prevent the IMB from running cycles while the external bus is granted away.

or

2. Do not assert BR coincident with AS of an IACK.

or

3. Do not use external AVEC. Use a chip select to assert internal AVEC for external interrupts.

IM:095

INTEGRATION: Under certain conditions a masked interrupt may occur with an incorrect level. The conditions are: an external unmasked interrupt must occur coincident with an internal masked periodic interrupt (PIT). Also, previous to the above interrupts, an external interrupt line at the same level as the masked PIT interrupt must have been asserted and remain asserted. Example sequence to cause problem:

1. Set CPU interrupt mask to 5;
2. Set PIT to level 2;
3. Hold IRQ2 line low.
4. Assert valid IRQ interrupts (asserting IRQ 6 or IRQ7) the PIT exception is taken if pending. This is an erratum.

IM:095

WORKAROUND: Do not allow matching levels on PIT and external pin.

IM:097

INTEGRATION: Several conditions combined may introduce apparent Periodic Interrupt Timer (PIT) clock errors. The clock error occurs if LPSTOP mode is entered and exited periodically using the PIT, and the system clock is set to minimum (131 KHz) prior to entry of LPSTOP mode and set to maximum at LPSTOP exit (PLL must re-lock). Also, on exiting from LPSTOP, the CPU will be held off of the bus until the PLL is re-locked. Variations in the PIT clock period may appear as the PIT counter missing clocks (the PIT is clocked by the EXTAL reference clock in LPSTOP, if STSIM = 0). During normal operation (not in LPSTOP) the PIT counter clock source (EXTAL) is synchronized by logic to the system clock (CLKOUT). The combination of PLL re-lock time, low frequency (131 KHz) clock source (too near 32 KHz reference), and the synchronization result in this behavior. This is information only.

IM:097

WORKAROUND: Use a minimum PLL frequency of 8 times the reference frequency (262 KHz for a 32 KHz reference) or higher if the system clock is toggled from a low frequency prior to LPSTOP entry (if STSIM = 0) and back to maximum on exit of LPSTOP periodically using the PIT as the controlling source. The problem is only seen when switching the PLL clock to a frequency that is too close to the reference (EXTAL) clock frequency.

IM:139

INTEGRATION: The RESET assertion time specification (#77) is 4 clocks (tcyc) minimum. However, the current version of this module requires RESET to be asserted until the current bus cycle in progress completes. This is an erratum

IM:139

WORKAROUND:

Assert the RESET pin for 2 clock cycles longer than the present timeout period of the bus monitor (BMT field in SYPCR register). This will result in an internal reset, independent of other system conditions (Bus Monitor does not need to be enabled).

VCO:051

INTEGRATION: In some Phase Lock Loop (PLL) documentation a three component filter from XFC to VDDSYN is recommended (18K resistor in series with 0.01 uF capacitor between VDDSYN and XFC, the series combination in parallel with a 3300 pF capacitor for a loop multiplier of N = 512). It has been determined with this three component filter, in the presence of external leakage (in excess of that provided by ~50 M Ohm) on the XFC pin, may result in the MCU not exiting RESET at power up. During this condition, the output frequency on CLKOUT is at the target value, but the PLL lock detect logic does not detect lock and continues to cause RESET assert ion. Versions of the integration module that are configured for either a slow or fast (Typ. 32.768 kHz or 4.194 MHz) crystal source use the same filter component values, since the internal reference frequency is always slow (32.768 kHz). Also, leakage from the XFC pin must not be in excess of test provided by a 15 M Ohm resistor to meet PLL jitter specifications (with 0.1 uF XFC filter, refer to Electrical Characteristics section of Users manual). If the PLL is not enabled (MODCK=0 at RESET) then the XFC filter is not required and the pin may be left unconnected but VDDSYN must be connected to VDD (This item was previously IM:179). This is information only.

VCO:051

WORKAROUND: Do not use the three component filter on XFC. Use the originally documented filter (single 0.1 uF capacitor from the XFC pin to the VDDSYN supply pin).

VCO:059

INTEGRATION: The PLL Lock time (tlpll) specification of 20 ms at warm startup (VDD power up with VDDSYN applied) may not be met under some conditions. The internal PLL lock detection logic holds off assertion of the SLOCK bit in the SYNCR register during the PLL re-lock time and may result in a time longer than the specification in increments of 10 msec (20, 30 or 40 msec). (This was previously IM:098). This is an erratum.

VCO:059

WORKAROUND: Allow additional lock time (50 ms total lock time) under warm startup conditions.

Archived: 18 Aug, 95

Revision 0.0, 20 NOV 96

last update: Mar 26 1998