56F8166

Preliminary Chip Errata

56F8166 Digital Signal Controller

This document reports errata information on chip revision A. Errata numbers are in the form n.m, where n is the number of the errata item and m identifies the document revision number. This document is a pre-publication draft.

Chip Revision A Errata Information:

The following errata items apply only to Revision A 56F8166 devices. These parts are either marked with date codes of 0437 or greater (bottom line of marking).

Errata Number	Description	Impact and Work Around
1.0	OCCS shutdown function is not as restrictive as desired.	Impact: This is one of several safety interlocks to prevent a coding error from shutting down the part accidentally. Work Around: The OCCS ISR should explicitly check for a loss of reference clock status bit set prior to shutting down the OCCS.
2.0	Unable to read COP counter register.	Impact: Unable to read COP counter register when the PLL is not on. Work Around: Read COP counter when PLL is in use.
3.0	Command conflict when setting CCIF in the Flash Module.	Impact: If the CCIF is set at the exact same time the CBEIF bit is cleared, only the set will occur. This gives the impression that a command has completed when in fact it is active. This can only occur on the very last cycle of a pipeline operation. Work Around: Use driver software to avoid issue.
4.0	Flash program/erase operations can cause other peripheral register access to be dupicated.	Impact: This condition can cause issues with the transmit/receive registers and quadrature decoder hold registers. Work Around: Avoid peripheral I/O to any peripheral except the Flash Module for 2 CPU cycles prior to writing to a flash memory over it's system bus interface.

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Errata Number	Description	Impact and Work Around
5.2	The LVI interrupt signal polarity in STOP mode is inverted. *In Rev 2.0, clarified errata impact and work around.*	Impact: The processor will not enter STOP mode if LVI is enabled or LVI IPL is set in the IPR2. Work Around: Disable LVI interrupt and clear LVI IPL. With this work around LVI will not wake up the processor from STOP mode.
6.0	Wait mode operation is inconsistent in debug mode.	Impact: WAIT appears to work properly when the device is in mission mode. In debug mode, the WAIT instruction sometimes has no effect. Work Around: Test WAIT mode operation outside of the debug environment.
7.0	EOnCE registers use the wrong clock. I/O fails in presence of holdoffs.	Impact: Real-time debugging not available. EOnCE reads will fail in the presence of holdoffs. Work Around: For EOnCE writes use NOP padding. No workaround for EOnCE reads in presence of holdoffs.
8.0	Software breakpoint in uninterruptable code can cause the debugger to execute instructions in the wrong order.	Impact: Use work around. For example, a conditional branch followed by two single word instructions with DBGHALT replaces the first instruction after the conditional branch. Work Around: CodeWarrior has implemented a workaround which utilizes NOP padding.
9.0	The SCI TIDLE flag may not be cleared immediately upon transmission of a break character via the SBK bit of the SCI control register.	Impact: This can result in a premature transmitter IDLE interrupt. This only occurs when using the SBK bit of the SCICR to transmit break characters. Workaround: Poll the TIDLE bit of the SCI status register. Do not enable interrupts until TIDLE goes low. IF polling for TIDLE high, make sure that it is seen going low first before responding to TIDLE high. Make sure that TIDLE is cleared and then later set after transmitting break characters.
10.0	The interrupt controller uses the COP reset vector at startup if the COPR bit in the SIM_RSTSTS register is set, even if the current reset is not COP reset.	Impact: Same as description Workaround: Clear the SIM_RSTSTS as part of the startup procedure.

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11.0	The EOnCE OPDBR register will not work properly if there is more than one JTAG serially connected device used in a scan chain configurations.	Impact: This register is used for executing instructions shifted in by the host through the JTAG when the device is in debug mode. The intended instruction will not be executed under this condition. Note: This does not affect boundary-scan operation, which will still work properly no matter what position the device is placed in the boundary-scan chain. Workarounds: 1. Each device must be on a separate scan chain for debugging purposes. 2. If there is only one 56800E device on a scan chain, then the EOnCE OPDRB register will work properly as long as the 56800E device is the first device on the scan chain.
12.0	The CodeWarrior debugger is not sensitive enough to the operation frequency of the device. Memory code may be corrupted when setting/ clearing.	Impact: Once the PLL is engaged, the device may be under erased/programmed when setting and clearing breakpoints. Workaround: flash.cfg file should contain the following entry: set_hfmclkd 0x14 This sets the on-chip flash interface unit to use the maximum program time at 4MHz system rate. At 40MHz, program/erase times will be less than desired, but appear operational under otherwise normal conditions. Use of hardware breakpoints also eliminates this issue.
13.0	The setting of the CHNCFG bits in the ADCR1 register for the mux channels associated with converter 0 override the settings for the mux channels associated with converter 1.	Impact: This problem effects scans with a mix of single ended and differential mode conversions. If AN0/2-AN1/3 is set for single ended then AN4/6-AN5/7 can't properly execute differential conversions and vise versa if AN0/2-AN1/3 is set for differential mode AN4/6-AN5/7 can't properly execute single ended conversions. Settings for differential mode for converter 1 also adversely effect single ended conversions in converter 0. Work Around: Restrict conversion types so that the cases described do not occur.
14.0	With a Quad Timer counter, when using a single compare register to generate timing intervals and clocking the timer at a rate other than at the IPbus_clock rate the timer may count incorrectly when the compare register is changed.	Impact: When the compare register matches the counter register and is updated before the next timer clock the counter increments/decrements instead of reloading. Work Around: 1. Use both compare registers, such that the compare register that is not active is updated for use in the next count period. 2. Instead of updating the compare register, architect the software so the LOAD register can be updated, with the compare register held constant. FAQ 25527 provides an in-depth discussion of this issue and can be found on the Freescale website. *freescale.com.*

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Errata Number	Description	Impact and Work Around
15.1	GPIO interrupts on the SAME port will not be detected if the edge of an input interrupt signal occurs in the same clock cycle that the IESR is written.	Impact: Hardware designs that have asynchronous interruptable inputs on the same GPIO port cannot rely on the device to generate the interrupt. Work Around(s): 1. Use different ports for these two interrupts. 2. After writing to the IESR, read the RAW_DATA register to determine if any other inputs have occurred at this exact instant.
16.2	With the Quad Timer, when using Count Mode (CM) 0b110 “edge of secondary source triggers primary count till compare” and the Output Mode (OM) is 0b111 “enable gated clock output while counter is active”, the OFLAG will incorrectly output clock pulses prior to the secondary input edge if the primary count source is not an IPBus clock/N.	Impact: Typically this will arise when an application is trying to output as finite number of 50% duty cycle clock pulses triggered by the output of another timer. Timer 1 creates an infinite pulse train which is fed into the primary input of Timer 2. Timer 2's secondary input is the triggering signal. Timer 2's job is to wait until the trigger and then count out the correct number of clock pulses. Work Around: The workaround is to rearrange functionality. Timer 1 uses an IPBus/N to generate a pulse train at 2x the desired clock rate. It uses CM = 0b110 and OM = 0b111 correctly. Then Timer 2's job is to simply convert the 2x pulse stream into a clock pulse stream at 1x frequency and 50% duty cycle. It does this by CM = 0b001 (count rising edges of primary input) and OM = 0b011 (toggle OFLAG on successful compare) with a compare value of zero.

17.3	If runtime flash programming is desired, Power-on reset (POR) of the device may not be fully effective for slow rise times of V_{DD} and/or V_{DDA}, on some small fraction of parts.	Impact:
		It may not be possible to write to the flash if the reset cause is not a software reset.
		
		Workaround:
		If runtime flash programming is desired, add the software reset in startup code if the reset cause is not a software reset. Example code:
		`If bit SWR of RSTSTS register is not set`
		`Set logical 1 to bit SWRST of SIM_CONTROL Register`
		`While loop (to wait for reset)`
		`else (continue with startup code)`

Errata Sheet History

Previously Documented in Past Errata Sheets	Correction
GPIO interrupts on the SAME port will not be detected if the edge of an input interrupt signal occurs in the same clock cycle that the IESR is written.	New item in Rev 1 of this errata sheet

Errata Sheet History (Continued)

Previously Documented in Past Errata Sheets	Correction
With the Quad Timer, when using Count Mode (CM) 0b110 “edge of secondary source triggers primary count till compare” and the Output Mode (OM) is 0b111 “enable gated clock output while counter is active”, the OFLAG will incorrectly output clock pulses prior to the secondary input edge if the primary count source is not an IPBus clock/N.	New item in Rev 2 of this errata sheet
If runtime flash programming is desired, Power-on reset (POR) of the device may not be fully effective for slow rise times of V_{DD} and/or V_{DDA}, on some small fraction of parts.	New item in Rev 3 of this errata sheet

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