

Freescale Semiconductor Chip Errata

Document Number: MC56F8002E

Rev. 4, 05/2014

Mask Set Errata for Mask 2M53M

Introduction

This report applies to mask 2M53M errata information for the MC56F8002 Digital Signal Controller.

Errata Number	Description	Impact and Workaround
1	If the Computer Operating Properly (COP) is used to wake the device from the Partial Power Down (PPD) mode, the COP may count down too quickly.	Impact: The device may not wake from the PPD mode reliably. Workaround: Use the RTC timer to wake from the PPD mode to the Run mode, rather than the Computer Operating Properly (COP) or use a timeout longer than 100MS for the COP to wake the device from Partial Power Down mode. The COP may be used to bring the device out of PPD mode if the COP is driven by the low power oscillator rather than by a crystal.
5	The VBA register reset value suggests the interrupt vector table should be placed at program address word 0x1000 instead of 0x800.	Impact: When the VBA is not correct the device may vector to an undetermined address. Workaround: Initialize the VBA register in the startup code, rather than utilize the reset value.
7	Unexpected Loss of Reference (LOR) from COP when COP clock is slower than the IP Bus Clock causes reset of system. The LOR function must be enabled in the COP for this to happen, as well as for the COP to be clocked more slowly than the IP Bus Clock.	Impact: Unexpected Loss of Reference (LOR) from COP. Workaround: Increase the COP clock speed, decrease the system clock speed, or disable the LOR feature of the COP with the configuration bit.





Document Revision History

Revision	Correction
0	Initial release
1	Added workaround for Errata Number 1
2	Added Errata Number 6
3	Added Errata Number 7
4	Removed errata 2, 3, 4, and 6



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