Document Number: MC34709ER
Rev. 3.0, 11/2012

MC34709, Silicon Errata (N88D)

Introduction

Device Revision Identification

This errata document applies to the following devices:

Table 1. Silicon Revision

Package	Part Number	Silicon Revision	Part Marking	Die ID
8 x 8	MC34709VK	P1.2	M34709VK	DA02N88D

Device Build Information / Date Code

Device markings indicate build information containing the week and year of manufacture. The date is coded with the last four characters of the nine character build information code (e.g. “CTZW1025”). The date is coded as four numerical digits, where the first two digits indicate the year and the last two digits indicate the week. For instance, the date code “1025” indicates the 25th week of the year 2010.

Device Part Number Prefixes

Some device samples are marked with a PC prefix. A PC prefix indicates a prototype device which has undergone basic testing only. After full characterization and qualification, devices will be marked with the MC prefix.

General Description

This errata document applies to the MC34709 data sheet.

Table 2. Definitions of Errata Severity

Errata Level	Meaning
High	Failure mode that severely inhibits the use of the device for all or a majority of intended applications.
Medium	Failure mode that might restrict or limit the use of the device for all or a majority of intended applications.
Low	Unexpected behavior that does not cause significant problems for the intended applications of the device.
Enhancement	Improvement made to the device due to previously found issues on the design.

Table 3. Errata for the MC34709

Errata Number	Erratum	System Impact	Description
High Severity Level			
4	**Buck Regulator:** Regulator output undershoot in APS mode.	Undershoot may cause processor to shutdown.	In APS mode the regulator output may undershoot for approximately 10 µs under transient loads of 1/2 of max rated current. Output voltage may drop as much as 160mV. **Workaround:** SW1-5 must be operated in PFM mode for loads lower than 100 mA and in PWM mode for loads greater than 100mA in order to meet the transient load response specification. **Fix Plan/Status:** No fix scheduled.
5	**RTC:** VSRTC drops out with slowly decaying battery and a valid coin cell.	In applications with a Li-Ion battery, the RTC can be lost when the battery voltage drops to ~2.2 V. In applications where VBATT is driven by an external source, the RTC can be lost as the voltage transitions below the 2.2 V range during power down.	There is an issue with the 'Best of Supply' switch, which powers VDDLP. During the change over from the primary power source to the coin cell, the VDDLP can dip to a voltage below the minimum voltage required to power the RTC. • The VSRTC supply is derived from VDDLP, and therefore affects the RTC of the application processor, as well as the on-board RTC • The 32 kHz clock to the processor's SRTC also drops out. **Workaround:** Figure 1 is the application circuit recommended for all applications where the RTC is used with a back-up coin cell attached to the MC34709. The LDO output is set to 1.5 V with a Schottky diode in series which keeps the voltage supplied to VDDLP below the VCOREDIG (1.5 V). • Add a low quiescent current 1.5 V LDO, supplied by the coin cell (LICELL pin). Recommended LDO: NCP4682/4685(1) or equivalent with a 1uA typical IQ. • Add a low voltage Schottky diode (D1) to block the output capacitance (C3) of LDO. • Add a low voltage/low leakage Schottky diode (D2) from LICELL to VIN of the LDO. • Add a low voltage/low leakage Schottky diode (D3) from BP to VIN of the LDO. **Fix Plan/Status**: No fix scheduled

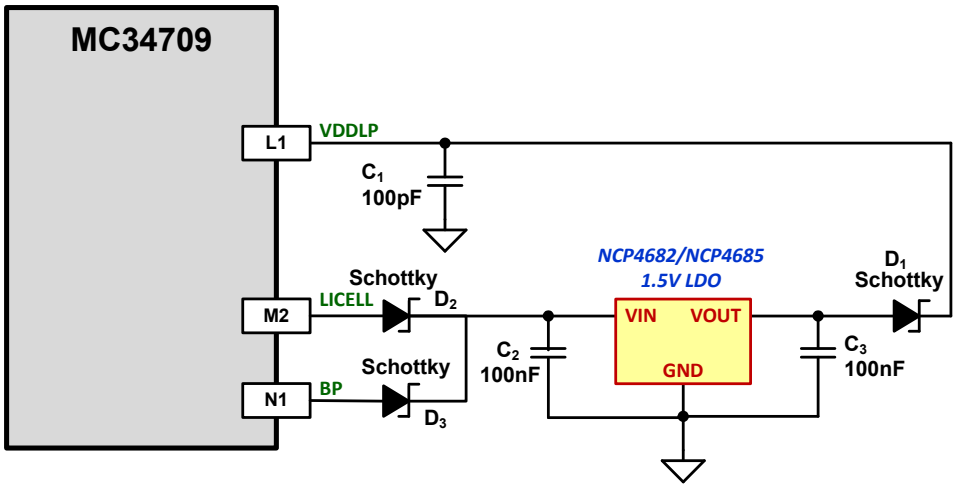

Figure 1. RTC Workaround Application Circuit

Notes

1. Freescale Disclaimer: Freescale does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

Table 3. Errata for the MC34709

Errata Number	Erratum	System Impact	Description
7	**VSRTC/Power Up:** When hot plugging BP, the VSRTC regulator may fail to regulate.	Application will not power up even with a PWRONx button press.	During a hot plug event on BP, the VSRTC, VDDLP and VCOREREF rails may not come up. Bringing the PWRONx pin low momentarily, will not turn on the IC. **Workaround:** Apply workaround shown in Figure 1. If a back-up coin cell is not present in the application, diodes D_2 and D_3 are not required. In this case the BP node can be connected directly to the VIN of the external LDO. **Fix plan/Status:** No fix scheduled
Medium Severity Level			
2	**LDO Regulator:** SCP nonfunctional	SCP may not turn off the internal pass LDOs (VGEN1 and VUSB) when a short circuit event is present.	The short circuit protection (SCP) could fail to shut down the VGEN1 and VUSB internal LDOs due to random variation of the shutdown timing.These LDOs will be protected by the current limit of the LDO. The short circuit protection will protect external pass (PNP) LDOs (VUSB2, VGEN2, and VDAC) from dissipating too much power. Therefore the short circuit protection should always be enabled by setting REGSCPEN=1. **Workaround**: None. Recommended to keep REGSCPEN=1. **Fix plan/Status:** No fix scheduled
6	**Coin cell:** Extra current draw on coin cell	The coin cell will discharge faster when the battery voltage is between 2.5 V and 2.2 V.	The battery current spikes up to 350 μA, during the coin cell transition (BP is ~2.2 V) and the coin cell draws up to 160 μA of current. **Workaround:** None **Fix Plan/Status:** No fix scheduled
8	**Incorrect CLK32K and CLK32KMCU Output**: Clock outputs not square. Falling edge may be step shaped.	Incorrect CLK32KMCU may cause system to hang. 2 to 5% of the units are affected.	When CLK32KVCC is higher than 2.0 V, ground bounce internal to the MC34709 can result in the CLK32K and CLK32KMCU outputs being step shaped. The issue does not occur when CLK32KVCC is below 2.0 V. **Workaround:** • Applications not using the CLK32K output: connect CLK32KVCC to ground. CLK32KMCU will continue to output 32 kHz clock pulses at the VSRTC level. • Applications using the CLK32K output: For CLK32K output level higher than 2.0 V, connect a 120 Ω resistor in series with the CLK32KVCC pin. The resistor should be connected between the CLK32KVCC pin and the bypass capacitor. For CLK32K output level lower than 2.0 V, no workaround is needed.
9	**Startup:** False start of regulators	As BP begins its ramp up from between 100 mV and UVDET, either or both may occur: • the buck regulator outputs can momentarily glitch high • the buck regulators may not start up	When BP voltage falls below the UVDET voltage, a turn-off event occurs. When BP voltage is re-applied subsequently before the BP voltage falls below 100 mV, regulator outputs may glitch while BP is ramping up. The above scenario can happen when BP is re-applied before the capacitors at BP have not discharged fully. **Workaround:** Design the regulator supplying BP such that its output is discharged to ground when disabled. This can be accomplished using bleeder resistors, if the supply does not have an active pull-down. **Fix Plan/Status:** No fix scheduled
Low Severity Level			
3	**Buck Regulator:** Forced to PWM mode instead of APS mode	SW4A/B efficiency will be reduced.	When SW4A and SW4B are in independent configuration and one of the outputs is loaded, the unloaded channel SRFET allows negative current to flow in the inductor; this causes the unloaded regulator to be forced into PWM mode when it should be in APS mode. **Workaround:** None. Due to the workaround in erratum 4, this issue is no longer applicable. **Fix Plan/Status:** No fix scheduled.

Table 4. Revision History

Revision	Date	Description of Changes
1.0	10/2012	• Initial release
2.0	10/2013	• Updated errata 8
3.0	11/2013	• Redefined errata 9

RoHS

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