MC33903, MC33904, and MC33905, Mask M87W, Rev. 3.2 Errata

Introduction

This errata sheet applies to the following device part numbers:

33903	33903S (Single LIN)	33903D (Dual LIN)	33904	33905S (Single LIN)	33905D (Dual LIN)
MCZ33903B3EK/R2 (1), (2)	MCZ33903BS3EK/R2 (1), (2)	MCZ33903BD3EK/R2 (1), (2)	MCZ33904B3EK/R2 (1), (2)	MCZ33905BS3EK/R2 (1), (2)	MCZ33905BD3EK/R2 (1), (2)
MCZ33903B5EK/R2 (1)	MCZ33903BS5EK/R2 (1)	MCZ33903BD5EK/R2 (1)	MCZ33904A5EK/R2 (1)	MCZ33905S5EK/R2 (1)	MCZ33905D5EK/R2 (1)
			MCZ33904B5EK/R2 (1)	MCZ33905BS5EK/R2 (1)	MCZ33905BD5EK/R2 (1)

Notes
1. The following part number is affected by Section , *Serial Peripheral Interface (SPI) Operation*
2. The following part number is affected by Section , *Higher VDD voltage during EMC tests on 3.3 V VDD devices.*

Device Revision Identification

The device revision is indicated by a 1-character code after the device code. All standard devices are marked with device identification and build information code. The MC33903, MC33904, MC33905S, and MC33905D, are identified by the following markings:

Engineering Samples:

- 1st line marking: Logo and assembly location
- 2nd line marking: PCZ33904Axxx or PCZ33905Sxxx or PCZ33905Dxxx
- 3rd line marking: pass 3.1
- 4th line marking: date code

Marking for production release material or MCZ material as below:

- 1st line marking: (F) MCZ33904AxEK or MCZ33905SxEK or MCZ33905DxEK
- 2nd line marking: AWLYYWWZ (Date Code)
- 3rd line marking: CCCCC (CHINA)

Device Build Information / Date Code

Device markings indicate build information containing the week and year of manufacture. The date is coded with the last four characters of the nine character build information code (e.g. “CTKAH0429”). The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the week. For instance, the date code “0429” indicates the 29th week of the year 2004.

Device Part Number Prefixes

Some device samples are marked with a PC prefix. A PC prefix indicates a prototype device which has undergone basic testing only. After full characterization and qualification, devices will be marked with the MC prefix.

Serial Peripheral Interface (SPI) Operation

Description:

In some instances, the SPI write command is not properly interpreted by the device. This results in either a “non received SPI command” or a “corrupted SPI command”, caused by the synchronization between internal and external (oscillator and Chip Select) signals.

Only SPI **write** commands (starting with bits 15,14 = 0,1) are affected. The SPI **read** commands (starting with bits 15,14 = 0,0 or 1,1) are not affected.

The occurrence of this issue is extremely low and can be fully prevented by implementing the workaround specified below.

Consequence:

This anomaly results in either a “non received SPI command” or a “corrupted SPI command”, caused by the synchronization between internal and external (oscillator and Chip Select) signals.

Root cause:

The root cause of this behavior results when the Chip Select ‘low’ duration is equal to the oscillator’s operating duration, the oscillator does not re-start on the Chip Select low to high transition, and a message sent is not written to the register.

Devices impacted:

MC33903, MC33904, and MC33905 (all device types)

Work around:

The workaround consists of 3 steps:

1. Ensure the duration of the **Chip Select Low (t_{CSLOW}) state is >5.5 µs.**

   Note: In data sheet revisions prior to 7.0, this parameter is not specified and is indirectly defined by the sum of 3 parameters, t_{LEAD} + 16 x t_{PCLK} + tLAG (sum = 4.06 µs).

2. Ensure SPI timing parameter **t_{LEAD} is a min of 550 ns**.

   Note: In data sheet revisions prior to 7.0, the t_{LEAD} parameter is a min of 30 ns.

3. Make sure to **include a SPI read command after a SPI write command.** In case a series of SPI write commands is used, only one additional SPI read is necessary. The recommended SPI read command is “device ID read: 0x2580” so device operation is not affected (ex: clear flag). Other SPI **read** commands may also be used.

When the previous steps are implemented, the device will operate as follows:

For a given SPI write command (named SPI write ‘n’):

- In case the SPI write command ‘n’ is not accepted, the following SPI command (named SPI ‘n+1’) will finish the write process of the SPI write ‘n’, thanks to step 2 (t_{LAG} > 550 ns), and step 3 (which is the additional SPI command ‘n+1’).
- By applying steps 1, 2, and 3, no SPI command is ignored. Worst case, the SPI write ‘n’ is executed at the time the SPI ‘n+1’ is sent. This will lead to a delay in device operation (delay between SPI command ‘n’ and ‘n+1’).

  Note: Occurrence of an incorrect command is reduced, thanks to step 1 (extension of tCSLOW duration to >5.5 µs).

Higher VDD voltage during EMC tests on 3.3 V VDD devices.

Description:

The maximum VDD output voltage for ALL 3.3 V VDD devices has been increased to 3.4 V, so the device stays within specification during EMC tests.

Note: In data sheet revisions prior to 7.0, the $V_{OUT-3.3}$ parameter is a maximum of 3.366 V.

Devices impacted:

All 3.3 V VDD devices

Recommendation, work around:

There is no work-around.

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