LPC55S3x

Errata sheet LPC55S3x

Rev. 1 — 29 August 2023 Errata

Document information

Information	Content
Keywords	LPC55S36, LPC55S34
Abstract	LPC55S3x errata

1 Product identification

The LPC55S3x HLQFP100 package has the following top-side marking:

- First line: LPC55S36JBD100
- Second line: xxxxxxx
- Third line: **zzz**yywwx**R**
  - yyww: Date code with yy = year and ww = week.
  - xR: Device revision 1B

The LPC55S3x HVQFN48 package has the following top-side marking:

- First line: LPC55S3x
- Second line: JHI48
- Third line: xxxxxxxx
- Fourth line: **zzz**yywwx**R**
  - yyww: Date code with yy = year and ww = week.
  - xR: Device revision 1B

2 Errata overview

Table 1. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
PKC.1	The PKC PKC_CTRL[STOP] bit does not function correctly.	1B	Section 3.1
I3C.1	Data lost when using the DMA to write transmit data to I3C, and the data size is greater than the I3C FIFO size.	1B	Section 3.2
I3C.2	IBI Slave Data EXTDATA is not abortable by another master on the bus.	1B	Section 3.3
PLL.1	PLL LOCK bit is not reliable	1B	Section 3.4
ROM.1	The warm reset cause status register (RESETCAUSE) in the PMC module does not function properly if the device is configured to operate above 100 MHz.	1B	Section 3.5

Table 2. AC/DC deviations table

AC/DC deviations	Short description	Product version(s)	Detailed description
n/a	n/a	n/a	n/a

Table 3. Errata notes

Errata notes	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

3 Functional problems detail

3.1 PKC.1: The PKC PKC_CTRL[STOP] bit does not function correctly

Introduction

The LPC55S3x Family includes a Public-Key Crypto Coprocessor (PKC) peripheral. The PKC_CTRL[STOP] bit is intended to allow freezing PKC calculations for power savings.

Problem

Setting PKC_CTRL[STOP] may not cleanly freeze PKC activity, and could lead to repeated RAM accesses. After PKC_CTRL[STOP] is set, reading its value never returns 1.

Workaround

None.

3.2 I3C.1: Data lost when using the DMA to write transmit data to I3C, and the data size is greater than the I3C FIFO size

Introduction

The LPC55S3x includes an I3C peripheral with a DMA interface that can be used to transfer data to or from the I3C data FIFO.

Problem

The issue occurs when using I3C to transmit data written by the SDMA to the Slave Write Data Half-word (SWDATAH)/Master Write Data Half-word (MWDATAH) registers or Master Write Message Data (MWMSG_SDR_DATA) register 2 bytes at a time. If the number of bytes to send exceeds the FIFO size of 8, data is overwritten by the SDMA after the FIFO becomes full.

Workaround

Set the DMAWIDTH field to 10 (Half word) in the Slave DMA Control (SDMACTRL)/Master DMA Control (MDMACTRL) registers and use the Slave Write Data Byte (SWDATAB)/Master Write Data Byte (MWDATAB) to write the SDMA data. Avoid using the Slave Write Data Half-word (SWDATAH)/Master Write Data Half-word (MWDATAH) registers or Master Write Message Data (MWMSG_SDR_DATA) register.

3.3 I3C.2: More than one In Band Interrupt (IBI) extended data bytes (EXTDATA) emitted by I3C slave are not abortable by the I3C bus master.

Introduction

On these devices, I3C peripheral works in master (controller) as well as in slave (target) mode. This I3C peripheral supports IN Band Interrupt (IBI) feature which allows it in target mode to notify the I3C controller of an interrupt . The I3C target on this device supports up to 7 bytes of extended IBI data following mandatory data byte (MDB). Most IBIs would not use EXTDATA and are only a single MDB.

Problem

When I3C peripheral, on these devices is working as a target device and transmits EXTDATA with more than one byte past the MDB, EXTDATA in IBI are not abortable by the controller on I3C bus.

Workaround

None.

Only use the standard IBI model of one MDB or one MDB and one additional byte. It is recommended to agree on data-size(EXTDATA) with external controller before transfer, so that controller will not need to abort EXTDATA.

3.4 PLL.1: PLL LOCK bit is not reliable

Introduction

On the LPC55S3x devices, PLLxSTAT register of PLLs contains a LOCK detector status bit (bit 0 of PLLxSTAT register).

When the LOCK detector status bit is set to 1, the PLL is considered to be locked and stable.

The PLL LOCK signal is specified to work for Fref range from 100 kHz to 20 MHz. When the Fref is below 100 kHz or above 20 MHz, software should use a 6 ms time interval to insure the PLL will be stable.

Problem

On the LPC55S3x, the PLL status LOCK bit is not always reliable in the ranges specified and as a result, the PLL doesn´t initialize correctly.

Workaround

For Fref ≥ 20 MHz:

Software must wait at least (500us + 400/Fref) (Fref in Hz result in s) to ensure the PLL is stable.

For Fref < 20 MHz:

- If the PLL lock detector status bit is 1 before the wait time duration ((500us + 400/Fref)) is completed, the PLL is stable.
- If the PLL lock detector status bit is 0 but the wait time duration ((500us + 400/Fref)) is completed, the PLL is stable.

Software workaround is implemented in SDK 2.14 clock driver version 2.3.7.

Remark: This errata does not apply for spread spectrum mode.

3.5 ROM.1: When the device is configured to operate above 100 MHz, the warm reset cause status register (RESETCAUSE) in the PMC module does not function properly

Introduction

In LPC55S3x devices, the digital glitch detector(GDET) sensor on the device is configured for the voltage range to operate the device at 96 MHz or below frequency only. When a user is planning to operate the device beyond 100 MHz, the Power Management Controller(PMC) module should be configured for higher voltage settings.

User application should disable the glitch detector before changing the PMC voltage control registers in the PMC module.

Problem

When PMC voltage registers in the PMC module are configured for more than 100 MHz and a warm reset event such as watchdog reset or ARM system reset request occurs, the execution control goes back to ROM. But the boot ROM enables the glitch detector to protect boot flow with SWRRESET (emulated Power on Reset(PoR)) reaction for a glitch attack event. Since PMC registers are configured for higher voltage settings and not cleared on warm reset, the glitch event is triggered causing a new emulated PoR reset (SWRRESET). The emulated PoR reset clears PMC voltage control registers and reset cause status register. The device boots subsequently due to emulated PoR (SWRRESET), however original reset cause status is lost and SWRRESET bit in the RESETCAUSE register is set.

Note: *The PMC voltage control registers are reset only on cold reset events (PoR or emulated PoR called SWRRESET).*

Workaround

When the application disables GDET to operate the device at frequencies greater than 100 MHz, then SWRRESET bit in RESETCAUSE register should be used as an indicator for watchdog reset status, given that the application does not use Software Reset Register (SWR_RESET) present in the SYSCON module to generate software reset.

4 AC/DC deviations detail

No known errata.

5 Errata notes detail

No known errata.

Revision history

Revision history

Rev	Date	Description
v.1	20230829	Initial version

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