Mask Set Errata for Mask 2N22D

Introduction

This report applies to mask 2N22D for these products:

- KINETIS

Errata ID	Errata Title
4588	DMAMUX: When using PIT with "always enabled" request, DMA request does not deassert correctly
5751	FTFx: Launching the Read 1's Section command (RD1SEC) on an entire flash block results in access error (ACCER).
5706	FTFx: MCU security is inadvertently enabled (secured) if a mass erase is executed when the flash blocks/ halves are swapped. This issue only affects applications that use the flash swap feature.
2793	I2C: MCU does not wake as expected from STOP or VLPS mode on subsequent address matches if previous address is mismatched
4590	MCG: Transitioning from VLPS to VLPR low power modes while in BLPI clock mode is not supported.
4481	PMC: STOP mode recovery unstable
4638	PMC: VLLSx mode current draw at cold can exceed maximum specification at cold
5667	PMC: When used as an input to ADC or CMP modules, the PMC bandgap 1-V voltage reference is not available in VLPx, LLS, or VLLSx modes
5138	RTC: The RTC_WAKEUP pin does not operate as specified and the WPON bit in RTC_IER register does not work
4949	Reset and Boot: Device may not exit the power on reset (POR) event correctly with fast ramp-up slew rates.
5130	SAI: Under certain conditions, the CPU cannot reenter STOP mode via an asynchronous interrupt wakeup event
3981	SDHC: ADMA fails when data length in the last descriptor is less or equal to 4 bytes
3982	SDHC: ADMA transfer error when the block size is not a multiple of four
4624	SDHC: AutoCMD12 and R1b polling problem
3977	SDHC: Does not support Infinite Block Transfer Mode
4627	SDHC: Erroneous CMD CRC error and CMD Index error may occur on sending new CMD during data transfer
3980	SDHC: Glitch is generated on card clock with software reset or clock divider change

Table continues on the next page...

Errata ID	Errata Title
3983	SDHC: Problem when ADMA2 last descriptor is LINK or NOP
3978	SDHC: Software can not clear DMA interrupt status bit after read operation
3984	SDHC: eSDHC misses SDIO interrupt when CINT is disabled
4218	SIM/FLEXBUS: SIM_SCGC7[FLEXBUS] bit should be cleared when the FlexBus is not being used.
6029	SIM: The System Integration Module Registers may not be programmed correctly.
5708	SLCD: LCD waveforms can exceed voltage specification for 3V or 5V glass
5952	SMC: Wakeup via the LLWU from LLS/VLLS to RUN to VLPR incorrectly triggers an immediate wakeup from the next low power mode entry
3928	TSI: Delta voltage is 400 mV instead of 600 mV
3927	TSI: TSI will scan continuously if only one electrode is enabled
3926	TSI: The TSI will run several scan cycles during reference clock instead of scanning each electrode once
2638	TSI: The counter registers are not immediately updated after the EOSF bit is set.
4546	TSI: The counter values reported from TSI increase when in low power modes (LLS, VLLS1, VLLS2, VLLS3)
4935	UART: CEA709.1 features not supported
2582	UART: Flow control timing issue can result in loss of characters
4945	UART: ISO-7816 T=1 mode receive data format with a single stop bit is not supported
3892	UART: ISO-7816 automatic initial character detect feature not working correctly
5928	USBOTG: USBx_USBTRC0[USBRESET] bit does not operate as expected in all cases
3964	When debug is active a wakeup from STOP or VLPS with interrupt causes a hard fault interrupt.

e4588: DMAMUX: When using PIT with "always enabled" request, DMA request does not deassert correctly

Errata type: Errata

Description: The PIT module is not assigned as a stand-alone DMA request source in the DMA request mux. Instead, the PIT is used as the trigger for the DMAMUX periodic trigger mode. If you want to use one of the PIT channels for periodic DMA requests, you would use the periodic trigger mode in conjunction with one of the "always enabled" DMA requests. However, the DMA request does not assert correctly in this case.

Instead of sending a single DMA request every time the PIT expires, the first time the PIT triggers a DMA transfer the "always enabled" source will not negate its request. This results in the DMA request remaining asserted continuously after the first trigger.

Workaround: Use of the PIT to trigger DMA channels where the major loop count is greater than one is not recommended. For periodic triggering of DMA requests with major loop counts greater than one, we recommended using another timer module instead of the PIT.

If using the PIT to trigger a DMA channel where the major loop count is set to one, then in order to get the desired periodic triggering, the DMA must do the following in the interrupt service routine for the DMA_DONE interrupt:

1. Set the DMA_TCDn_CSR[DREQ] bit and configure DMAMUX_CHCFGn[ENBL] = 0

2. Then again DMAMUX_CHCFGn[ENBL] = 1, DMASREQ=channel in your DMA DONE interrupt service routine so that "always enabled" source could negate its request then DMA request could be negated.

This will allow the desired periodic triggering to function as expected.

e5751: FTFx: Launching the Read 1's Section command (RD1SEC) on an entire flash block results in access error (ACCER).

Errata type: Errata

Description: FTFx: Launching the Read 1's Section command on an entire flash block (i.e. with flash address = flash block base address & number of longwords = total number of longwords in the flash block) results in an incorrectly asserted access error (ACCER).

Workaround: To verify an entire flash block, use the Read 1's Block command. Use the Read 1's Section command only to verify sections that are smaller than an entire flash block.

e5706: FTFx: MCU security is inadvertently enabled (secured) if a mass erase is executed when the flash blocks/halves are swapped. This issue only affects applications that use the flash swap feature.

Errata type: Errata

Description: When the logical addresses of the flash blocks (halves) are swapped via the flash swap control command sequence and a mass erase is executed (via the MDM-AP or EzPort), the MCU security can go from un-secure to secure. Thus, when using a debugger to erase the entire flash memory and re-download a software application, the debugger may report that the device is secure after the erase completes. This issue only affects applications that use the flash swap feature.

Workaround: Issue the mass erase request (via the MDM-AP or EzPort) a second time to un-secure the device.

e2793: I2C: MCU does not wake as expected from STOP or VLPS mode on subsequent address matches if previous address is mismatched

Errata type: Errata

Description: The I2C module, acting as a slave on the I2C bus, does not wake as expected from normal STOP mode or VLPS mode on a valid address match if the previous address was not a match.

When the external I2C master sends a non-matching address, the I2C slave state machine does not look for a start bit past the first start bit on the bus. Consequently, subsequent transmissions by the I2C master with a matching address do not, on the first matching address, wake the MCU from stop mode or VLPS via the I2C interrupt.

Workaround: There are multiple workarounds:

(1) The master must continually re-transmit the MCU's slave address upon not receiving a NACK from the slave device during the slave addressing phase of the transmission. For clarification, the master must perform the following:

a) Send slave device address

b) Check for ACK bit

c) If ACK was received, continue with data transmission. Else, send repeated start signal and repeat steps a-c.

NOTE: Due to the nature of the errata, the maximum number of retransmissions needed to wake the part is nine times.

(2) When the MCU, operating as an I2C slave, is in STOP or VLPS mode: Ensure that the external I2C master sends a matching address to wake the slave MCU before it sends any transaction to other I2C slaves. The user must also ensure that MCU does not return to STOP or VLPS until after all packets to non-matching addresses have been sent.

(3) Use a pin interrupt (any pin, whether that pin is or is not being used by the active I2C module) to wake up the part before receiving I2C packets. NOTE: If using the SDA or SCL pin that the active I2C module is using, the part will wake-up on every I2C transaction on the bus.

(4) Use Wait mode instead of STOP or VLPS mode.

e4590: MCG: Transitioning from VLPS to VLPR low power modes while in BLPI clock mode is not supported.

Errata type: Errata

Description: Transitioning from VLPS mode back to VLPR (LPWUI control bit = 0) while using BLPI clock mode only, is not supported. During Fast IRC startup, the output clock frequency may exceed the maximum VLPR operating frequency. This does not apply to the BLPE clock mode.

Workaround: There are two options for workarounds

a) Exit to Run instead of VLPR. Before entering VLPR set the LPWUI bit so that when exiting VLPS mode the MCU exits to RUN mode instead of VLPR mode. With LPWUI set any interrupt will exit VLPR or VLPS back into RUN mode. To minimize the impact of the higher RUN current re-enter VLPR quickly.

or

b) Utilize MCG clock mode BLPE when transitioning from VLPS to VLPR modes.

e4481: PMC: STOP mode recovery unstable

Errata type: Errata

Description: Recovery from STOP mode is not guaranteed if STOP mode is used for a period of time longer than 50ms.

Workaround: There are two methods that can be used:

1. Set the BGEN bit in the PMC_REGSC register prior to entering STOP mode, and when existing STOP mode clear the BGEN bit.

2. Use a different low power mode such as VLPS.

e4638: PMC: VLLSx mode current draw at cold can exceed maximum specification at cold

Errata type: Errata

Description: When operating below -20C and above 3.4V in a VLLSx mode, current consumption can behave non-linearly and exceed maximum specification at cold. Current draw may approach maximum specification at hot.

Workaround: Limit operating temperature to -20C or greater or keep operating voltage below 3.4V, otherwise design power supply scheme should account for maximum specification as specified for hot.

e5667: PMC: When used as an input to ADC or CMP modules, the PMC bandgap 1-V voltage reference is not available in VLPx, LLS, or VLLSx modes

Errata type: Errata

Description: The Power Management Controller (PMC) bandgap 1-V reference is not available as an input to the Analog-to-Digital Converter (ADC) module (using ADC input channel AD27) or the Comparator (CMP) module (using CMP input IN6) in Very Low Power Run (VLPR), Very Low Power Wait (VLPW), Very Low Power Stop (VLPS), Low Leakage Stop (LLS), Very Low Leakage Stop3 (VLLS3), Very Low Leakage Stop2 (VLLS2), Very Low Leakage Stop1 (VLLS1), or Very Low Leakage Stop0 (VLLS0) modes.

This erratum does not apply to the VREF module 1.2 V reference voltage.

Workaround: Use of the PMC bandgap 1-V reference voltage as an input to the ADC and CMP modules requires the MCU to be in Run, Wait, or Stop modes.

e5138: RTC: The RTC_WAKEUP pin does not operate as specified and the WPON bit in RTC_IER register does not work

Errata type: Errata

Description: This errata only applies to devices that contain the RTC_WAKEUP pin. When an ALARM occurs and this pin is asserted, it is quickly de-asserted when MCU VDD level reaches the POR threshold. In addition, the WPON bit in the RTC_IER register which controls the state of the RTC_WAKEUP pin has no affect, and setting or clearing this bit will not change the state of the RTC_WAKEUP pin.

Only the RTC ALARM interrupt will assert the RTC_WAKEUP pin and a pulse will be generated when the ALARM occurs. If MCU VDD is present the RTC_WAKEUP pin will not remain asserted.

Workaround: For some cases it may be necessary to use an additional GPIO in order to control external circuits. For example, if using an external FET to control MCU VDD, an additional GPIO which asserts is required in order to maintain control of the external FET. This will be corrected on future revisions.

e4949: Reset and Boot: Device may not exit the power on reset (POR) event correctly with fast ramp-up slew rates.

Errata type: Errata

Description: Device may not exit the power on reset (POR) event correctly when the Vdd ramp-up slew rate is greater than 17 kV/sec as VDD is raised from 0V to 1.7V.

Workaround: Keep instantaneous slew rate of VDD below 17 kV/sec.

Status: This errata will be fixed on future mask sets.

e5130: SAI: Under certain conditions, the CPU cannot reenter STOP mode via an asynchronous interrupt wakeup event

Errata type: Errata

Description: If the SAI generates an asynchronous interrupt to wake the core and it attempts to reenter STOP mode, then under certain conditions the STOP mode entry is blocked and the asynchronous interrupt will remain set.

This issue applies to interrupt wakeups due to the FIFO request flags or FIFO warning flags and then only if the time between the STOP mode exit and subsequent STOP mode reentry is less than 3 asynchronous bit clock cycles.

Workaround: Ensure that at least 3 bit clock cycles elapse following an asynchronous interrupt wakeup event, before STOP mode is reentered.

e3981: SDHC: ADMA fails when data length in the last descriptor is less or equal to 4 bytes

Errata type: Errata

Description: A possible data corruption or incorrect bus transactions on the internal AHB bus, causing possible system corruption or a stall, can occur under the combination of the following conditions:

1. ADMA2 or ADMA1 type descriptor

2. TRANS descriptor with END flag

3. Data length is less than or equal to 4 bytes (the length field of the corresponding descriptor is set to 1, 2, 3, or 4) and the ADMA transfers one 32-bit word on the bus

4. Block Count Enable mode

Workaround: The software should avoid setting ADMA type last descriptor (TRANS descriptor with END flag) to data length less than or equal to 4 bytes. In ADMA1 mode, if needed, a last NOP descriptor can be appended to the descriptors list. In ADMA2 mode this workaround is not feasible due to ERR003983.

e3982: SDHC: ADMA transfer error when the block size is not a multiple of four

Errata type: Errata

Description: Issue in eSDHC ADMA mode operation. The eSDHC read transfer is not completed when block size is not a multiple of 4 in transfer mode ADMA1 or ADMA2. The eSDHC DMA controller is stuck waiting for the IRQSTAT[TC] bit in the interrupt status register.

The following examples trigger this issue:

1. Working with an SD card while setting ADMA1 mode in the eSDHC

2. Performing partial block read

3. Writing one block of length 0x200

4. Reading two blocks of length 0x22 each. Reading from the address where the write operation is performed. Start address is 0x512 aligned. Watermark is set as one word during read. This read is performed using only one ADMA1 descriptor in which the total size of the transfer is programmed as 0x44 (2 blocks of 0x22).

Workaround: When the ADMA1 or ADMA2 mode is used and the block size is not a multiple of 4, the block size should be rounded to the next multiple of 4 bytes via software. In case of write, the software should add the corresponding number of bytes at each block end, before the write is initialized. In case of read, the software should remove the dummy bytes after the read is completed.

For example, if the original block length is 22 bytes, and there are several blocks to transfer, the software should set the block size to 24. The following data is written/stored in the external memory:

4 Bytes valid data

4 Bytes valid data

4 Bytes valid data

4 Bytes valid data

4 Bytes valid data

2 Bytes valid data + 2 Byte dummy data

4 Bytes valid data

4 Bytes valid data

4 Bytes valid data

4 Bytes valid data

4 Bytes valid data

2 Bytes valid data + 2 Byte dummy data

In this example, 48 (24 x 2) bytes are transferred instead of 44 bytes. The software should remove the dummy data.

e4624: SDHC: AutoCMD12 and R1b polling problem

Errata type: Errata

Description: Occurs when a pending command which issues busy is completed. For a command with R1b response, the proper software sequence is to poll the DLA for R1b commands to determine busy state completion. The DLA polling is not working properly for the ESDHC module and thus the DLA bit in PRSSTAT register cannot be polled to wait for busy state completion. This is relevant for all eSDHC ports (eSDHC1-4 ports).

Workaround: Poll bit 24 in PRSSTAT register (DLSL[0] bit) to check that wait busy state is over.

e3977: SDHC: Does not support Infinite Block Transfer Mode

Errata type: Errata

Description: The eSDHC does not support infinite data transfers, if the Block Count register is set to one, even when block count enable is not set.

Workaround: The following software workaround can be used instead of the infinite block mode:

1. Set BCEN bit to one and enable block count

2. Set the BLKCNT to the maximum value in Block Attributes Register (BLKATTR) (0xFFFFfor 65535 blocks)

e4627: SDHC: Erroneous CMD CRC error and CMD Index error may occur on sending new CMD during data transfer

Errata type: Errata

Description: When sending new, non data CMD during data transfer between the eSDHC and EMMC card, the module may return an erroneous CMD CRC error and CMD Index error. This occurs when the CMD response has arrived at the moment the FIFO clock is stopped. The following bits after the start bit of the response are wrongly interpreted as index, generating the CRC and Index errors.

The data transfer itself is not impacted.

The rate of occurrence of the issue is very small, as there is a need for the following combination of conditions to occur at the same cycle:

- The FIFO clock is stopped due to FIFO full or FIFO empty
- The CMD response start bit is received

Workaround: The recommendation is to not set FIFO watermark level to a too small value in order to reduce frequency of clock pauses.

The problem is identified by receiving the CMD CRC error and CMD Index error. Once this issue occurs, one can send the same CMD again until operation is successful.

e3980: SDHC: Glitch is generated on card clock with software reset or clock divider change

Errata type: Errata

Description: A glitch may occur on the SDHC card clock when the software sets the RSTA bit (software reset) in the system control register. It can also be generated by setting the clock divider value. The glitch produced can cause the external card to switch to an unknown state. The occurrence is not deterministic.

Workaround: A simple workaround is to disable the SD card clock before the software reset, and enable it when the module resumes the normal operation. The Host and the SD card are in a master-slave relationship. The Host provides clock and control transfer across the interface. Therefore, any existing operation is discarded when the Host controller is reset.

The recommended flow is as follows:

1. Software disable bit[3], SDCLKEN, of the System Control Register

2. Trigger software reset and/or set clock divider

3. Check bit[3], SDSTB, of the Present State Register for stable clock

4. Enable bit[3], SDCLKEN, of the System Control Register.

Using the above method, the eSDHC cannot send command or transfer data when there is a glitch in the clock line, and the glitch does not cause any issue.

e3983: SDHC: Problem when ADMA2 last descriptor is LINK or NOP

Errata type: Errata

Description: ADMA2 mode in the eSDHC is used for transfers to/from the SD card. There are three types of ADMA2 descriptors: TRANS, LINK or NOP. The eSDHC has a problem when the last descriptor (which has the End bit '1') is a LINK descriptor or a NOP descriptor.

In this case, the eSDHC completes the transfers associated with this descriptor set, whereas it does not even start the transfers associated with the new data command. For example, if a WRITE transfer operation is performed on the card using ADMA2, and the last descriptor of the WRITE descriptor set is a LINK descriptor, then the WRITE is successfully finished. Now, if a READ transfer is programmed from the SD card using ADMA2, then this transfer does not go through.

Workaround: Software workaround is to always program TRANS descriptor as the last descriptor.

e3978: SDHC: Software can not clear DMA interrupt status bit after read operation

Errata type: Errata

Description: After DMA read operation, if the SDHC System Clock is automatically gated off, the DINT status can not be cleared by software.

Workaround: Set HCKEN bit before starting DMA read operation, to disable SDHC System Clock auto-gating feature; after the DINT and TC bit received when read operation is done, clear HCKEN bit to re-enable the SDHC System Clock auto-gating feature.

e3984: SDHC: eSDHC misses SDIO interrupt when CINT is disabled

Errata type: Errata

Description: An issue is identified when interfacing the SDIO card. There is a case where an SDIO interrupt from the card is not recognized by the hardware, resulting in a hang.

If the SDIO card lowers the DAT1 line (which indicates an interrupt) when the SDIO interrupt is disabled in the eSDHC registers (that is, CINTEN bits in IRQSTATEN and IRQSIGEN are set to zero), then, after the SDIO interrupt is enabled (by setting the CINTEN bits in IRQSTATEN and IRQSIGEN registers), the eSDHC does not sense that the DAT1 line is low. Therefore, it fails to set the CINT interrupt in IRQSTAT even if DAT1 is low.

Generally, CINTEN bit is disabled in interrupt service.

The SDIO interrupt service steps are as follows:

1. Clear CINTEN bit in IRQSTATEN and IRQSIGEN.

2. Reset the interrupt factors in the SDIO card and write 1 to clear the CINT interrupt in IRQSTAT.

3. Re-enable CINTEN bit in IRQSTATEN and IRQSIGEN.

If a new SDIO interrupt from the card occurs between step 2 and step 3, the eSDHC skips it.

Workaround: The workaround interrupt service steps are as follows:

1. Clear CINTEN bit in IRQSTATEN and IRQSIGEN.

2. Reset the interrupt factors in the SDIO card and write 1 to clear CINT interrupt in IRQSTAT.

3. Clear and then set D3CD bit in the PROCTL register. Clearing D3CD bit sets the reverse signal of DAT1 to low, even if DAT1 is low. After D3CD bit is re-enabled, the eSDHC can catch the posedge of the reversed DAT1 signal, if the DAT1 line is still low.

4. Re-enable CINTEN bit in IRQSTATEN and IRQSIGEN.

e4218: SIM/FLEXBUS: SIM_SCGC7[FLEXBUS] bit should be cleared when the FlexBus is not being used.

Errata type: Errata

Description: The SIM_SCGC7[FLEXBUS] bit is set by default. This means that the FlexBus will be enabled and come up in global chip select mode.

With some code sequence and register value combinations the core could attempt to prefetch from the FlexBus even though it might not actually use the value it prefetched. In the case where the FlexBus is unconfigured, this can result in a hung bus cycle on the FlexBus.

Workaround: If the FlexBus is not being used disabled the clock to the FlexBus during chip initialization by clearing the SIM_SCGC7[FLEXBUS] bit.

If the FlexBus will be used, then enable at least one chip select as early in the chip initialization process as possible.

e6029: SIM: The System Integration Module Registers may not be programmed correctly.

Errata type: Errata

Description: The following System Integration Modules Registers may not be programmed correctly: the FAMID and PINID bit fields in the SIM_SDID Register, the RAMSIZE in the SIM_SOPT1 Register, the NVMSIZE, PFSIZE and EESIZE in SIM_FCFG1 Register and information in the Unique ID Registers SIM_UIDx.

Workaround: Production, MC-qualified, devices will have these values programmed correctly.

e5708: SLCD: LCD waveforms can exceed voltage specification for 3V or 5V glass

Errata type: Errata

Description: The LCD controller power supply can be sourced using VDD, internal regulated voltage VIREG, or an external supply on the VLL3. Using the internal Vireg (VSUPPLY[1:0] = 11, LCD_GCR [RVEN] = 1, and LCD_GCR[CPSEL] =1) to generate the LCD bias voltages can cause the generated LCD waveform voltages to go out of specification for 3V and 5V glass. For LCD_GCR[HREFSEL] = 0, Vireg = 1V, but bias voltages can exceed specificationVLL1 > 1V, VLL2 > 2V, and VLL3 >3V. For LCD_GCR[HREFSEL] = 1 Vireg = 1.67V, but the bias voltages can exceed specification VLL1>1.67, VLL2 >3.3V, and VLL3>5V.

Workaround: Use an alternate LCD power supply configuration.

1. Vdd can be used as the LCD controller power supply.

a. For VSUPPLY[1:0] = 00 and LCD_GCR[CPSEL1] = 1, Vdd is used to drive VLL2. For 3V glass Vdd must be 2V and for 5V glass Vdd must be 3.3V.

b. For VSUPPLY[1:0] = 01 and LCD_GCR[CPSEL1] = 1, Vdd is used to drive VLL3. For 3V glass Vdd must be 3V and for 5V glass Vdd must be 5V.

2. Drive VLL3 with an external supply VSUPPLY[1:0] = 11 and LCD_GCR [RVEN] = 0.

a. For 3V glass VLL3 must equal 3V. The resistor bias network or charge pump can be used to generate VLL1 and VLL2. Note, VLL3 should never be externally driven to any level other than VDD.

e5952: SMC: Wakeup via the LLWU from LLS/VLLS to RUN to VLPR incorrectly triggers an immediate wakeup from the next low power mode entry

Errata type: Errata

Description: Entering VLPR immediately after an LLWU wakeup event from LLS/VLLS, will cause any subsequent entry into LLS/VLLS to fail if entry into VLPR mode occurs before clearing the pending LLWU interrupt.

Workaround: After an LLWU wakeup event from LLS/VLLS, the user must clear the LLWU interrupt prior to entering VLPR mode.

e3928: TSI: Delta voltage is 400 mV instead of 600 mV

Errata type: Errata

Description: Currently the delta voltage for the TSI channels is nominally 400mV. On future revisions the delta voltage will be changed to 600mV.

Workaround: Customers should account for this change in specification during their evaluations.

e3927: TSI: TSI will scan continuously if only one electrode is enabled

Errata type: Errata

Description: TSI will scan continuously if only one electrode is enabled even if a scan period using AMCLKS, AMPSC and SMOD has been defined.

Workaround: 1. If the system has an unused TSI pin, enable that electrode as a dummy electrode and configure the scanning period to half of the desired period. This will give half of the period for the single used electrode and half for the dummy electrode.

2. If no extra TSI pin is available to use as a "dummy" electrode, trigger scans with software using SWTS bit and control timing with an additional timer (RTC, MTIM, etc.)

e3926: TSI: The TSI will run several scan cycles during reference clock instead of scanning each electrode once

Errata type: Errata

Description: The TSI will run several scan cycles during reference clock instead of scanning each electrode once. For each automatic scanning period determined by AMCLKS (clock source), AMPSC (prescaler) and SMOD (period modulo), TSI will scan during one reference clock cycle divided by the AMPSC prescaler.

This does not affect the count result from TSI because TSI counters keep the last scan result.

Workaround: 1. Because counter results are not affected, a simple workaround is to use the smallest prescaler possible and use a bigger SMOD value, this will minimize the number of extra scans, thus also minimizing the amount of average extra current used by the module.

2. If strict control of number of scan cycles is needed, trigger scans with software control (using the SWTS bit) and control time between scans with a separate timer. This solution is only recommended if strict control of scan cycles is needed, if not, recommendation is to use workaround 1.

e2638: TSI: The counter registers are not immediately updated after the EOSF bit is set.

Errata type: Errata

Description: The counter registers are not immediately updated after the end of scan event (EOSF is set). The counter registers will become available 0.25 ms after the EOSF flag is set. This also applies for the end-of-scan interrupt, as it is triggered with the EOSF flag. This behavior will occur both in continuous scan and in software triggered scan modes.

Workaround: Insert a delay of 0.25 ms or greater prior to accessing the counter registers after an end of scan event or an end of scan interrupt that is triggered by the EOSF flag. This delay does not need to be a blocking delay, so it can be executing other actions before reading the counter registers. Notice that the out-of-range flag (OUTRGF) and interrupt occur after the counters have been updated, so if the OUTRGF flag is polled or the out-of-range interrupt is used, the workaround is not necessary.

e4546: TSI: The counter values reported from TSI increase when in low power modes (LLS, VLLS1, VLLS2, VLLS3)

Errata type: Errata

Description: When the MCU goes into LLS or VLLSx modes, with the TSI enabled for wakeup, the counter value reported by the TSI increases with respect to what was reported in active mode. Because the wakeup threshold is calculated in active mode, it is highly likely that MCU will wakeup immediately after going to low power.

Workaround: 1. Use Wait, Stop, or VLPS. These modes do not require any wakeup threshold calibration as TSI remains in active mode and wakes up each end of scan so that normal baseline tracking algorithm can be used.

2. To use LLS or VLLSx modes with the TSI as a wakeup source, calibrate the wakeup threshold using the desired low power mode. During application initialization, configure the TSI to exit low power via the LLWUI (low-leakage wake-up interrupt) with an End of Scan using the desired wakeup electrode. For example enter LLS mode with automatic scanning enabled so that after the first scan the TSI module causes an exit from low power at the end of scan. After the wakeup event, read the TSIx_WUCNTR Register, this register will have the value for the count during low power mode. Use this value to calculate THRSHLD register value.

e4935: UART: CEA709.1 features not supported

Errata type: Errata

Description: Due to some issues that affect compliance with the specification, the CEA709.1 features of the UART module are not supported. Normal UART mode, IrDA, and ISO-7816 are unaffected.

Workaround: Do not use the UART in CEA709.1 mode.

e2582: UART: Flow control timing issue can result in loss of characters

Errata type: Errata

Description: When /RTS flow control signal is used in receiver request-to-send mode, the /RTS signal is negated if the number of characters in the Receive FIFO is equal to or greater than the receive watermark. The /RTS signal will not negate until after the last character (the one that makes the condition for /RTS negation true) is completely received and recognized. This creates a delay between the end of the STOP bit and the negation of the /RTS signal. In some cases this delay can be long enough that a transmitter will start transmission of another character before it has a chance to recognize the negation of the /RTS signal (the /CTS input to the transmitter).

Workaround: For UARTs that implement an eight entry FIFO: When the FIFO is enabled, the receive watermark should be set to seven or less. This will ensure that there is space for at least one more character in the FIFO when /RTS negates. So in this case no data would be lost.

For UARTs without a FIFO (or if the FIFO is disabled): Delay might need to be added between characters on the transmit side in order to allow time for the negation of /RTS to be recognized before the next character is sent.

e4945: UART: ISO-7816 T=1 mode receive data format with a single stop bit is not supported

Errata type: Errata

Description: Transmission of ISO-7816 data frames with single stop bit is supported in T=1 mode. Currently in order to receive a frame, two or more stop bits are required. This means that 11 ETU reception based on T=1 protocol is not supported. T=0 protocol is unaffected.

Workaround: Do not send T=1, 11 ETU frames to the UART in ISO-7816 mode. Use 12 ETU transmissions for T=1 protocol instead.

e3892: UART: ISO-7816 automatic initial character detect feature not working correctly

Errata type: Errata

Description: The ISO-7816 automatic initial character detection feature does not work. The direct convention initial character can be detected correctly, but the inverse convention initial character will only be detected if the S2[MSBF] and S2[RXINV] bits are set. This defeats the purpose of the initial character detection and automatic configuration of the S2[MSBF], S2[RXINV], and C3[TXINV] bits.

Workaround: Use software to manually detect initial characters. Configure the UART with S2[MSBF] and S2[RXINV] cleared. Then check UART receive characters looking for 0x3B or 0x03. If 0x3B is received, then the connected card is direct convention. If 0x03 is received, then the connected card is inverse convention. If an inverse convention card is detected, then software should set S2[MSBF], S2[RXINV], and C3[TXINV].

e5928: USBOTG: USBx_USBTRC0[USBRESET] bit does not operate as expected in all cases

Errata type: Errata

Description: The USBx_USBTCR0[USBRESET] bit is not properly synchronized. In some cases using the bit can cause the USB module to enter an undefined state.

Workaround: Do not use the USBx_USBTCR0[USBRESET] bit. If USB registers need to be written to their reset states, then write those registers manually instead of using the module reset bit.

e3964: When debug is active a wakeup from STOP or VLPS with interrupt causes a hard fault interrupt.

Errata type: Errata

Description: When exiting STOP or VLPS back into RUN mode with an interrupt a hard fault interrupt is caused when the JTAG debuger is enabled.

The MCU enters a pseudo STOP mode when the debugger is enabled.

The user cannot use the debugger to test code that wakes up from STOP with an interrupt.

Workaround: a. Disable the debugger with a Power off and on cycle before testing code that exits STOP or VLPS with an interrupt.

or

b. From the debugger, while in STOP or VLPS, halt the MCU with the debugger tools before triggering an interrupt.

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