ES_PF8100_PF8200_2

Errata sheet for PF8100, PF8200

Rev. 2 — 11 August 2020 **Errata sheet**

Document information

Information	Content
Keywords	PF8100, PF8200
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table.

Table 1. Revision history

Rev	Date	Description
2	20200811	• Updated ER101 as per CIN 202008022I
1	20191127	• Initial release (ER101)

1 Product identification

This errata document applies to PF8100 and PF8200 identified in the following table.

Table 2. Revision overview

Revision ID	Part number	Package	Device marking
C1	MC33PF8100xxES (xx represents all OTP versions of this device)	56-pin 8 x 8 mm QFN	MC33PF8100xxES
C1	MC33PF8200xxES (xx represents all OTP versions of this device)	56-pin 8 x 8 mm QFN	MC33PF8200xxES

1.1 Device build information / date code

The marked trace code is the link between the physically marked materials and the manufacturing lot's system genealogy information. Once the connection between the marked material and system genealogy information is made, traceability reports provide the material's manufacturing/shipping history. All devices listed in the errata sheet are affected unless specific date codes are provided.

2 Errata overview

Table 3. Errata summary table

Erratum ID	Short description	Severity level [1][2][3][4]	Work-around	Product version	Detailed description
ER101	Output overshoot/undershoot when enabling another regulator	Medium	Yes	C1	Section 3.1

[1] High: Failure mode that severely inhibits the use of the device for all or a majority of intended applications
[2] Medium: Failure mode that might restrict or limit the use of the device for all or a majority of intended applications
[3] Low: Unexpected behavior that does not cause significant problems for the intended applications of the device
[4] Enhancement: Improvement made to the device due to previously found issues on the design

3 Functional problems detail

3.1 ER101: Output overshoot/undershoot when enabling another regulator

3.1.1 Severity level

Medium

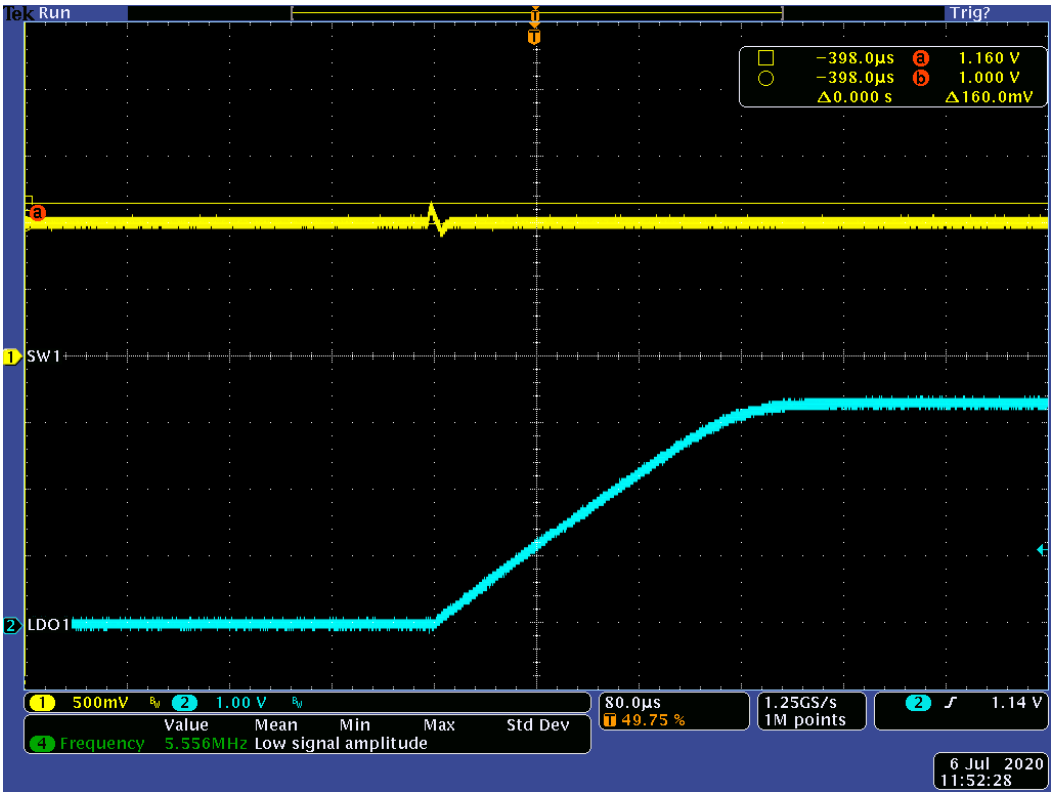
3.1.2 Problem

Overshoot observed on SW1, SW5 and SW7 when a specific regulator is enabled after the respective switching regulator.

The specific interactions are as follows:

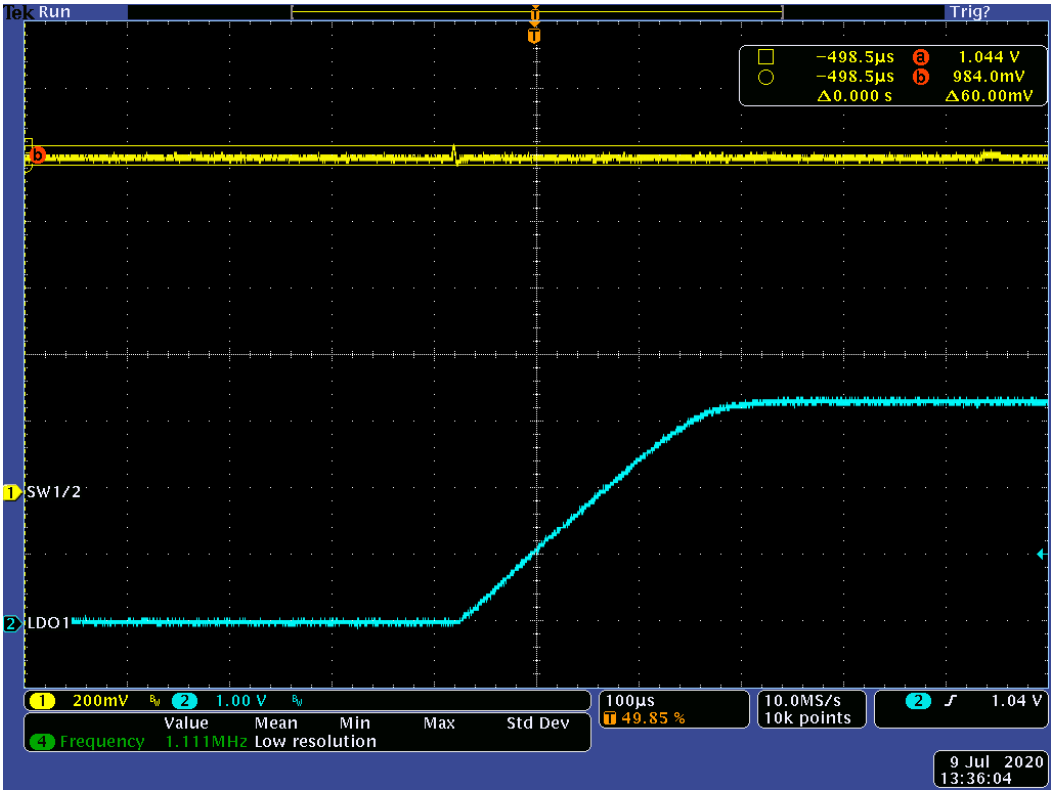
- SW1 is affected, when LDO1 is enabled (aggressor)
- SW5 is affected, when LDO3 is enabled (aggressor)
- SW6 is affected, when SW7 is enabled (aggressor)

When the affected regulator is using the default output capacitance (2 × 44 µF), the overshoot / undershoot can be as high as ±200 mV. The overshoot / undershoot occurs only when the OV/UV monitor of the aggressor is enabled, therefore it can occur during the power-up sequence when the aggressor is turned On at a slot greater than the affected regulator, or during normal operation if the OV/UV monitor of the aggressor is enabled while the affected regulator is already On.



When the affected regulator is configured in dual phase, turning On the aggressor creates a glitch at the output of the affected phase, however, the second phase helps to mitigate the impact causing only around 52 mV (peak to peak) glitch on the regulator output when using the nominal capacitance 4 x 22 µF.

Triple phase and quad phase configurations are not significantly affected by this condition.



3.1.3 Root cause

The PF8x00 uses a centralized bias generation block from which bias signals are routed to the respective blocks. Because of the high-density routing on PF8x00 device, some of the bias traces are too close to each other, causing induced noise to the nearby neighbors.

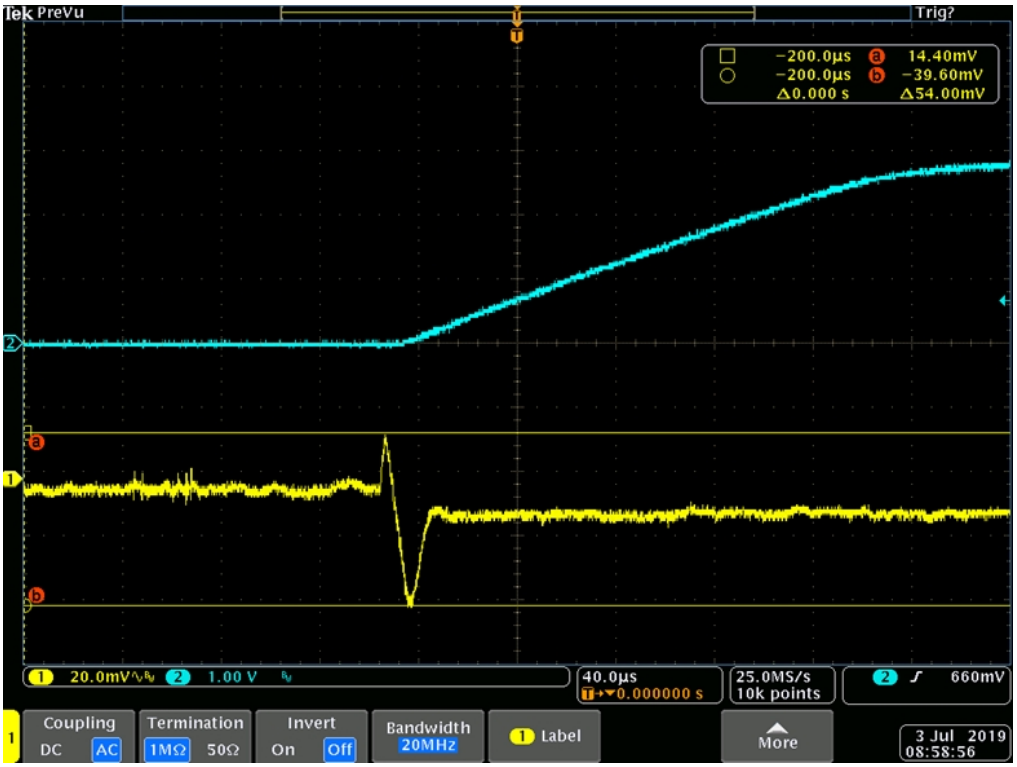
On production silicon C1, most of the conditions observed on B0 silicon are solved, however, we discovered the following interactions are still present:

- SW5 is affected by the bias trace of the OV/UV monitor of LDO3
- SW1 is affected by the bias trace of the OV/UV monitor of LDO1
- SW6 is affected by the bias trace of the OV/UV monitor of SW7

When the regulator is enabled, the OV/UV monitor is enabled as well, causing the inductive kick on the bias trace of the affected regulator, therefore creating the glitch at the output.

3.1.4 Work-around

1. The overshoot / undershoot is reduced with a higher output capacitance. The systems using PF8x00 PMIC to power the i.MX8 MCUs are already loading the switching regulators from 150 µF to 200 µF. Based on the characterization test, the overshoot / undershoot, gets reduced to a total ~55 mV (peak to peak) with an output capacitance of 150 µF.



2. Ensure that the aggressor is turned On before or in the same slot as the affected regulator.
   - If all LDOs are not used, avoid using LDO3 if it cannot meet this condition.
   - If all LDOs are not used, avoid using LDO1 if it cannot meet this condition.
3. Do not toggle the aggressor Off and On during normal operation.

3.1.5 Fix plan

No new silicon revision planned.

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