ES_P89LPC952

Errata sheet P89LPC952

Rev. 02 — 23 February 2010 **Errata sheet**

Document information

Info	Content
Keywords	P89LPC952 errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table at the end of the document.

Revision history

Rev	Date	Description
02	20100223	• The format of this errata sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Added “Revision identifier” column in Table 4.
01	20080718	Initial version.

Contact information

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1. Product identification

The P89LPC952 devices typically have the following top-side marking:

P89LPC952x x

xxxxxxx xx

xxYYWW R

The last letter in the last line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the P89LPC952:

Table 1. Device revision table

Revision identifier (R)	Revision description
'-'	Initial device revision
'A'	Second device revision
'B'	Third device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier
OCI.1	OCI debug information is lost after pin reset	'-'
INTERRUPTS.1	Interrupts are not handled in background during debug mode	'-', A, B
RESET.1	Internal reset is not driven out when debugging	'-'
CLOCK.1	Clock doubler bit UCFG1.3 is ignored	'-'
UART.1	Breakdetect trips after 10 zero bits	'-'
DIVM.1	Using DIVM in power-down mode	'-', A, B
I/O.1	Port 3.0 can be an output during a power-up cycle	'-'
ADC.1	Digital disable hook-up swapped	'-'
I/O.2	Port 5 can not be driven to 5V in open-drain mode	'-', A, B

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Revision identifier
IPD.1	Power down current increase	'-'

Table 4. Errata notes

Note	Short description	Revision identifier
V_{DD}.1	V_{DD} Power cycling	'-', A
IRC.1	Internal RC oscillator accuracy	'-', A, B

3. Functional problems detail

3.1 OCI.1: JTAG debug information is lost after pin reset

Introduction:

The LPC952 JTAG debugger has the capability to trace code execution. Trace can also be used through reset.

Problem:

On the first engineering samples marked with Rev - when a pin reset is generated the JTAG debug information is lost and also the Trace data prior to the pin reset.

Work-around:

No known workaround.

3.2 Interrupts.1: Interrupts are not handled in background during debug mode

Introduction:

The LPC952 JTAG debug interface has the capability to keep running interrupt service routines while the debug is stopped or single stepping. The servicing of interrupt service routines can either be enabled or disabled in XSFRs.

Problem:

On the first engineering samples of the LPC952 marked with Rev - the interrupt service routines are always turned off in debug mode.

Work-around:

No known workaround.

3.3 Reset.1: Internal reset is not driven out when debugging

Introduction:

The LPC952 will drive the external Reset pin low in debugging mode when any reset occurs. The resets that will cause the external reset pin to be driven low are a watchdog timer reset, a brownout reset and a software reset.

Problem:

On the first engineering samples of the LPC952 marked with Rev - the reset out feature does not function correctly.

Work-around:

No known workaround.

3.4 Clock.1: Clock doubler bit UCFG1.3 is ignored

Introduction:

The LPC952 has the option to double the clock of the internal RC oscillator from 7.37258 MHz to 14.745 MHz by setting the UCFG1.3 bit.

Problem:

On the first engineering samples of the LPC952 marked with Rev - the clock doubling feature does not function correctly.

Work-around:

No known workaround.

3.5 UART.1: Breakdetect trips after 10 zero bits

Introduction:

The UART on the LPC952 has the ability to detect a breakdetect signal, a break signal is a 11 bit long low signal on the RxD input of the UART.

Problem:

The breakdetect flag will be set after 10 low bits on the RxD input of the UART. When 9 bit mode is used and all 9 data bits are 0 and the start bit is zero this will be detected as a breakdetect.

Work-around:

No known workaround.

3.6 DIVM.1: Using DIVM in power-down mode

Introduction:

The LPC952 has a DIVM register that can be used to divide the clock down. Using DIVM can greatly reduce power when in active mode.

Problem:

When DIVM is used in active mode and power-down mode is then entered the LPC952 can not be waken up from power down mode.

Work-around:

Before entering powerdown mode set DIVM back to 0x00. This way the LPC952 will be operating full speed for one instruction before entering power-down mode. After the LPC952 has been waken up DIVM can be set back to its original value.

3.7 I/O.1: Port 3.0 can be an output during a power-up cycle

Introduction:

The LPC952 can be selected to be clocked by an internal RC oscillator. When the internal RC oscillator is selected, P3.0 and P3.1 (which would be used for the crystal oscillator circuit) pins can now be used as general purpose IO pins.

Problem:

When the LPC952 is powered up the configuration of the UCFG1 is read out and the LPC952 configured accordingly. The UCFG1 gets read out on the low brownout level of the LPC952 (typically around 2.3V). Before the UCFG1 is read out the crystal oscillator circuit might be enabled. When the crystal circuit is enabled P3.0 is driven to the inverse state of P3.1.

Work-around:

Please make sure your external circuitry connected to P3.0 is not affected by this behavior. Otherwise it is recommended to switch to a different port pin.

3.8 ADC.1: Digital disable hook-up swapped

Introduction:

The LPC952 has a 10-bit ADC. When using the ADC the digital inputs should be disabled to get the ADC accuracy specified in the datasheet.

Problem:

Digital input disable (enable analog input) for all 8 channels of the 10-bit A/D are swapped.

- AD00 disables digital input of AD04 and vice versa
- AD01 disables digital input of AD05 and vice versa
- AD02 disables digital input of AD06 and vice versa
- AD03 disables digital input of AD07 and vice versa.

Work-around:

If more than 1 channel selected, use the pair nibble bits together, meaning, if AD00 selected, select AD04 as the other A/D input. Similarly, AD01 with AD05, AD02 with AD06, AD03 with AD07. If an odd number of channels are used, then the remaining pin cannot be used as a digital input, but may be used as an output.

3.9 I/O.2: Port 5 can not be driven to 5V in open-drain mode

Introduction:

Port 5 has high current sourcing/sinking (20 mA) for all Port 5 pins. All other port pins have high sinking capability (20 mA).

Problem:

In open-drain mode, the Port 5 pins can not be pulled up to 5V, they can only be driven to Vdd+0.7V.

Work-around:

No known workaround.

4. AC/DC deviations detail

4.1 IPD.1: Power down current increase

Introduction:

The LPC952 can be put into power down mode by setting the power down bits in PCON. Total power down mode will typically consume less than 1uA.

Problem:

On the first engineering samples of the LPC952 marked with Rev - the typical power down current might be higher than the specified maximum of 5uA at high temperatures.

Work-around:

No known workaround.

5. Errata notes

5.1 V_{DD}.1: V_{DD} power cycling

To generate a proper Power-On-Reset (POR), V_{DD} must have dropped below 0.2V before being powered back up. Power-cycling without V_{DD} having dropped below 0.2V may result in incorrect Program Counter values.

5.2 IRC.1: Internal RC oscillator accuracy

To be able to guarantee the Internal RC oscillator accuracy over the full operating range the VDD supply has to be decoupled sufficiently. Sufficient decoupling is dependant on the noise level in the application, typically a 0.1uF should be sufficient for most applications.

Noise on the V_{DD} supply pins can cause the Internal RC oscillator to go slightly outside of the specified range.

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