ES_P89LPC9351

Errata sheet P89LPC9351

Rev. 02 — 8 March 2010 **Errata sheet**

Document information

Info	Content
Keywords	P89LPC9351 errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table at the end of the document.

Revision history

Rev	Date	Description
02	20100308	• The format of this errata sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Removed DIVM.1
01	20081203	Initial version.

Contact information

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1. Product identification

The P89LPC9351 devices typically have the following top-side marking:

P89LPC9351x x

xxxxxxx xx

xxYYWW R

The last letter in the last line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the P89LPC9351:

Table 1. Device revision table

Revision identifier (R)	Revision description
'-'	Initial device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier
ADC.1	Single Step mode multi channel boundary interrupt	'-'
PGA.1	PGA0 enabled by setting PGATRIM0 bit	'-'

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Revision identifier
-	-	-

Table 4. Errata notes

Note	Short description	Revision identifier
-	-	-

3. Functional problems detail

3.1 ADC.1: Single Step mode multi channel boundary interrupt

Introduction:

The ADC on the P89LPC9351 is an Analog to Digital converter with 8 bits of resolution. The ADC has features such as a Single Step mode where the ADC will step through the selected channels on each ADC start condition.

Problem:

When the ADC is in Single Step mode with more than 1 channel selected, and a boundary interrupt occurs to any of the lower selected channel-bits, a write to the ADMODA register to clear the BNDI bit before all the selected channels are converted will reset the channel selection counter and the ADC will go back and wait at the lowest selected channel for the next conversion. This applies to both ADC0 and ADC1 on the P89LPC9351.

Work-around:

1. Clear the lower channel bits including the boundary interrupted channel in ADCINS register before the next start request.
2. Use the default boundary channel, not clear BNDI bit until all channels are converted.

3.2 PGA.1: PGA0 enabled by setting PGATRIM0 bit

Introduction:

Register PGACON0 and PGACON0B are used for PGA0 configuration. In register PGACON0, ENPGA0 bit is used to enable PGA0. PGATRIM0 bit is used to enable PGA0 trim. If set, PGA0 is grounded for calibration mode.

Problem:

PGA0 is also enabled by setting PGATRIM0 bit. When disabling PGA0 by clearing ENPGA0 bit, PGA0 still functions. When entering power down mode or total power down mode, PGA module does not enter power down mode and will continue to consume power.

Work-around:

Make sure to clear both PGATRIM0 bit and ENPGA0 bit before entering power down mode or total power down mode. To disable PGA0, also make sure to clear both PGATRIM0 bit and ENPGA0 bit.

4. AC/DC deviations detail

No known errata

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