ERRATA SHEET

Date: **2008 Nov 07**
Document Release: **Version 1.2**
Device Affected: **P89LPC921**

This errata sheet describes both the functional deviations and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

NXP
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Identification:

The typical P89LPC921 devices have the following top-side marking:

P89LPC921x x

xxxxxxx xx

xxYYWW R

The last letter in the third line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the P89LPC921:

Revision Identifier (R)	Comment
'A'	Initial device revision
'B'	Updated device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

Errata Overview - Functional Problems

Functional Problem	Short Description	fixed in revision	added
DIVM.1	Using DIVM in power-down mode	none	v1.1
I/O.1	Port 3.0 can be an output during a power-up cycle	none	v1.1
ICP.1	ICP Global Erase	none	v1.0
RESET.1	External reset does not function correctly when using DIVM	none	v1.0
UART.1	Breakdetect trips after 10 zero bits	none	v1.1
I/O.2	Eight pins with high drive current can not be driven to 5V in open-drain mode	none	v1.2

Errata Overview - AC/DC Deviations

AC/DC Deviation	Short Description	fixed in revision	added
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Errata Notes

Note	Short Description	added
V_{DD}.1	V_{DD} Power cycling.	v1.1
IRC.1	Internal RC oscillator accuracy	v1.1

Functional Deviations of P89LPC921

DIVM.1: Using DIVM in power-down mode

Introduction: The LPC921 has a DIVM register that can be used to divide the cclk down. Using DIVM can greatly reduce power when in active mode.

Problem: When DIVM is used in active mode and power-down mode is then entered the LPC921 can not be waken up from power down mode.

Workaround: Before entering powerdown mode set DIVM back to 0x00. This way the LPC921 will be operating full speed for one instruction before entering power-down mode. After the LPC921 has been waken up DIVM can be set back to its original value.

I/O.1: Port 3.0 can be an output during a power-up cycle

Introduction: The LPC921 can be selected to be clocked by an internal RC oscillator. When the internal RC oscillator is selected, P3.0 and P3.1 (which would be used for the crystal oscillator circuit) pins can now be used as general purpose IO pins.

Problem: When the LPC921 is powered up the configuration of the UCFG1 is read out and the LPC921 configured accordingly. The UCFG1 gets read out on the low brownout level of the LPC921 (typically around 2.3V). Before the UCFG1 is read out the crystal oscillator circuit might be enabled. When the crystal circuit is enabled P3.0 is driven to the inverse state of P3.1.

Workaround: Please make sure your external circuitry connected to P3.0 is not affected by this behaviour. Otherwise it is recommended to switch to a different port pin.

ICP.1: ICP Global Erase

Introduction: The LPC921 can be programmed using ICP (In Circuit Programming). One of the ICP functions is the Erase Global command, which will erase the entire chip including the security bytes and configuration information.

Problem: When giving the Erase Global command through the ICP interface the LPC921 will not clear the busy flag and stay busy forever.

Workaround: The workaround can be done in 4 steps:

Step 1: Shift out the WR_FMCON command followed by the Erase Global opcode.

Step 2: Wait 5ms.

Step 3: Do 8 dummy reads with the RD_FMDATA_I command.

Step 4: Read FMCON until the busy flag gets cleared.

Please also see figure 1 on the following page.

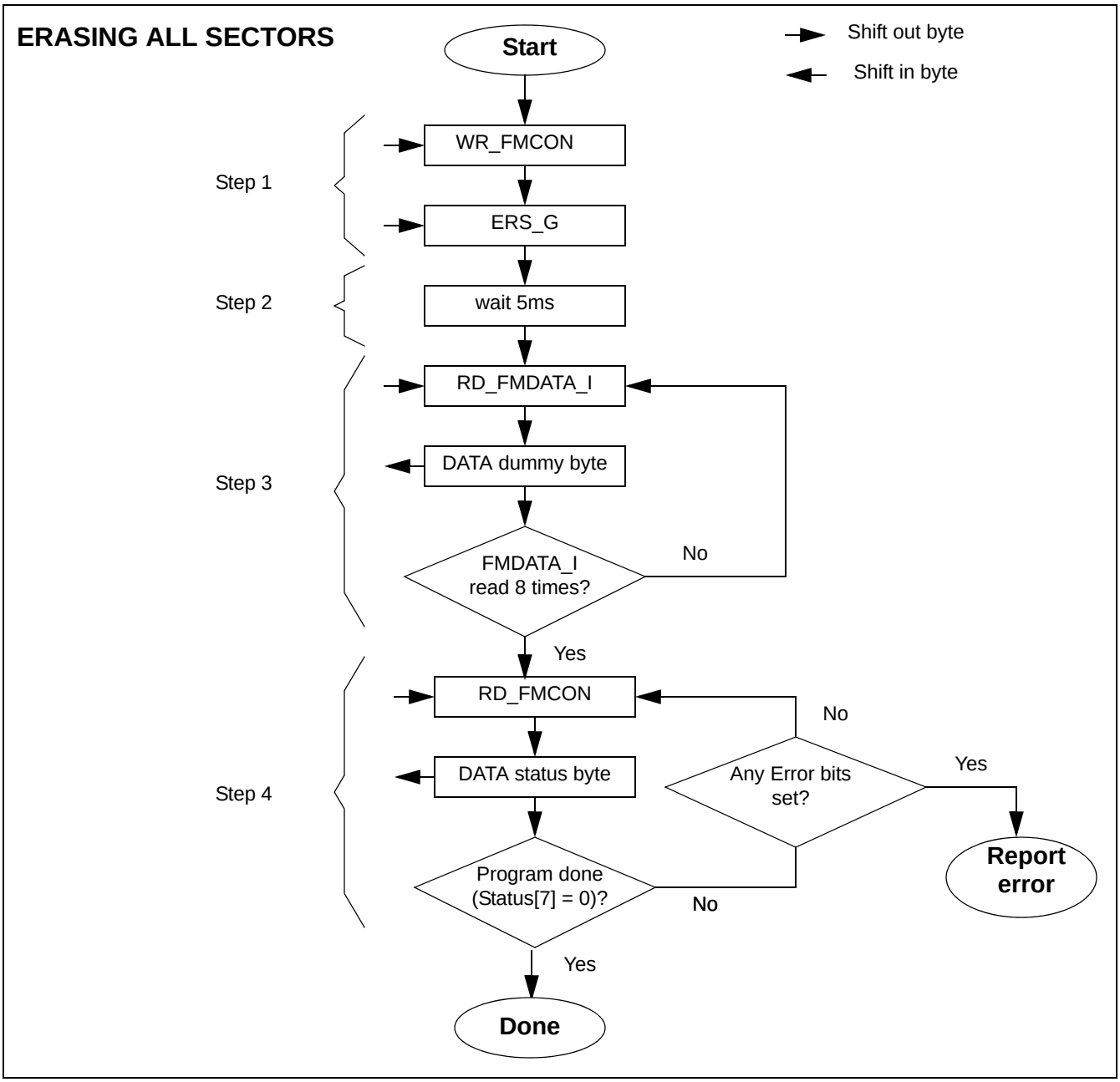

Figure 1: Flowchart ICP Global Erase

RESET.1: External reset does not function correctly when using DIVM

Introduction: The LPC921 can be set up to use either an internal reset or an external reset pin on P1.5. The DIVM register can be used to divide down the internal CCLK down.

Problem: When the LPC921 is configured to have an external reset pin on P1.5 and in the program the DIVM register is programmed to a value different from 0x00 to slow down CCLK, then the next reset pulse will not generate a proper reset for the LPC921. A power cycle has to be applied for the LPC921 to start up again properly.

Workaround: Use the internal reset function.

UART.1: Breakdetect trips after 10 zero bits

Introduction: The UART on the LPC921 has the ability to detect a breakdetect signal, a break signal is a 11 bit long low signal on the RxD input of the UART.

Problem: The breakdetect flag will be set after 10 low bits on the RxD input of the UART. When 9 bit mode is used and all 9 data bits are 0 and the start bit is zero this will be detected as a breakdetect.

Workaround: No known workaround.

I/O.2: Eight pins with high drive current can not be driven to 5V in open-drain mode

Introduction: High drive current (20 mA) on eight I/O pins (P0.3 to P0.7,P1.4, P1.6, P1.7). All other port pins have high sinking capability (20 mA).

Problem: In open-drain mode, the eight pins with high drive current can not be pulled up to 5V, only can be driven to Vdd+0.7V.

Workaround: No known workaround.

Electrical and Timing Specification Deviations of P89LPC921

No known erratas.

Errata Notes

V_{DD}.1: V_{DD} Power cycling

To generate a proper Power-On-Reset (POR), V_{DD} must have dropped below 0.2V before being powered back up. Power-cycling without V_{DD} having dropped below 0.2V may result in incorrect Program Counter values.

Please also see the V_{POR} specification in LPC921 Datasheet, DC electrical characteristics. Section 8.15 (Reset) states that during a power cycle, V_{DD} must fall below V_{POR}.

IRC.1: Internal RC oscillator accuracy

To be able to guarantee the Internal RC oscillator accuracy over the full operating range the V_{DD} supply has to be decoupled sufficiently. Sufficient decoupling is dependant on the noise level in the application, typically a 0.1uF should be sufficient for most applications.

Noise on the V_{DD} supply pins can cause the Internal RC oscillator to go slightly outside of the specified range.