ERRATA SHEET

Date: **2004 Aug 17**
Document Release: **Version 1.0**
Device Affected: **P89LPC932A1**

This errata sheet describes both the functional deviations and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

Philips Semiconductors

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Identification:

The typical P89LPC932A1 devices have the following top-side marking:

P89LPC932A1x x

xxxxxxx xx

xxYYWW R

The last letter in the third line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the P89LPC932A1:

Revision Identifier (R)	Comment
'A'	Initial device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

Errata Overview - Functional Problems

Functional Problem	Short Description	fixed in revision	added
CCU.1	CCU in Alternate output mode inverting	none	v1.0
CCU.2	CCU in Alternate output mode halting	none	v1.0
CCU.3	CCU PLL divider	none	v1.0
CCU.4	CCU capture reading ICRxH	none	v1.0
EEPROM.1	EEPROM lock-up on power up	none	v1.0

Errata Overview - AC/DC Deviations

AC/DC Deviation	Short Description	fixed in revision	added
-	-	-	-

Errata Notes

Note	Short Description	added
V_{DD}.1	V_{DD} Power cycling.	v1.0

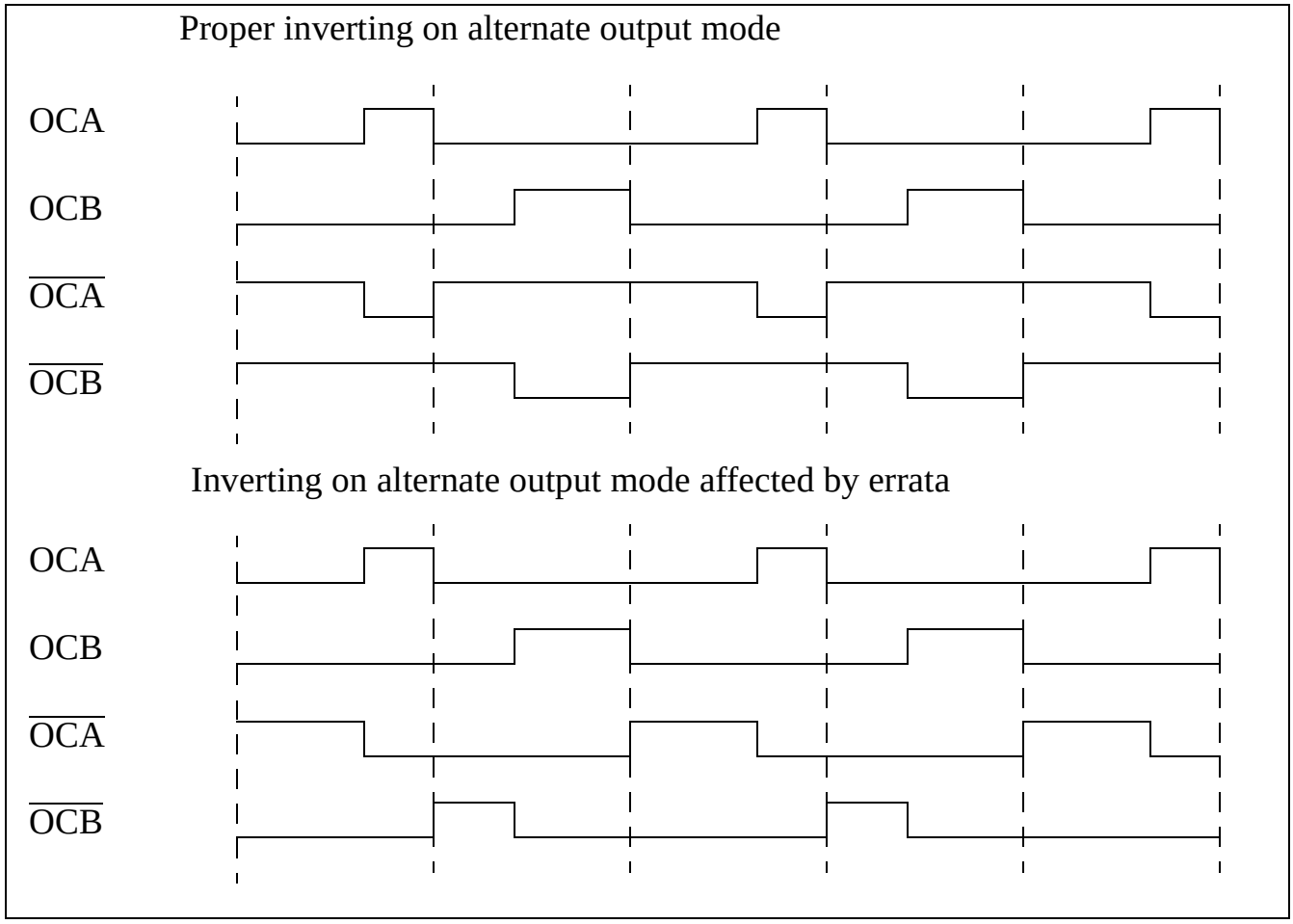
Functional Deviations of P89LPC932A1

CCU.1: CCU in Alternate output mode inverting

Introduction: The CCU in the LPC932A1 is the capture compare unit, which has the option to generate alternate output on 2 PWM signals.
All PWM signals can be inverted.

Problem: In the inactive state of the alternate output mode the inverted PWM signal is always low.

Workaround: No known workaround.

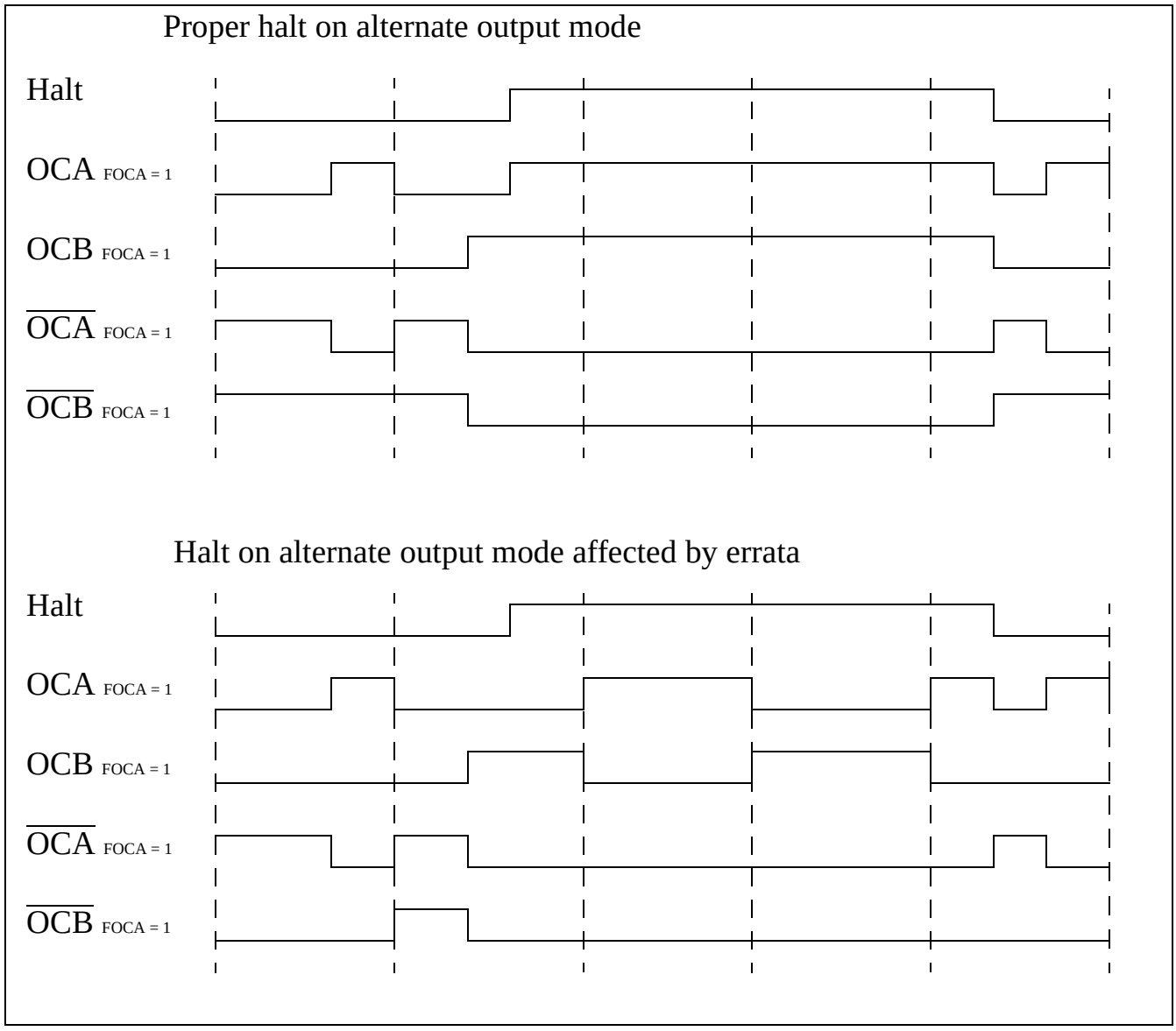


CCU.2: CCU in Alternate output mode halting

Introduction: The CCU in the LPC932A1 is the capture compare unit, which has the option to generate alternate output on 2 PWM signals. When a halt condition occurs all the PWM outputs go to the predefined state of FOCx.
All PWM signals can be inverted.

Problem: In the inactive state of the alternate output mode the inverted PWM signal is always low, even during a halt condition.

Workaround: No known workaround.



CCU.3: CCU PLL divider

Introduction: The CCU in the LPC932A1 is the capture compare unit, which has a PLL to boost the frequency of the CCU block. The PLL has an input range between 0.5 MHz and 1MHz. Different clock dividers such as the DIVM and PLLDIV can be used to get the desired input frequency to the PLL.

Problem: When the PLLDIV is selected to divide by 0, the PLL circuit does not lock and output the correct frequency.

Workaround: Use a different combination of DIVM and PLLDIV where PLLDIV is not 0.

CCU.4: CCU capture reading ICRxH

Introduction: The CCU in the LPC932A1 is the capture compare unit, which has the option to capture external signals on the ICA and ICB channels.
The capture event is read out in 2 registers the capture low register ICRxL and ICRxH.

Problem: When reading out ICRxH the data will not be correct, the data in ICRxH will be updated after ICRxH is read.

Workaround: Read ICRxH twice, the second read of the ICRxH will have the correct data.

EEPROM.1: EEPROM lock-up on power up

Introduction: The LPC932A1 has onboard data EEPROM, which allows to store non volatile data bytes on the LPC932A1 that will hold their value when the power is not applied to the LPC932A1.

Problem: With a slow rising VDD slower than 10ms there is a chance that the EERPOM circuitry will lock up, and incorrect data will be read out.

The EEPROM itself still has the correct data.

Workaround: The data EEPROM can be unlocked by a dummy write cycle. The following function shows a dummy write cycle.

```
void dummywrite(void)
{
  DEECON &= 0x0E;                 // EEPROM write mode
  DEEDAT = 0x5A;                  // dummy data
  DEEADR = 0x00;                  // dummy write address 0x000
  while(!(DEECON&0x80))           // wait till interrupt flag is set
  {
  }
}
```

Electrical and Timing Specification Deviations of P89LPC932A1

No known errata

Errata Notes

V_{DD}.1: V_{DD} Power cycling

To generate a proper Power-On-Reset (POR), V_{DD} must have dropped below 0.2V before being powered back up. Power-cycling without V_{DD} having dropped below 0.2V may result in incorrect Program Counter values.

Please also see the V_{POR} specification in LPC932A1 Datasheet, DC electrical characteristics. Section 8.15 (Reset) states that during a power cycle, V_{DD} must fall below V_{POR}.