ERRATA SHEET

Date: 2009 Apr 9
Document Release: Version 4.0
Device Affected: LPC2921FBD100, LPC2923FBD100, LPC2925FBD100

This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

NXP Semiconductors

founded by Philips

Document revision history

Rev	Date	Description
4.0	2009 April 9	Corrected revision identifier for EEPROM.1
3.0	2009 April 1	Added EEPROM.1
2.0	2009 February 12	Updated ESD.1
1.0	2009 January 27	First version

Identification

The typical LPC292XFBD100 devices have the following top-side marking:

LPC292XFBD100

xxxxxxx

xxYYWWR

The last letter in the third line (field ‘R’) will identify the device revision. This Errata Sheet covers the following revisions of the LPC292XFBD100:

Revision Identifier (R)	Comment
‘0’	Second device revision
‘(blank)’	Initial device revision

Field ‘YY’ states the year the device was manufactured. Field ‘WW’ states the week the device was manufactured during that year.

Errata Overview - Functional Problems

Functional Problem	Short Description	Device Revision the problem occurs in
EEPROM.1	The LPC292XFBD100 EEPROM were not trimmed at ESORT.	(blank), 0

Errata Overview - AC/DC Deviations

AC/DC Deviation	Short Description	Device Revision the deviation occurs in
ESD.1	The LPC292XFBD100 does not meet the NXP QRS ESD requirements on the $V_{DD(OSC\_PLL)}$ pin.	(blank)

Errata Notes

Notes	Short Description	Device Revision the note applies to
N/A	N/A	N/A

Functional problems

EEPROM.1 The LPC292XFBD100 EEPROM were not trimmed at ESORT.

Introduction: Program, erase, and readback of data from the EEPROM is not reliable at the specified 375 kHz speed.

Problem: Devices with date codes on or before 0909 exhibit this issue (actual package marking ZSG09090). For products with newer date codes the EEPROM are correctly trimmed.

Work around: Use devices with date codes after 0909.

AC/DC Deviations

ESD.1 The LPC292XFBD100 does not meet the NXP QRS ESD requirements on the $V_{DD(OSC\_PLL)}$ pin.

Introduction: The LPC292XFBD100 is rated for 2 kV ESD HBM. The $V_{DD(OSC\_PLL)}$ pin is the power supply pin for the oscillator circuit.

Problem: On devices with date codes before 0905, the LPC292XFBD100 does not meet the required 2 kV ESD HBM specification.

Work around: Observe proper ESD handling precautions for the LPC292XFBD100.