56F827

Chip Errata

DSP56F827 Digital Signal Controller

This document reports errata information on chip revision B. Errata numbers are in the form n.m, where n is the number of the errata item and m identifies the document revision number. This document is a pre-publication draft.
Note: **Differences between Chip Revisions are listed on page 4** and errata information for chip revisions prior to revision B have been archived and can be requested from Motorola Sales.

Chip Revision B Errata Information:

The following errata items apply only to Revision B 56F827 devices. These devices are marked as DSP56F827 or as PC56F827 with date codes of 0222 or later.

Errata Number	Description	Impact and Work Around
1.0	Writes to internal XRAM during the first cycle out of reset does not work properly.	Impact: Does not write to the XRAM during the first cycle out of reset. Work Around: To insert a NOP at the program entry point or move any other type of instruction onto the first location.
2.0	N register is not available in the cycle immediately after it is changed.	Impact: In the case of an index+ offset move into the N register, N is not available in the cycle immediately following the change in value. Example: move x:(r2+ 3), N lea (R2) +N Work Around: A no-operation (NOP) or some other instruction that does not use the N register will need to be inserted between the two statements. As an aid the assembler will be modified to flag this as a problem.
3.0	While in operation if TOD is disabled and the value written onto the TOD alarm registers happens to match with the value on the counters, a TOD alarm interrupt is raised.	Impact: Generates an interrupt even if TOD is not enabled. Work Around: When disabling TOD, also disable the TOD alarm bit. When using TOD, configure the alarm registers, wait for the first one second interrupt after enabling the TOD and then enable the alarm interrupt.

Chip Revision B Errata Information:

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Errata Number	Description	Impact and Work Around
4.3	A one second first alarm value causes an alarm interrupt after two seconds instead of one.	Impact: A one second first alarm value will cause an alarm interrupt after two seconds instead of one. The second occurrence of this alarm will trigger correctly. For example, if the initial day/hr/min/sec counters are set to zero and the alarm registers set to 1 second. Alarms will happen at 00:00:02, 00:01:01, 00:02:01, etc. Work Around: The SDK adds one second to the initial seconds counter time to cause the first alarm to occur after one second instead of two.
SSI Errata Items		
5.4	Under some conditions when using the FIFO, SSI misses an increment of the FIFO read index and erroneously retransmits the prior word.	Impact: Same as description. Work Around: The following procedure permits FIFO utilization and avoids the problem: a) Set watermark for 2 or more words left in TX FIFO when ISR triggers b) Before writing to FIFO, verify TFCNT $\geq$ 2 c) If TFCNT was $\geq$ 2, then write word to FIFO d) Repeat steps b and c to refill the FIFO e) If TFCNT was not $\geq$ 2, then don't make writes and instead disable the TFE ISR in the interrupt controller; wait for TUE to occur, let the TUR ISR handle the situation by reloading the FIFO, and re-enable the TFE ISR before exiting the TUE ISR.
6.4	Under some conditions, SSI can increment the FIFO read index too often after an underrun, resulting in corruption of the FIFO data.	Impact: Same as description. Work Around: Use work around detailed in Errata Item 5.4.
7.4	If a word is partially received when RE is deasserted, reception of that word will complete and the word will be added to the FIFO.	Impact: Same as description. Work Around: Before asserting RE, software can check for and discard a residual word left in the FIFO arising from an in-process transmission when RE was last deasserted.

Chip Revision B Errata Information:

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Errata Number	Description	Impact and Work Around
Timer Errata Items		
8.4	Unable to count on both edges when IP_CLK is primary count source.	Impact: The problem only occurs When IPbus clock divide by one is used as primary clock source. The timer is not able to count on both edges, it counts only on rising edge. Work Around: None.
9.6	With a Quad Timer counter, when using a single compare register to generate timing intervals and clocking the timer at a rate other than at the IPbus_clock rate the timer may count incorrectly when the compare register is changed.	Impact: When the compare register matches the counter register and is updated before the next timer clock the counter increments/decrements instead of reloading. Work Around: 1. Use both compare registers, such that the compare register that is not active is updated for use in the next count period. 2. Instead of updating the compare register, architect the software so the LOAD register can be updated, with the compare register held constant. A more in depth FAQ can be found on the Freescale website. *freescale.com*
10.5	The interrupt controller uses COPR bit in SIM_RSTSTS register to determine whether to use COP reset vector in the vector table.	Impact: The user must clear this bit at startup after a COP reset, or any subsequent resets will use the COP reset vector. Work Around: Clear the COP Reset bit in the SIM STATUS register.

Differences between Chip Revisions

Chip Rev. A *Date Code = ≥ 0112 < 0222*	**Chip Rev. B** *Date Code = ≥ 0222*
Device will meet ten years of data retention after 5,000 program-erase cycles over the full specified temperature range.	**Corrected**
GPIO interrupts may be missed when clearing other interrupts.	**Corrected**
Writes to internal XRAM during the first cycle out of reset does not work properly. *See errata item 1 for clarification.*	Same as A
N register is not available in the cycle immediately after it is changed *See errata item 2 for clarification.*	Same as A
While in operation if TOD is disabled and the value written onto the TOD alarm registers happens to match with the value on the counters, a TOD alarm interrupt is raised. *See errata item 3 for clarification.*	Same as A
PLL Stabilization Time	**Corrected**
Does not meet all ESD test specifications	**Corrected**
A one second first alarm value causes an alarm interrupt after two seconds instead of one. *See errata item 4 for additional information.*	Same as A
Slave Mode SPI data is corrupted on the MISO output	**Corrected**
Slave Mode SPI TE (transmitter empty) flag set too early.	**Corrected**
Slave Mode SPI transmit shift register data corruption.	**Corrected**
SSI SYNRST can clear RX_FIFO even when RE is cleared.	**Corrected**
The SSI frame sync setup and hold requirements limit input timing when in slave mode.	**Corrected**
The SSI RFS and TFS flags are not synchronized with the system clock.	**Corrected**
When Tx FIFO is refilled with 8 words, the 8th written word is transmitted in the immediate time slot instead of first written word.	**Corrected**
SSI re-transmits previous data, even though new data is available in FIFO (with TUE set).	**Corrected**
A pipeline dependency problem occurs on the secondary data RAM bus when dual parallel reads to XRAM in adjacent instruction cycles, and the read addresses straddle a 1K address boundary.	**Corrected**
Under some conditions when using the FIFO, SSI misses an increment of the FIFO read index and erroneously retransmits the prior word. *See errata item 5 for clarification.*	Same as A
Under some conditions, SSI can increment the FIFO read index too often after an underrun, resulting in corruption of the FIFO data. *See errata item 6 for clarification.*	Same as A
Contrary to spec, if a word is partially received when RE is deasserted, reception of that word will complete and the word will be added to the FIFO. *See errata item 7 for clarification.*	Same as A

Differences between Chip Revisions

Chip Rev. A *Date Code = ≥ 0112 < 0222*	**Chip Rev. B** *Date Code = ≥ 0222*
Unable to count on both edges when IP_CLK is primary count source. *See errata item 8 for additional information.*	Same as A
With a Quad Timer counter, when using a single compare register to generate timing intervals and clocking the timer at a rate other than at the IPbus_clock rate the timer may count incorrectly when the compare register is changed. *See errata item 9 for additional information.*	Same as A
The interrupt controller uses COPR bit in SIM_RSTSTS register to determine whether to use COP reset vector in the vector table. *See errata item 10 for additional information.*	Same as A

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
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