56853

Chip Errata

56853 16-bit Digital Signal Controller

This document reports errata information on chip revision B2. Errata numbers are in the form n.m, where n is the number of the errata item and m identifies the document revision number. This document is a pre-publication draft. **Note:** **Differences between Chip Revisions are listed on page 5** and errata information for chip revisions prior to revision B2 have been archived and can be requested from Freescale Sales.

Chip Revision B2 Errata Information:

The following errata items apply only to Revision B2 56853 devices. These parts are either marked with date codes of 0317 or greater (bottom line of marking).

Errata Number	Description	Impact and Work Around
1.7	Software breakpoint in uninterruptable code can cause debugger to execute instructions in wrong order. *In Rev 7.0, clarified errata impact and work around.*	Impact: If a sequence of code includes a conditional branch (i.e. Bcc) followed by two single word instructions and a breakpoint is set on the first single word instruction, the incorrect code execution will occur when the conditional branch is not taken. Work Around: CodeWarrior has implemented a work around that inserts a NOP after all conditional branches. The breakpoint will be located in the second single word instruction after the NOP, so execution will be correct. This workaround can be enabled or disabled by the user. Disabling the workaround will generate smaller code.
2.0	JTAG Core TAP incorrectly handles bypass instructions using xA instruction code. Also, the combined instruction for Debug requests and TLM select malfunctions.	Impact: Same as description. Work Around: Use separate Debug requests and TLM select instructions. Use other available codes for bypass.
3.3	External interrupts, $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ are unreliable when edge sensitive. This can result in execution of incorrect interrupt.	Impact: Same as description. Work Around: Configure external interrupts for level sensitive operation.
4.5	When Core clock is not continuous, debug mode will fail to shift instructions into the Core.	Impact: Same as description. Work Around: Disable DMA prior to using debug mode to shift instructions into core.

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Errata Number	Description	Impact and Work Around
5.7	DMA circular queue operation does not work properly.	Impact: Data in the destination buffer may be repeated. For example, if a {1, 2, 3, 4} are received, then the destination buffer may contain {1, 2, 3, 3, 4}. Work Around: Do not use the circular queue operation. Instead, use the DMA non-circular operation (default) or use the fast and/or normal interrupts.
6.6	The EOnCE OPDBR register will not work properly if there is more than one JTAG serially connected device used in a scan chain configurations.	Impact: This register is used for executing instructions shifted in by the host through the JTAG when the device is in debug mode. The intended instruction will not be executed under this condition. Note: This does not affect boundary-scan operation, which will still work properly no matter what position the device is placed in the boundary-scan chain. Work Around: 1. Each device must be on a separate scan chain for debugging purposes. 2. If there is only one 56800E device on a scan chain, then the EOnCE OPDRB register will work properly as long as the 56800E device is the first device on the scan chain.
ESSI Errata Items		
7.4	Under some conditions when using the FIFO, ESSI misses an increment of the FIFO read index and erroneously retransmits the prior word. *In Rev 4.0, clarified errata impact and work around.*	Impact: • The ESSI may fail to transmit or may transmit the next available word twice in the transmit FIFO if the following conditions are true simultaneously: - ESSI FIFO is enabled. - Transmit FIFO is written two within 2 ipb_clks before or after the “start point of a word transmit time slot” - Just prior to this 4 ipb_clk window, the TFCNT was less than or equal to 1. • For Normal mode operation with external frame sync, TE should not be cleared until after the first data bit of the last word has been transmitted; otherwise, transmission of the last data word may not be guaranteed. Work Around: The failure is avoided by preventing the TFCNT from falling below 2. To do this, set the watermark (for the number of words left in TX fifo when ISR triggers) to 2 or more. The higher the watermark is set, the longer the TFE ISR has to add new data to the FIFO before TFCNT falls below 2. Error will always be avoided provided the TFE ISR completes execution before (watermark -1) time slot durations have elapsed. A time slot duration is the duration of SCK times bits per word. SCK duration is determined by baud rate controls and bits per word is determined by the WL control. Under some conditions, the safe interval for TFE ISR completion is substantially increased. Please see http://www.freescale.com/ for an FAQ which addresses error recovery options, transmission of filler words when real data isn’t available, and more detail on the safe interval for TFE ISR completion.

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Errata Number	Description	Impact and Work Around
8.4	Under some conditions, ESSI can increment the FIFO read index too often after an underrun, resulting in corruption of the FIFO data. *In Rev 4.0, clarified errata impact and work around.*	Impact: Same as description. Work Around: Use work around detailed in Errata Item 7.4.
9.3	The ESSI specification does not guarantee that a final word loaded into the transmit shift register will be sent.	Impact: The ESSI specification states, “The normal transmit disable sequence is to clear the TE bit and the TIE bit after the TDE bit is set.” In normal mode with external frame sync and regardless of clock source (external or internal), this procedure does not guarantee that a final word loaded into the transmit shift register will be sent. Work Around: The following procedure may be used to insure the complete transmission of a final word conveyed to the transmit shift register: a) Poll for TDE b) Wait for TFS c) Use timer or other method to permit at least one ESSI bit interval to pass d) Set TE and TIE 0
10.8	ESSI Receive Last Slot (RLS) and Transmit Last Slot (TLS) can be missed when the ESSI is configured for network mode and as a slave.	Impact: Same as description. Work Around: Since the number of time slots are known by the application, the software can count the samples as they are received and/or transmitted. The ESSI FIFO or DMA could also be used to buffer an entire frame and then generate an interrupt when the desired number of samples have been received and/or transmitted. Another work around is to connect the Frame Sync signal to a timer input. The timer module can be configured to request an interrupt at the rising edge of its input signal (which is FS), so the interrupt works as a "transmit/receive first slot" indicator (not last). The FS signal must of course be regular, i.e. not "early".

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Errata Number	Description	Impact and Work Around
Timer Errata Items		
11.7	With a Quad Timer counter, when using a single compare register to generate timing intervals and clocking the timer at a rate other than at the IPbus_clock rate the timer may count incorrectly when the compare register is changed.	Impact: When the compare register matches the counter register and is updated before the next timer clock the counter increments/decrements instead of reloading. Work Around: 1. Use both compare registers, such that the compare register that is not active is updated for use in the next count period. 2. Instead of updating the compare register, architect the software so the LOAD register can be updated, with the compare register held constant. FAQ 25527 provides an in-depth discussion of this issue and can be found on the Freescale website, www.*freescale.com.*
12.8	With the Quad Timer, when using Count Mode (CM) 0b110 “edge of secondary source triggers primary count till compare” and the Output Mode (OM) is 0b111 “enable gated clock output while counter is active”, the OFLAG will incorrectly output clock pulses prior to the secondary input edge if the primary count source is not an IPBus clock/N.	Impact: Typically this will arise when an application is trying to output as finite number of 50% duty cycle clock pulses triggered by the output of another timer. Timer 1 creates an infinite pulse train which is fed into the primary input of Timer 2. Timer 2's secondary input is the triggering signal. Timer 2's job is to wait until the trigger and then count out the correct number of clock pulses. Work Around: The workaround is to rearrange functionality. Timer 1 uses an IPBus/N to generate a pulse train at 2x the desired clock rate. It uses CM = 0b110 and OM = 0b111 correctly. Then Timer 2's job is to simply convert the 2x pulse stream into a clock pulse stream at 1x frequency and 50% duty cycle. It does this by CM = 0b001 (count rising edges of primary input) and OM = 0b011 (toggle OFLAG on successful compare) with a compare value of zero.
GPIO Errata Item		
13.7	GPIO interrupts on the SAME port will not be detected if the edge of an input interrupt signal occurs in the same clock cycle that the IESR is written.	Impact: Hardware designs that have asynchronous interruptable inputs on the same GPIO port cannot rely on the device to generate the interrupt. Work Around(s): 1. Use different ports for these two interrupts. 2. After writing to the IESR, read the RAW_DATA register to determine if any other inputs have occurred at this exact instant.

Differences between Chip Revisions

Chip Rev. A *Date Code = ≥ 0141 < 0215*	**Chip Rev. A1** *Date Code = ≥ 0215 < 0235*	**Chip Rev. B** *Date Code = ≥ 0235 < 0302*	**Chip Rev. B1** *Date Code = > 0302 < 0316*	**Chip Rev. B2** *Date Code = ≥ 0317*
Control register field VAB does not always correctly indicate which ISR is executing.	*This entry was the result of a misinterpretation; it was never an errata.*			
Edge sensitive interrupt pulse width must be longer than clock hold off to be seen.	Same as A	**Corrected**		
Software breakpoint in uninterruptable code can cause debugger to execute instructions in wrong order. *See errata item 1 for clarification.*	Same as A	Same as A1	Same as B	Same as B1
Core TAP incorrectly handles bypass instructions using xA instruction code. *See errata item 2 for clarification.*	Same as A	Same as A1	Same as B	Same as B1
X1 read in the next system cycle after X1 write, returns invalid data if either write, read or both are long and addresses differ only in bit A0.	Same as A	**Corrected**		
Contention in XRAM in reset state wastes power.	Same as A	**Corrected**		
False trigger on clock inputs in the Slave mode.	Same as A	**Corrected**		
SCI Boot mode does not operate properly.	**Corrected**			
Improper Power-On Reset (POR).	Same as A	**Corrected**		
Does not meet all ESD test specifications.	Same as A	**Corrected**		
Power loss when output TDO is tristated.	Same as A	**Corrected**		
Invalid transfer in early framesync mode when frames separated by two unused cycles	Same as A	**Corrected**		
Can not generate exception/error interrupts in DMA mode	Same as A	**Corrected**		
When configured as master with inverted clock output and non-inverted frame sync, some fed slave devices which sample FS with an inverted clock can observe FS as a clock early, resulting in incorrect transfers.	Same as A	**Corrected**		
SPTE flag does not set dependably in slave mode.	Same as A	**Corrected**		
SPI Boot mode does not work with all specified devices.	**Corrected**			
SPI receiver shift register residual after overflow, resulting in duplicate transmission.	Same as A	**Corrected**		
Intermittent duplicate transmission in slave mode when CPHA=0.	Same as A	**Corrected**		
The DMA bit in ISR does not reflect correct status.	Same as A	**Corrected**		
The HDMA status field in the HSR register does not correctly indicate whether the HI is appropriately configured for Host side DMA operation.	Same as A	**Corrected**		

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Intermittently, the RXDF bit is not cleared in ISR after read and intermittent data corruption occurs on the HD0 - HD7 bus.	**Corrected**			
When processor enters the Stop mode status, bits in HSR and ISR are not properly updated.	Same as A	**Corrected**		
When programmed for stop mode operation, COP can hang and fail to operate if stop mode is entered while it is setting or resetting the counter.	Same as A	**Corrected**		
Transmitter underrun can occur without TUE flag asserting.	Same as A	**Corrected**		
Last slot interrupts fire repeatedly while in the last slot.	Same as A	**Corrected**		
ESSI loses first word in Network Transmit mode if first time slot is invalid.	Same as A	**Corrected**		
Transmitter side DMA request signal is not qualified with the SPI enable signal, so the SPI can be disabled but still issue the transmitter DMA requests.	Same as A	**Corrected**		
The $\overline{\text{HREQ}}$/$\overline{\text{HTRQ}}$ output should operate as an open drain output only.	Same as A	**Corrected**		
External interrupts, $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ are unreliable when edge sensitive. This can result in execution of incorrect interrupt. *See errata item 3 for clarification.*	Same as A	Same as A1	Same as B	Same as B1
Low speed differential clock used for the OSC module's time of day prescaler and for deep stop mode detection is unreliable.	Same as A	Same as A1	**Corrected**	
When Core clock is not continuous, debug mode will fail to shift instructions into the Core. *See errata item 4 for clarification.*	Same as A	Same as A1	Same as B	Same as B1
DMA circular queue operation does not work properly. *See errata item 5 for clarification.*	Same as A	Same as A1	Same as B	Same as B1
PLL sensitivity at low temperature/low supply voltage.	Same as A	Same as A1	Same as B	**Corrected**
The EOnCE OPDBR register will not work properly if there is more than one JTAG serially connected device used in a scan chain configurations. *See errata item 6 for clarification.*	Same as A	Same as A1	Same as B	Same as B1
In DMA mode, when the high address byte is written or read, a narrow glitch could appear on the $\overline{\text{HREQ}}$ output when the $\overline{\text{HACK}}$ input transitions from low to high.	Same as A	**Corrected**		
Only one of the two channels can be dedicated to DMA at one time.	Same as A	**Corrected**		
Under some conditions when using the FIFO, ESSI misses an increment of the FIFO read index and erroneously retransmits the prior word. *See errata item 7 for clarification.*	Same as A	Same as A1	Same as B	Same as B1

Differences between Chip Revisions

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TUE can assert without an actual transmitter underrun having occurred.	Same as A	Same as A1	**Corrected**	
Under some conditions, ESSI can increment the FIFO read index too often after an underrun, resulting in corruption of the FIFO data. *See errata item 8 for clarification.*	Same as A	Same as A1	Same as B	Same as B1
An internal clock, known as the op clock, can glitch, causing the serial output flags to malfunction.	Same as A	Same as A1	**Corrected**	
The ESSI specification does not guarantee that a final word loaded into the transmit shift register will be sent. *See errata item 9 for clarification.*	Same as A	Same as A1	Same as B	Same as B1
ESSI Receive Last Slot (RLS) and Transmit Last Slot (TLS) can be missed when the ESSI is configured for network mode and as a slave. *See errata item 10 for clarification.*	Same as A	Same as A1	Same as B	Same as B1
If a word is partially received when RE is deasserted, reception of that word will complete and the word will be added to the FIFO.	Same as A	Same as A1	**Corrected**	
Underrun error can occur without TUE set.	Same as A	Same as A1	**Corrected**	
Failure occurs if a duplicate read is done on the ESSI FIFO, resulting in loss of receiver data.	Same as A	Same as A1	**Corrected**	
Intermittent loss of lock by digital lock detector.	Same as A	**Corrected**		
Scan muxes on POR reset outputs can block the reset unless TRST asserts to reset scan mode before the POR disasserts.	Same as A	**Corrected**		
POR can trigger falsely at combinations of very high V_{DDA} and very cold temperatures.	Same as A	Same as A1	**Corrected**	
With a Quad Timer counter, when using a single compare register to generate timing intervals and clocking the timer at a rate other than at the IPbus_clock rate the timer may count incorrectly when the compare register is changed. *See errata item 11 for clarification.*	Same as A	Same as A1	Same as B	Same as B1
With the Quad Timer, when using Count Mode (CM) 0b110 and the Output Mode (OM) is 0b111, the OFLAG will incorrectly output clock pulses prior to the secondary input edge if the primary count source is not an IPBus clock/N. *See errata item 12 for clarification.*	Same as A	Same as A1	Same as B	Same as B1
GPIO interrupts on the SAME port will not be detected if the edge of an input interrupt signal occurs in the same clock cycle that the IESR is written. *See errata item 13 for clarification.*	Same as A	Same as A1	Same as B	Same as B1

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