DSP56321CE0K93M
Rev. 1, 11/2004

DSP56321 Device Errata for Mask 0K93M

To prevent the use of instructions or sequences of instructions that do not operate correctly, we encourage you to use the “lint563” program to identify such cases and use alternative sequences of instructions. This program is available as part of the Freescale DSP Tools CLAS package.

Silicon Errata

Errata Number	Errata Description	Applies to Mask
	None known.	0K93M

ED1	Description (revised 11/9/98):
	
	XY memory data move does not work properly under one of the following two situations:
	
	1. The X-memory move destination is internal I/O and the Y-memory move source is a register used as destination in the previous adjacent move from non Y-memory
	
	2. The Y-memory move destination is a register used as source in the next adjacent move to non Y-memory.
	
	Here are examples of the two cases (where x:(r1) is a peripheral):
	
	Example 1:
	
	`move #$12,y0`
	`move x0,x:(r7) y0,y:(r3) (while x:(r7) is a peripheral).`
	
	Example 2:
	
	`mac x1,y0,a x1,x:(r1)+ y:(r6)+,y0`
	`move y0,y1`
	
	Any of the following alternatives can be used:
	
	a. Separate these two consecutive moves by any other instruction.
	
	b. Split XY Data Move to two moves.
	
	Pertains to: DSP56300 Family Manual, Section B-5 “Peripheral pipeline restrictions.
		0K93M

ED7	Description (added 1/27/98): When activity is passed from one DMA channel to another and the DMA interface accesses external memory (which requires one or more wait states), the DACT and DCH status bits in the DMA Status Register (DSTR) may indicate improper activity status for DMA Channel 0 (DACT = 1 and DCH[2:0] = 000). Workaround: None. This is not a bug, but a specification update.	0K93M

ED9	Description (added 1/27/98): When the SCI is configured in Synchronous mode, internal clock, and all the SCI pins are enabled simultaneously, an extra pulse of 1 DSP clock length is provided on the SCLK pin. Workaround: a. Enable an SCI pin other than SCLK. b. In the next instruction, enable the remaining SCI pins, including the SCLK pin. This is not a bug, but a specification update.	0K93M
ED17	Description (added 9/28/98): In all DSP563xx technical data sheets, a note is to be added under "AC Electrical Characteristics" that although the minimum value for "Frequency of Extal" is 0MHz, the device AC test conditions are 16 MHz and rated speed. Workaround: N/A	0K93M
ED26	Description (added 1/6/99): The specification DMA Chapter is wrong. "Due to the DSP56300 Core pipeline, after DE bit in DCRx is set, the corresponding DTDx bit in DSTR will be cleared only after two instruction cycles." Should be replaced with: "Due to the DSP56300 Core pipeline, after DE bit in DCRx is set, the corresponding DTDx bit in DSTR will be cleared only after three instruction cycles."	0K93M

ED28	Description (added 1/7/1997; identified as Documentation Errata 2/1/99):
	
	When two consecutive LAs have a conditional branch instruction at LA-1 of the internal loop, the part does not operate properly. For example, the following sequence may generate incorrect results:
	
	`DO #5, LABEL1`
	`NOP`
	`DO #4, LABEL2`
	`NOP`
	`MOVE (R0) +`
	`BSCC _DEST ; conditional branch at LA-1 of internal loop`
	`NOP ; internal LA LABEL2`
	`NOP ; external LA LABEL1`
	`NOP`
	`NOP`
	`_DEST NOP`
	`NOP`
	`RTS`
	
	Workaround: Put an additional NOP between LABEL2 and LABEL1.
	
	Pertains to: DSP56300 Family Manual, Appendix B, Section B-4.1.3, "At LA-1."
		0K93M

ED29	Description (added 9/12/1997; identified as a Documentation errata 2/1/99): When the ESSI transmits data with the CRA Word Length Control bits (WL[2:0]) = 100, the ESSI is designed to duplicate the last bit of the 24-bit transmission eight times to fill the 32-bit shifter. Instead, after shifting the 24-bit word correctly, eight 0s are being shifted. Workaround: None at this time. **Pertains to:** UM, Section 7.4.1.7, "CRA Word Length Control." The table number is 7-2.	0K93M

ED30	Description (added 9/12/1997; identified as a Documentation errata 2/1/99): When the ESSI transmits data in the On-Demand mode (i.e., MOD = 1 in CRB and DC[4:0] = $00000 in CRA) with WL[2:0] = 100, the transmission does not work properly. Workaround: To ensure correct operation, do not use the On-Demand mode with the WL[2:0] = 100 32-bit Word-Length mode. **Pertains to:** UM, Section 7.5.4.1, "Normal/On-Demand Mode Selection."	0K93M
ED31	Description (added 9/12/1997; modified 9/15/1997; identified as a Documentation errata 2/1/99): Programming the ESSI to use an internal frame sync (i.e., SCD2 = 1 in CRB) causes the SC2 and SC1 signals to be programmed as outputs. If however, the corresponding multiplexed pins are programmed by the Port Control Register (PCR) to be GPIOs, then the GPIO Port Direction Register (PRR) chooses their direction, but this causes the ESSI to use an external frame sync if GPIO is selected. **Note:** This errata and workaround apply to both ESSI0 and ESSI1. Workaround: To assure correct operation, either program the GPIO pins as outputs or configure the pins in the PCR as ESSI signals. **Note:** The default selection for these signals after reset is GPIO. **Pertains to:** UM, Section 7.4.2.4, "CRB Serial Control Direction 2 (SCD2) Bit 4"	0K93M

ED32	Description (added 11/9/98; identified as a Documentation errata 2/1/99):
	
	When returning from a long interrupt (by RTI instruction), and the first instruction after the RTI is a move to a DALU register (A, B, X, Y), the move may not be correct, if the 16-bit arithmetic mode bit (bit 17 of SR) is changed due to the restoring of SR after RTI.
	
	Workaround:
	
	Replace the RTI with the following sequence:
	
	`movec  ssl,sr`
	`nop`
	`rti`
	
	Pertains to: DSP56300 Family Manual. Add a new section to Appendix B that is entitled “Sixteen-Bit Compatibility Mode Restrictions.”
		0K93M

ED33	Description (added 12/16/98; identified as a Documentation errata 2/1/99): When Stack Extension mode is enabled, a use of the instructions BRKcc or ENDDO inside do loops might cause an improper operation. If the loop is non nested and has no nested loop inside it, the errata is relevant only if LA or LC values are being used outside the loop. Workaround: If Stack Extension is used, emulate the BRKcc or ENDDO as in the following examples. We split between two cases, finite loops and do forever loops. 1) Finite DO loops (i.e. not DO FOREVER loops) ========== BRKcc Original code: do #N,label1 .... do #M,label2 .... BRKcc .... label2 .... label1 Will be replaced by: do #N, label1 .... do #M, label2 .... Jcc fix_brk_routine	0K93M

ED33 cont.	nop_before_label2 nop ; This instruction must be NOP. label2 .... label1 .... fix_brk_routine move #1,lc jmp nop_before_label2 ENDDO ------ Original code: do #M,label1 .... do #N,label2 .... ENDDO .... label2 .... label1 Will be replaced by: do #M, label1 .... do #N, label2 .... JMP fix_enddo_routine	0K93M

ED33 cont.	nop_after_jmp NOP ; This instruction must be NOP. .... label2 .... label1 .... fix_enddo_routine move #1,lc move #nop_after_jmp,la jmp nop_after_jmp 2) DO FOREVER loops ========== BRKcc ----- Original code: do #M,label1 .... do forever,label2 .... BRKcc .... label2 .... label1	0K93M

ED33 cont.	Will be replaced by: do #M,label1 .... do forever,label2 .... JScc fix_brk_forever_routine ; <--- note: JScc and not Jcc .... nop_before_label2 nop ; This instruction must be NOP. label2 .... label1 .... fix_brk_forever_routine move ssh,x:<..> ; <..> is some reserved not used address (for temporary data) move #nop_before_label2,ssh bclr #16,ssl ; move #1,lc rti ; <---- note: "rti" and not "rts" ! ENDDO ------ Original code: do #M,label1	0K93M

ED33 cont.	do forever,label2 .... ENDDO .... label2 .... label1 Will be replaced by: do #M,label1 .... do forever,label2 .... JSR fix_enddo_routine ; <--- note: JSR and not JMP nop_after_jmp NOP ; This instruction should be NOP .... label2 .... label1 .... fix_enddo_routine nop move #1,lc bclr #16,ssl move #nop_after_jmp,la rti ; <--- note: "rti" and not "rts" **Pertains to:** DSP56300 Family Manual, Section B-4.2, “General Do Restrictions.”	0K93M

ED34	Description (added 1/5/99; identified as a Documentation errata 2/1/99): When stack extension is enabled, the read result from stack may be improper if two previous executed instructions cause sequential read and write operations with SSH. Two cases are possible: Case 1: For the first executed instruction: move from SSH or bit manipulation on SSH (i.e. jclr, brclr, jset, brset, btst, bsset, jsset, bsclr, jsclr). For the second executed instruction: move to SSH or bit manipulation on SSH (i.e. jsr, bsr, jscc, bscc). For the third executed instruction: an SSL or SSH read from the stack result may be improper - move from SSH or SSL or bit manipulation on SSH or SSL (i.e., bset, bclr, bchg, jclr, brclr, jset, brset, btst, bsset, jsset, bsclr, jsclr). Workaround: Add two NOP instructions before the third executed instruction. Case 2: For the first executed instruction: bit manipulation on SSH (i.e. bset, bclr, bchg). For the second executed instruction: an SSL or SSH read from the stack result may be improper - move from SSH or SSL or bit manipulation on SSH or SSL (i.e., bset, bclr, bchg, jclr, brclr, jset, brset, btst, bsset, jsset, bsclr, jsclr). Workaround: Add two NOP instructions before the second executed instruction. **Pertains to:** DSP56300 Family Manual, Appendix B, add a new section called “Stack Extension Enable Restrictions.” Cover all cases. Also, in Section 6.3.11.15, add a cross reference to this new section.	0K93M

ED38	Description (added 7/14/99): If Port A is used for external accesses, the BAT bits in the AAR3-0 registers must be initialized to the SRAM access type (i.e. BAT = 01) or to the DRAM access type (i.e. BAT = 10). To ensure proper operation of Port A, this initialization must occur even for an AAR register that is not used during any Port A access. Note that at reset, the BAT bits are initialized to 00. **Pertains to:** *DSP56300 Family Manual*, Port A Chapter (Chapter 9 in Revision 2), description of the BAT[1 –0] bits in the AAR3 - AAR0 registers. Also pertains to the core chapter in device-specific user's manuals that include a description of the AAR3 - AAR0 registers with bit definitions (usually Chapter 4).	0K93M

ED40	Description (added 11/11/99):
	When an instruction with all the following conditions follows a repeat instruction, then the last move will be corrupted.:
	1. The repeated instruction is from external memory.
	2. The repeated instruction is a DALU instruction that includes 2 DAL registers, one as a source, and one as destination (e.g. tfr, add).
	3. The repeated instruction has a double move in parallel to the DALU instruction: one move's source is the destination of the DALU instruction (causing a DALU interlock); the other move's destination is the source of the DALU instruction.
	Example:
	rep #number
	tfr x0,a x(r0)+,x0 a,y0 ; This instruction is from external memory
	|__|_____|------|----------> This is condition 3 second part.
	|_____|----------> This is condition 3, first part - DALU interlock
	In this example, the second iteration before the last, the "x(r0)+,x0" doesn't happen. On the first iteration before the last, the X0 register is fixed with the "x(r0)+,x0", but the "tfr x0,a" gets the wrong value from the previous iteration's X0. Thus, at the last iteration the A register is fixed with "tfr x0,a", but the "a,y0" transfers the wrong value from the previous iteration's A register to Y0.
	Workaround:
	1. Use the DO instruction instead; mask any necessary interrupts before the DO.
	2. Run the REP instructions from internal memory.
	3. Don't make DALU interlocks in the repeated instruction. After the repeat make the move. In the example above, all the "move a,y0" are redundant so it can be done in the next instruction:
	`rep #number`
	`tfr x0,a x(r0)+,x0`
	`move a,y0`
	If no interrupts before the move is a must, mask the interrupts before the REP. **Pertains to:** *DSP56300 Family Manual*, Rev. 2, Section A.3, "Instruction Sequence Restrictions."
		0K93M

ED42	Description (added on 3/22/2000) **Revised 10/29/2004.** When the device is operating in a mode in which DE is not cleared at the end of the block transfer (DTM = 100 or 101), the DMA end-of-block-transfer interrupt may not be latched when the external bus arbitration controller asserts the bus grant/BG pin. This causes the end-of-block-transfer interrupt to be lost. **Pertains to:** *DSP56300 Family Manual,* Rev. 2, Section 10.4.1.2, “End-of-Block-Transfer Interrupt.” Also, Section 10.5.3.5, “DMA Control Registers (DCR[5–0],” discussion of bits 21 – 19 (DTM bits).	0K93M
ED47	Description: (added 1/19/2002): When DMA line-by-line block transfers are used with the EFCOP to perform IIR filtering with two or fewer IIR coefficients, the first output of the IIR filter is lost. The rest of the outputs are shifted and inaccurate. Workaround: Instead of DMA line-by-line block transfers, use DMA word-by-word block transfers.	0K93M
ED50	Description (added 9/10/1996 as ES29; reclassified as a documentation erratum on 8/2/2002): When the SCI transmitter is used in Synchronous mode, the last bit of the transmitted byte might be truncated to the half of the serial cycle. Workaround: Not available.	0K93M

NOTES

1. An over-bar (i.e., $\overline{\text{xxxx}}$) indicates an active-low signal.
2. The letters in the right column tell which DSP56321 mask numbers apply.

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