



MOTOROLA

Chip Errata
DSP56156 Digital Signal Processor
 Mask: E98S/F44E

ERRATA

Errata Description

1. There are three speed grades of the E98S/F44E silicon of the DSP56156: 40 MHz, 50 MHz and 60 MHz. These three speed grades are tested as shown in the table below.

Applies to Mask

D13N
 E69A
 E25H
 E25S
 E98S
 F44E

Table 1: E98S/F44E Marking and Testing Conditions

| Characteristic | Symbol | 40 MHz | | 50 MHz | | 60 MHz | | Unit |
|----------------------|-----------------|--------|------|--------|------|--------|------|------|
| | | Min | Max | Min | Max | Min | Max | |
| Supply Voltage | V _{CC} | 4.75 | 5.25 | 4.75 | 5.25 | 4.75 | 5.25 | V |
| Junction Temperature | T _J | — | 115 | — | 115 | — | 115 | °C |

Errata Description

Applies to Mask

2. The \overline{BS} signal is being deasserted before \overline{TA} is deasserted if the BCR is programmed for one or more wait states. In this case, the \overline{BS} signal ignores the \overline{TA} signal and is deasserted under control of the BCR even though \overline{TA} is still active and should cause \overline{BS} to remain active.

F44E
E98S

This problem occurs at:

| | | |
|-----------|---|--------|
| f_{OSC} | = | 60 MHz |
| T_J | ≥ | 25 °C |
| V_{CC} | ≤ | 5 V |

This problem has not been reported on parts rated at less than 60 MHz, although it has been seen at 50 MHz at 5 V and may be appear at other speeds.

The temporary solution is to use either the BCR register or the \overline{TA} signal to insert wait states but not both.

3. The lock bit detection circuitry in the PLL fails to operate correctly in an overdamped system. A work around is to use a smaller capacitance value for the SXFC capacitor to GND. However reducing this capacitor value will increase PLL jitter. If jitter is found to be unacceptable then it is recommended to switch to a larger capacitance once the lock bit has been asserted. If this (hardware) fix cannot be done then the operating software for the device must be changed from a polling technique on the lock bit to simply waiting for 5mS for the PLL to lock before enabling the PLL to the core.

F44E
E98S



Freescale Semiconductor, Inc.

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NOTES

1. An over-bar (i.e. $\overline{\text{xxxx}}$) indicates an active-low signal.
2. The letters seen to the right of the errata tell which DSP56156 mask numbers apply.
3. Manuals and data sheets may also have errata that is documented on the appropriate errata sheet as discovered.

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