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MAC57D5xx STCU BIST Configuration

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Contents

1 Introduction

This document describes the MAC57D5xx default Self-Test Control Unit (STCU) configuration for offline Built-In Self-Tests (BIST). The default STCU configuration is programmed in the MAC57D5xx during factory test and enables BIST execution by default. BIST will execute at device startup events, as specified in the MAC57D5xx Reference Manual. This document provides instructions for disabling BIST execution. Also included in this document are details on the default configuration settings for BIST faults and recommendations on handling BIST faults.

2 STCU BIST Configuration Summary

- Offline BIST **enabled** by default
- Overall coverage level (with BIST enabled): ASIL-B
- IRC: 16 MHz Internal RC Oscillator
- MBIST:
  - Memory partitions 0-167, tested in parallel

- Coverage/Algorithm: Auto test - simplified Multi Bit Upset algorithm is used to check the RAM. In case a ROM is selected, the applied algorithm will be the Standard one without PMOS Test
- Execution time: 10 ms (+/- 8% according to IRC trim tolerance)

3 Disable BIST Execution

The default BIST configuration for MAC57D5xx enables BIST execution at start-up. To prevent execution of BIST at start-up, the STCU configuration must be adjusted to disable offline BIST.

To disable BIST, a single Device Configuration Format (DCF) record should be written to the UTEST FLASH section in the first available space immediately after the last valid DCF entry in the UTEST. The DCF record area starts at 0x18400300. After the DCF record area, the first address which contains 0xFFFFFFFF_FFFFFFFF is the first open UTEST memory address, as shown in Figure 1.

The following DCF record should be written to the first open UTEST memory address to disable BIST:

Table 1. DCF record configuration

Data	DCF client
0x7FC00000 (pointer to NIL- No BIST execution)	0x0008000C (STCU2_CFG)

NOTE

In case the STCU2 register access lasts more cycles than the one defined into the Hardcoded WDG time-out, the STCU2 write access is locked and the WDG and Register ITF clocks are switched off. Also in this case, in order to enable again the write access to the STCU2 and the WDG and Register ITF clocks, it is required to apply again the sequence.

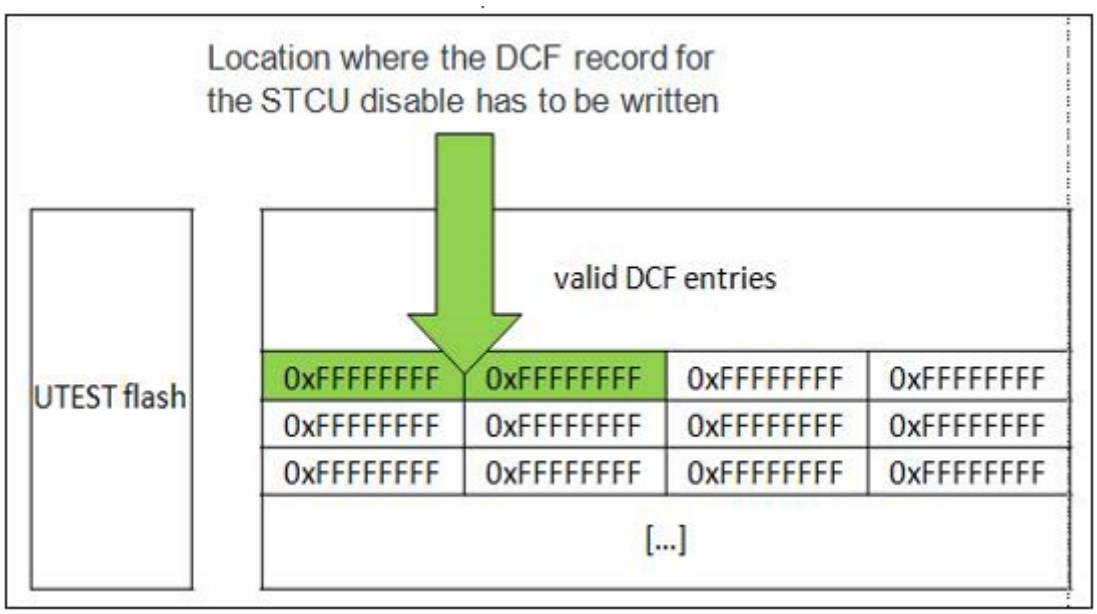

Figure 1. How to identify first open UTEST memory address

4 BIST Execution

When enabled, BIST will execute at the following start-up events:

- Power-on reset (POR)
- External reset with the reset sequence configured in Reset Generation Module to start from PHASE1
- Destructive reset

5 BIST Clock Settings

STCU offline BIST uses the 16 MHz IRC clock. No external clocks are required to run offline self-test.

6 MBIST

MBIST is executed for all memories which are segmented into 168 individual memory partitions as shown in following table. The default MBIST configuration tests all MAC57D5xx memory partitions, 0-167, in parallel.

The default MBIST configuration for the MAC57D5xx executes auto Test Mode with PMOS disabled and simplified algorithm, which provides greater than 60% coverage.

Table 2. MBIST memory partitioning

Partition number	Memory association
0	CM0+ RAM
1	
2	2D-ACE 0
3	
4	
5	2D-ACE 1
6	
7	
8	2D-ACE 1
9	2D-ACE 0
10	2D-ACE 0
11	
12	
13	2D-ACE 1
14	
15	
16	2D-ACE 0
17	

Table continues on the next page...

Table 2. MBIST memory partitioning (continued)

18	
19	
20	
21	
22	
23	
24	
25	
26	
27	
28	2D-ACE 1
29	
30	
31	
32	
33	
34	
35	
36	
37	
38	
39	
40	2D-ACE 1
41	2D-ACE 0
42	2D-ACE 1
43	
44	
45	
46	GC355 GPU
47	
48	
49	
50	
51	
52	
53	
54	
55	
56	
57	

Table continues on the next page...

Table 2. MBIST memory partitioning (continued)

58	
59	
60	
61	
62	
63	
64	
65	
66	
67	
68	
69	
70	
71	
72	CA5 ETB RAM
73	CA5 TLB RAM
74	
75	CA5 DCACHE DRAM
76	
77	
78	
79	CA5 ICACHE DRAM
80	
81	CA5 DIRTY RAM
82	CA5 DCACHE TAG RAM
83	
84	
85	
86	CA5 ICACHE TAG RAM
87	
88	SRAM_0
89	
90	
91	
92	
93	
94	
95	
96	SRAM_1
97	

Table continues on the next page...

Table 2. MBIST memory partitioning (continued)

98	
99	
100	
101	
102	
103	
104	GRAM
105	
106	
107	
108	
109	
110	
111	
112	
113	
114	
115	
116	
117	
118	
119	
120	
121	
122	
123	
124	
125	
126	
127	CSE RAM
128	
129	
130	
131	
132	
133	
134	
135	DMA RAM
136	
137	FlexCAN

Table continues on the next page...

Table 2. MBIST memory partitioning (continued)

138	
139	
140	MLB
141	ENET
142	
143	QuadSPI
144	
145	SGM
146	
147	
148	
149	CM4 ETB RAM
150	CM4 TCM
151	
152	
153	
154	CM4 DCACHE DRAM
155	
156	
157	
158	CM4 ICACHE DRAM
159	
160	
161	
162	CM4 ICACHE TAG RAM
163	
164	CM4 DCACHE TAG RAM
165	
166	HTM ETB RAM
167	BAR ROM

7 Fault Handling

The default configuration for the MAC57D5xx sets all BIST faults as recoverable faults.

After BIST execution, application software should check the following registers to determine whether a fault has occurred:

- STCU2 error register: STCU2_ERR_STAT (will read all zeros if no fault occurred)
  - Recoverable Faults Status Flag: STCU2_ERR_STAT[RFSF]
  - Unrecoverable Faults Status Flag: STCU2_ERR_STAT[UFSF]

If a fault has occurred, the following STCU2 status registers should be read to determine the source of the fault:

Table 3. STCU Status registers

STCU register name	Register description	Expected value if no fault after BIST execution
STCU2_MBSLn	Off-Line MIBST Status Low Register	0xFFFF_FFFF
STCU2_MBSMn	Off-Line MBIST Status Medium Register	0xFFFF_FFFF
STCU2_MBSHn	Off-Line MBIST Status High Register	0x0FFF_FFFF
STCU2_MBELn	Off-Line MBIST End Flag Low Register	0xFFFF_FFFF
STCU2_MBEMn	Off-Line MBIST End Flag Medium Register	0xFFFF_FFFF
STCU2_MBEHn	Off-Line MBIST End Flag High Register	0x0FFF_FFFF

The STCU2 communicates fault information to the Fault Control and Collection Unit (FCCU) to indicate the occurrence of an unrecoverable fault and/or a recoverable fault failure during the BIST sequence. If a fault does occur, application software should check the FCCU status registers to see if an error has occurred. The FCCU has dedicated fault input mappings for STCU BIST fault indications, as shown in the table below.

Table 4. FCCU Non-Critical Fault Mapping for STCU Module

FCCU Non-Critical Fault Number	Description
NCF[6]	Critical fault indication from STCU
NCF[7]	Non-critical fault indication from STCU
NCF[8]	Critical fault indication from STCU in case MBIST control signals go to wrong condition during user application

Refer to FCCU module chapter in the device reference manual for more information, and consult the MAC57D5xx Reference Manual and Safety Manual to ensure that fault handling is performed correctly in order to achieve required safety coverage levels.

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