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908QTA/QYxA Conversion Guidelines

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1 Introduction

This engineering bulletin describes the 908QTA/QYxA. The 908QTA/QYxA is an enhanced device intended to replace the 908QT/QYx series of devices (referred to as the QY Classic in this document). Customer requests have led to the advanced design of the QYxA that has added adaptability, new features, and contains lead-free packaging.

This document:

- Provides information needed to convert from QY Classic to the enhanced QYxA
- Highlights the benefits of making this change

Sections:

- Benefits of the Enhanced QYxA
- Conversion Considerations
- Code Changes Checklist
- Development Tools
- Differences in Packaging

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2 Benefits of the Enhanced QYxA

The QYxA contains new and enhanced modules that add more flexibility and new features to the QY Classic. These benefits can improve the operation of an application or lead to new features for an application. For more information regarding these features refer to the QYxA data sheet (Freescale document order number MC68HC908QYxA).

2.1 New Analog-to-Digital Converter Module (ADC)

The QYxA contains a 10-bit ADC which replaces the 8-bit ADC on the QY Classic. This module allows both 10-bit and 8-bit conversion modes. The increased precision for ADC readings can be very useful in many applications.

Features of the ADC new 10-bit module include:

- There are two new ADC channels that have been placed on PTB0 and PTB1 allowing added flexibility especially when debugging in Monitor Mode.
  - A limitation of QY Classic debugging is that access to the ADC channels is limited because many of the QY Classic pins are multiplexed. Having extra ADC channels on the PTB pins resolves this limitation.
- The ADC that is on the QYxA can operate while the MCU is in stop mode allowing lower power operation. This also adds a lower noise environment for precise ADC results.
- Enabling an ADC channel no longer overrides the digital I/O function of the associated pin. To prevent the digital I/O from interfering with the ADC read of the pin, the data direction bit associated with the port pin must be set as input.
- Finally, the new ADC can be configured to select two different reference clock sources:
  - The internal bus x 4
  - An internal asynchronous source

  The internal asynchronous clock source allows the ADC to be clocked for operation in stop mode.

2.1.1 Registers Affected

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	COCO	AIEN	ADCO	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0
Write:								
Reset:	0	0	0	1	1	1	1	1

= Unimplemented

Figure 1. ADC10 Status and Control Register (ADSCR)

The ADCHx bits can be used to select additional ADC channels or bandgap measurement.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	AD9	AD8
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 2. ADC10 Data Register High (ADRH), 10-Bit Mode

10-bit ADC uses the new ADRH register for the upper 2 bits.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	ADLPC	ADIV1	ADIV0	ADICLK	MODE1	MODE0	ADLSMP	ACLKEN
Write:								
Reset:	0	0	0	0	0	0	0	0

Figure 3. ADC10 Clock Register (ADCLK)

A long sample time option has been added to conserve power at the expense of longer conversion times. This option is selected using the new ADLSMP bit in the ADCLK register. (The bit location was previously reserved.)

The ADC will now run in stop mode if the ACLKEN bit is set to enable the asynchronous clock inside the ADC module. Utilizing stop mode for an ADC conversion gives the quietest operating mode to get extremely accurate ADC readings. (This bit location now used by ACLKEN was reserved — it always read as a 0 and writes to that location had no affect.)

2.2 Enhanced Oscillator Module (OSC)

The QYxA contains a much enhanced oscillator module that allows more options than the QYx Classic.

- The ICFS bits in the Oscillator Status and Control Register (OSCSC) allow the Internal Oscillator to be configured for 1-, 2-, or 3.2-MHz operation. Also, the ECFS bits in the same register allow a low, medium, or high crystal frequency range to be selected for the source of the system clock. With this option you can choose to use a 32-kHz (low range) or a 16-MHz (high range) crystal.
- Another improvement to the Oscillator Module design is that you can switch between internal oscillator and external oscillator options at any time. For example, if you wanted the low power advantage of running from a 32-kHz crystal but still needed some processing power to perform math calculations you could switch back and forth between internal and external clock. The same is true for switching between 1-, 2-, and 3.2-MHz internal oscillator options.

2.2.1 Registers Affected

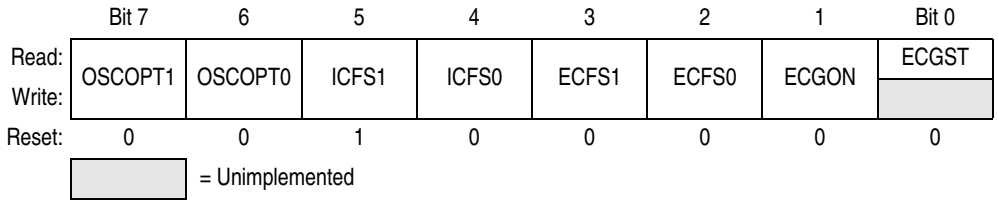

Figure 4. Oscillator Status and Control Register (OSCSC)

The OSCOPT bits are no longer in the CONFIG2 register and now reside in the OSCSC register. Also, the ICFSx and ECFSx bits now reside in this register.

The IFS bits are used to select different Internal Oscillator speeds.

The ECFS bits are used to select the range of crystal that should be used to provide the reference clock.

2.3 Improved Auto Wakeup Module (AWU)

The QYxA contains an AWU that has improved accuracy across voltage and temperature for typical testing.

- A new feature provides ability to run the AWU from an alternate source (internal oscillator or external crystal). This is an advantage for an application that needs more accurate AWU operation.
- On the QYxA AWU approximate time out will be 16 ms for short time out and 512 ms for long time out when running from the internal 32-kHz RC source.
- Finally, at lower voltages typical measurements have shown lower power consumption by the QYxA AWU.

2.3.1 Registers Affected

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	IRQPUD	IRQEN	R	R	R	R	OSCENINSTOP	RSTEN
Reset:	0	0	0	0	0	0	0	U
POR:	0	0	0	0	0	0	0	0

R = Reserved U = Unaffected

Figure 5. Configuration Register 2 (CONFIG2)

Setting the OSCENINSTOP bit forces the AWU to use bus clock x 4 as the source to this timeout.

2.4 New Power-on Reset Module (POR)

The QYxA POR re-arm voltage will have a minimum specification of 0.7 V while the QYx Classic POR re-arm was 0.1 V. The higher POR re-arm voltage provides added protection against brown out conditions.

2.5 Keyboard Interface Module (KBI) Functionality

The KBI module for the QYxA has the added capability of:

- Triggering a KBI interrupt on the rising or falling edge of an input while the QYx Classic has the capability of triggering on falling edges only.
  - A new register (Keyboard Interrupt Polarity Register) determines the polarity of KBI and the default state of this register configures the QYxA for triggering on falling edges to be compatible with QYx Classic.
  - The QYxA now has pull down resistors for the input pins that are configured for rising edge operation.

2.5.1 Registers Affected

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	KBIP5	KBIP4	KBIP3	KBIP2	KBIP1	KBIP0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 6. Keyboard Interrupt Polarity Register (KBIPR)

The KBIPR allows the selection of polarity, if any of these bits are set the corresponding interrupt pin will be configured for rising edge and a pulldown resistor will be added to the pin.

2.6 On-Chip Routine Enhancements

Enhancements have been made to the on-chip routines that are used for FLASH as EEPROM. Refer to AN2346 for information about using FLASH as EEPROM.

- A new mass erase routine requires a valid FLASH address loaded into the H:X register to perform an erase. This added step helps ensure that the erase routine is not inadvertently used to cause an unwanted erase. Also, on-chip FLASH programming routine ERARNGE variable CTRLBYT requires $00 for page erase and $40 for mass erase. The entire control byte must be set for proper operation.
- Separate routines will allow easy access to perform software SCI (Serial Communications Interface). For information on how to use on-chip FLASH programming routines refer to AN2635.
- Finally, there is improved security and robustness. The latest Monitor ROM implements updated security checks to make the program memory more secure.

3 Conversion Considerations

Enhancements lead to slight differences in operation from QYx Classic to the QYxA. There are a few points that should be considered in the conversion process.

- The Monitor ROM changed from 2 K to 1 K in size. This has led to the limitation that programming across page boundaries is no longer supported by the on-chip program range routine. Also, in very rare cases, ROM code improvements could cause customers to have to modify a few instructions in their application code. For example, when performing a mass erase, a valid address is required instead of an unspecified address.
- The QYxA contains new modules like the 10-bit ADC and OSC. In rare cases, new modules could cause customers to have to modify a few instructions in their application code. For example, if ADC code was written so that entire registers are configured without respect to reserve bits, then the ADC code will need to be revised to work correctly on the QYxA.
- The Reference Clock for ADC conversions has changed from the bus clock to the system clock (Bus Clock * 4). A change to the divide register may be necessary to set the reference clock to a specified value.

4 Code Changes Checklist

Below is a checklist that should be reviewed in the conversion process. This checklist will point out all the issues that should be addressed as your code is ported.

1. Does the original software use Auxiliary ROM routines (for example, Getbyte, Putbyte, delnus)?

   If so, the software will have to be changed to handle new Auxiliary ROM routines, addresses of these routines have changed in QYxA. Code will have to be changed to use the proper addresses.
2. Does the software use FLASH as EEPROM?

   If so, there are several possible issues for the page erase and mass erase routine. Software will have to be checked to ensure that proper procedure is used and the CTRLBYT is set with a MOV instruction not a BSET. Also, on-chip FLASH programming routines can no longer program across row boundaries
3. Does the code use the auto wake up timer and does the application depend on the typical auto wake time out?

   Since the timeout has been improved for QYxA it may be necessary to modify software to compensate for the change in timeout.
4. Bits changed in the OSCSC, CONFIG2, and ADC registers?

   Any code that writes to these registers should be reviewed to ensure that the writes are not affecting the changed bits
5. Does the code use external OSC, crystal, or RC?

   If so, since the OSCOPT bits have changed locations code will have to be updated to update these bits in their proper locations.
6. Does the code use the ADC?

   If so, because on QYxA the ADC clock is driven from 4XBUSCLK instead of BUSCLK changes to the ADC clock divider bits may be needed to maintain proper operation.

5 Development Tools

Development hardware used for QYx can be used with QYxA. The QYxA is pin-for-pin compatible with QY Classic and can be placed on existing QY4 Classic hardware. Existing Cyclone/Multilink tools and any programming or evaluation boards will work for the QYxA. Emulation can be done using the EML08QCBLTYE.

6 Differences in Packaging

All QYxA packages will be lead free. All packages that the QYx classic supported will be supported by the QYxA.

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