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Resetting MCUs

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Introduction

A simple function such as reset can cause many problems since different applications impose very different conditions on the start up and power down of the microcontroller unit (MCU). This document covers the main issues relating to reset and aims to lead the user of the M68HC05 and M68HC11 devices to a safe a reliable approach for the application.

Reset in its most basic function ensures that the MCU starts executing code in a controlled manner once power is applied. It may also be used to prevent the device running out of specification (often in conjunction with external devices) and can cause a system reset at the board level whenever the MCU has not executed the code in the expected way (watchdog).

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Factors which affect reset are:

1. External components attached to the RESET pin
2. Low-voltage reset (LVR) on chip
3. Power-on reset (POR) detection
4. System power-up sequence
5. Watchdog operation
6. Electrically erasable, programmable read-only memory (EEPROM) on chip
7. Battery backup
8. Device controls to its own power off
9. Partial power loss
10. HC05 clock source
11. Power applied resets

These factors are explained in detail later in this application note. In most applications several factors apply and so it may be a combination of these elements of reset functionality that must be considered for the safe operation of the MCU application.

Almost all HC05 and HC11 devices have an external 4-MHz or 8-MHz crystal and so it is assumed that the device will have a stable oscillator within 10 ms of V_{DD} reaching 4 V (5-V V_{DD} is also assumed, unless stated otherwise). Other possibilities for clock sources are discussed in **HC05 Clock Source**.

External Components Attached to the RESET Pin

At the simplest level, a battery connection is connected to the V_{DD} pin of the HC05 device and the V_{DD} reaches 4.5 V within 1 ms. This assumes a relatively small reservoir capacitor (for instance, 1 µF). In this case, the crystal oscillator will usually start between 5 ms and 10 ms after power on and the V_{DD} supply will be above the minimum allowed for the system clock. Remember that the 3-V specification normally includes reduced operating frequency.

In this case, the internal reset circuit of the HC05 device will hold reset low internally for the first 4064 system clock cycles (2 ms at 4-MHz clock). Thus, the internal reset will be released between 7 ms and 12 ms after power on. This arrangement simply requires a 10-kΩ pullup resistor externally on the RESET pin. Some HC05 devices have an internal resistor which means that the RESET pin may be left unconnected or simply have an external capacitor.

In a situation where the power supply takes more than 10 ms to reach 4 V, the oscillator is likely to have started up and the internal reset released before the V_{DD} pin reaches the minimum voltage for the particular clock frequency used in the application. This could cause incorrect device operation and a fatal error for the application is likely. In this case an external delay is necessary on the RESET pin.

The simplest delay is a resistor/capacitor (RC) network (see **Figure 1**) where the capacitor is charged up by the current flowing through the resistor until it reaches a level detected by the HC05 RESET pin circuitry as a logic 1 state. This value is normally defined as a minimum required V_{IH} of 0.7 x V_{DD}; however, the actual detection voltage is often much lower and can be as little as 0.5 x V_{DD} (2.5 V with a V_{DD} = 5.0 V). The RESET pin does have a Schmitt input but the hysteresis can be as little as 300 mV on some devices. The diode ensures that the capacitor discharges quickly with a sudden fall in V_{DD}; otherwise, the capacitor could keep the MCU powered up for a short time, especially if the MCU is in stop mode where power consumption is very low.

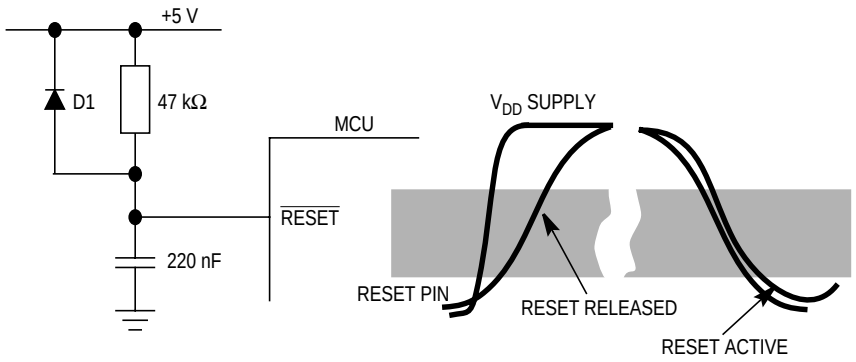


Figure 1. RC Network to Delay Reset Release by Approximately 10 ms

Ideally there would be no restriction on the values of the resistors and capacitors, but there are other considerations. Internal leakage currents for the RESET pin are normally specified at 1 μA maximum which means that the resistor has a maximum value of 100 kΩ and the capacitor should not be an electrolytic type to keep the stop current to a minimum. Ceramic capacitors are recommended as a compromise between low cost, low leakage, and good high-frequency response. The RESET pin capacitance is very low (less than 5 pF).

There are also limits for the minimum resistor impedance since the maximum pulldown current is approximately 5 mA at 1 V (V_{OL}). Together with the low-impedance voltage source of the external capacitor, it is necessary to ensure a minimum pullup resistor value of 2 kΩ. See **Watchdog Operation** for details of the output mode of the RESET pin where this feature is available on the device.

Low-Voltage Reset (LVR) On Chip

To protect against total or partial loss of power, some devices have an LVR circuit which effectively resets the device while the V_{DD} supply is lower than the trigger point. It is difficult to make an accurate voltage reference with high-density complementary metal oxide semiconductor (HCMOS) designs and so there is often a manufacturing tolerance built into the specification. As a consequence, the minimum trigger voltage can be sufficiently low that the device cannot run at the maximum bus speed for reliable operation before the LVR circuit resets the device. This restricts the maximum bus speed whenever the LVR circuit is used to protect the device from runaway.

Significant advantages of the built-in LVR circuit are the reliability of the integration of the LVR function and low cost. Additionally, the application can determine the presence of a low-power reset rather than an external reset. This can be achieved by the use of either separate vectors for the LVR and normal reset or by means of a register containing a reset condition status flag. This is of course not normally possible with an external LVR circuit.

EEPROM On Chip discusses protection for on-chip EEPROM where the use of an external LVR device is highly recommended.

Power-On Reset (POR) Detection

While the LVR circuit can protect against a partial power loss, the POR function can only indicate a total loss of power followed by power up. The V_{DD} supply must drop to less than 0.2 V to ensure that the POR register is reset correctly. On power up, a bit in one of the HC05 registers (often the miscellaneous register if it exists) will be set to a logic high state. This bit once cleared (by reading the bit) will remain in the logic low state even if an external reset occurs and only be reset to a 1 when the power is totally lost and returned.

System Power-Up Sequence

When power is applied to the system, it will normally take a finite period to achieve the designed operating voltage. During this time, the MCU may be required to maintain a specific state on its output pins and hold off any execution of code until it is safe to commence running the application.

Once power is applied to an HC05 device, the oscillator will start running whether reset is held in the active state or not. Of course the oscillator takes a short time to start up (4-MHz crystals take about 5 ms to start and 32-kHz crystals take much longer, often as much as 500 ms), but once the first couple of clocks have occurred, the active state (logic 0) of the RESET pin normally configures the port lines to be inputs or to a known state if they are only able to operate in output mode. In this way, the external circuitry can assume a known state on the MCU pins just a short time after power on but before the MCU reset is released.

Please remember that the port data registers are not usually initialized by power on or reset and so a reset will normally leave the port data unchanged and simply place the port in input mode.

Care should be taken not to force excessive current into the MCU during this time in case a latch-up condition arises. It is likely that some external voltages could rise much faster than the MCU V_{DD} supply, especially since care is needed in most cases to ensure that the V_{DD} supply is a good clean and preferably noise free power source. A simple method is to place in-line resistors on port pins that could see voltage levels in excess of the rising V_{DD} supply, and diodes to clamp the maximum difference between V_{DD} and the port pin voltage to less than 0.6 V. A good value for the resistor is normally about 50 Ω since there is normally a maximum allowed current per pin of 20 mA and, it is assumed that the external voltage is an absolute maximum of 1 V greater than V_{DD} in worst case circumstances. Similarly a negative voltage, below V_{SS} (0 V in most applications) must be current limited to avoid damage to the MCU.

Another phenomenon is the ability of low-power HC05 devices to be powered up by an oscillating signal attached to the port pin of the HC05, while the HC05 device is powered off. This occurs due to current being forced into the V_{SS} and V_{DD} supply via the inherent port protection diodes to both power supply rails within the MCU. As long as the current is limited to 20 mA total for all pins in this state, no harm will come to the MCU. However, it is important to keep the MCU in the reset condition while powered off, at least so that during power up the MCU does not drive data onto the port and draw a large current. While such current is flowing, functionality of the MCU is not guaranteed due to the possibility of substrate currents changing the state of the internal logic gates.

Often the reset signal is used by other sections of the application to start up after the power-on sequence is complete and so it is possible that the reset line is distributed throughout the board. Some devices will be released from reset after different voltages on the reset signal and so it is advisable to bring this signal up to V_{DD} within the rest delay time (normally 4064 cycles) to avoid the MCU coming out of reset before other parts of the board have done the same. This is particularly important when there are several printed circuit boards (PCBs) and multiple MCU devices talking to one another.

Watchdog Operation

The watchdog is the computer operating properly (COP) function that forces a reset of the HC05 device if the counter is not cleared before it overflows. The timeout of the counter varies between devices, but in most cases the RESET pin is driven low for a short time when the COP times out and thus resets the HC05. The timing of the COP reset is shown in **Power-On Reset and External Reset Timing for the MC68HC05J1**. There is no oscillator start-up delay, and so the reset vectors are fetched within 3 cycles of reset going high.

Some HC05 devices have no buffering internally and so the external voltage seen on the RESET pin is the actual signal that forces the reset. More recently designed HC05 devices have the reset signal from the COP buffered internally so that the external load has no effect on the COP reset timing or functionality.

With unbuffered COP output on the RESET pin, the maximum external capacitance or minimum possible pullup resistance on the RESET pin are critical as these determine the timing and level of the COP reset output signal.

Check the data sheet for details of the HC05 device COP function but, where there is any uncertainty a good working limit is a maximum capacitance of 1 μF and a minimum pullup impedance of 2 kΩ.

EEPROM On Chip

Integrating EEPROM into the HC05 device is increasingly common but may cause several problems during power up and power down.

Normally the EEPROM array would be initialized, at least in part, during the production phase. The application normally makes further writes to the EEPROM in addition to reading the data and so it is unlikely that the EEPROM could be physically protected from unexpected writing.

Certain conditions such as partial power loss can cause the HC05 to run at a higher frequency than allowed for the current V_{DD} voltage level and

this in turn can result in the HC05 running away by incorrectly reading ROM or RAM.

The best solution to such problems is the use of a low-voltage reset circuit (such as the MC34064 and MC34164 devices) which force reset low whenever the V_{DD} supply drops below 4.65 V. See **Figure 2**.

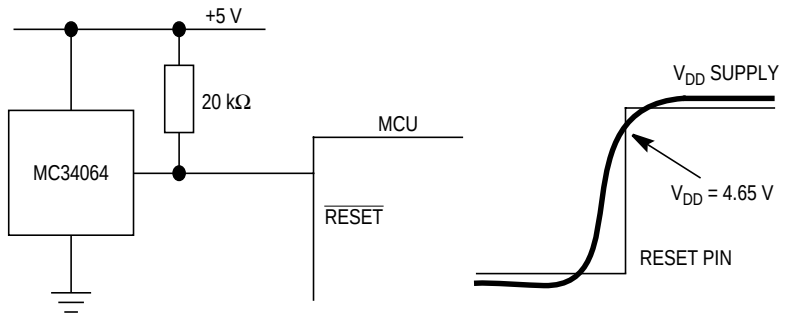


Figure 2. MC34064 Low-Voltage Reset Device Application

It is often assumed that EEPROM is erased or incorrectly written during power up, but normally it is during power down that the erroneous EEPROM activity occurs.

NOTE: *The power-down voltage decay is often slow and the lack of any low-voltage reset device could allow the MCU to run at too high a frequency for the current V_{DD} for several tens of milliseconds (plenty of time for several erases and writes to EEPROM).*

Battery Backup

The usual purpose for battery backup operation is to avoid resetting the MCU when the main power is removed. There comes a point though, when the battery also fails and this can cause the voltage on the system to drop very gradually. To save the battery from damaging itself, it is usual to have low-voltage detection circuits that force a system reset as the power drops below a critical level. In these circumstances, it is often necessary to save the current status of the MCU before the reset occurs and so it is likely the system will first warn the MCU of the pending reset.

The MCU can perform a number of read and writes to EEPROM or RAM which could be independently backed up and a good practice is to place the MCU in low-power stop mode, ensuring first that all outputs are in a low-current state. This way, the device is in a secure state and ready for reset to be applied with no risk of a partially completed saving of system data.

Stop mode is ideal for power down as the port lines are all in a known state and there is a reset delay time (4064 cycles in most devices) before the device can resume operation. In this way a slow decay of the V_{DD} supply poses no problems as long as reset is held low once the V_{DD} supply passes below the minimum specified for the current clock frequency.

Device Controls Its Own Power Off

An application that does not have a battery backup but which is required to save power may switch itself off by activating an external control of the power supply. Clearly as the power is being switched off, the MCU could see external pins change state and interpret the signals wrongly. If care is not taken to place the MCU in a dormant state before the power supply voltage drops below the safe level for MCU operation, the MCU could run away and cause a power on to be initiated again.

Partial Power Loss

The only way to protect against failure of the application during partial power loss is to install a lower voltage detection and reset circuit. Some MCU devices have these built into the design and these will force the RESET pin low (active state) to reset the MCU and any other external devices that use the reset signal.

A power-on reset (POR) bit will not usually register a partial power loss so on coming out of reset, the MCU will not be aware that the V_{DD} voltage dropped before reset occurred.

Once the reset signal is applied, the MCU pins will mostly go to high-impedance state and the oscillator will stop running, thus making the system power consumption lower and this can allow a more graceful power down of the system.

HC05 Clock Source

Different types and frequencies of oscillator circuits take differing lengths of time to start up and stabilize. A 4-MHz crystal takes about 5 ms while a 4-MHz ceramic resonator will usually start up very quickly (normally less than 1 ms). As the frequency drops, the time taken to start up and stabilize increases. A 32-kHz crystal can take as long as 500 ms to start up. The internal clock count delay accommodates these differences since it simply counts the oscillations and it is assumed that 4064 clocks is enough under most conditions. If a different amount of time is required then of course an external reset control is needed.

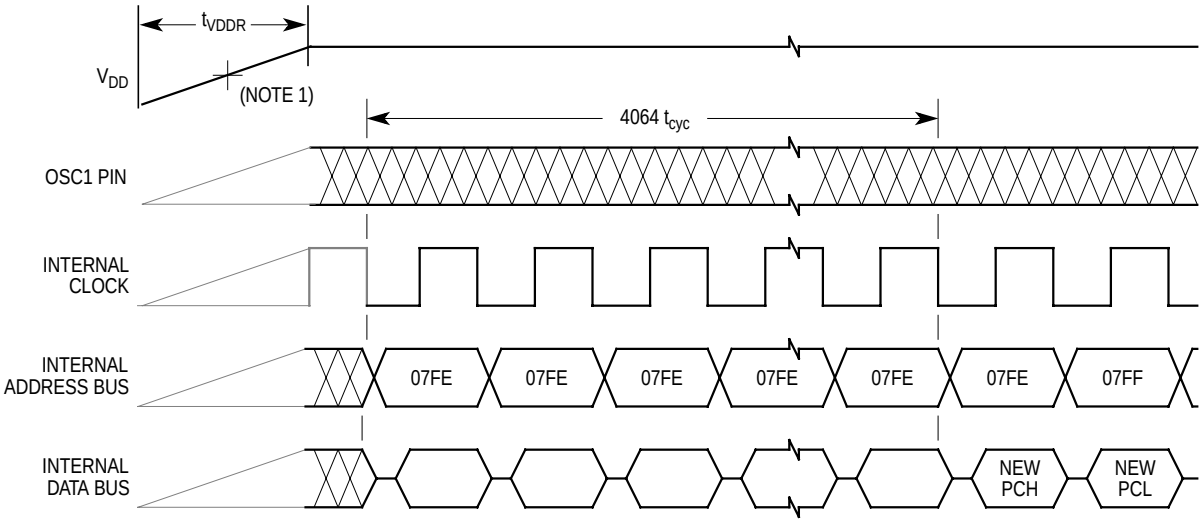
An RC (resistor-capacitor) option rather than external crystal or resonator has much poorer accuracy of oscillator frequency but has virtually instantaneous start up and is very cheap.

Some applications provide an external clock source rather than use the crystal oscillator option. In these cases the clock source may be present but the MCU may be in reset. When the reset signal is released the application may be able to operate more quickly and so some HC05 devices have options for the delay time for system operation after reset is released. Since 4064 cycles is 2 ms with a 4-MHz clock, shorter delays are often required.

Power Applied Reset

It is often a requirement of the application that an external circuit controls the reset of the MCU. In these conditions, reset may be applied and released without power down of the application. The 4064-cycle delay is only applicable to a power-on condition or after the MCU comes out of stop mode. In each case the oscillator must be restarted and so a short delay for the oscillator to stabilize is required. When a reset pulse is subsequently received, the oscillator continues to run and there is no start-up delay. See **Power-On Reset and External Reset Timing for the MC68HC05J1** for timing diagrams showing power-on reset and the external reset. The minimum low time for the reset pulse is 1.5 times the bus cycle time to ensure that a full reset occurs. It is up to the user to ensure that the minimum low time is met. A shorter low time may cause a partial reset of the MCU.

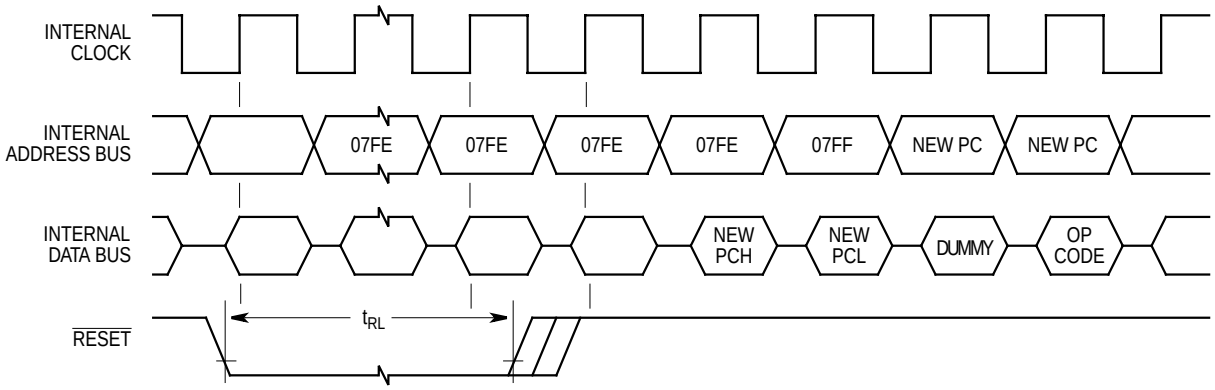
Power-On Reset and External Reset Timing for the MC68HC05J1



Notes:

1. Power-on reset threshold is typically between 1 V and 2 V.
2. Internal clock, internal address bus, and internal data bus are not available externally.

Figure 3. Power-On Reset Timing



Notes:

1. Internal clock, internal address bus, and internal data bus are not available externally.
2. The next rising edge of the internal clock after the rising edge of $\overline{\text{RESET}}$ initiates the reset sequence.
3. At 5-V V_{DD}:
   t_{VDDR} = V_{DD} supply rise time
   t_{RR} = $\overline{\text{RESET}}$ pulse width — minimum 1.5 t_{cyc}
   t_{cyc} = cycle time — minimum 476 ns

Figure 4. External Reset Sequence

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