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Differences Between the HC08GP32 and the HC908GP32 and Code Conversion Considerations

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Overview

This document describes the differences between the MC68HC08GP32 (HC08GP32) and the MC68HC908GP32 (HC908GP32), and the requirements/considerations for converting code from the HC08GP32 to the HC908GP32.

Differences Between the Devices

The HC908GP32 is the FLASH version of the HC08GP32. **Table 1** shows the differences between the two parts.

Table 1. Differences

	MC68HC08GP32	MC68HC908GP32
User Memory	32,256 bytes ROM	32, 256 bytes FLASH
User Vectors	36 bytes ROM	36 bytes FLASH
Registers at $001E and $001F	Mask Option Registers [1]: $001E – MOR2 $001F – MOR1	Configuration Registers [2]: $001E – CONFIG2 $001F – CONFIG1
Registers at $FE08 and $FF7E	Not used: Locations are reserved	FLASH Related Registers: $FE08 – FLCR $FF7E - FLBPR
Bit 2 at $FE01	Not used: Bit is reserved	MODRST bit Forced monitor mode entry
Monitor ROM	Used for testing only	Used for testing and FLASH programming/erasing
Packages	42-pin SDIP 44-pin QFP	40-pin PDIP 42-pin SDIP 44-pin QFP

1. The mask options registers are read-only registers. Values in the registers are defined by mask options (hard-wired connections) specified at the same time as the ROM code submission.

2. The configuration registers are write-once after reset. Values in the registers are defined by the user's software.

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Code Conversion: HC80GP32 to HC908GP32

Due to aforementioned differences, some details must be considered in the user's software and setup when the HC08GP32 is replaced with the HC908GP32.

The following sections describe each item required for the conversion.

CONFIG1 and CONFIG2 Registers

The HC08GP32 has mask option registers MOR1 and MOR2. Instead of these mask option registers, the HC908GP32 has configuration registers CONFIG1 and CONFIG2. These registers must be initialized by the user's software. Usually the initialization is performed just after reset. Since the registers are write-once registers, they can not be rewritten until the next reset.

Here is an example of code that must be added to initialize the CONFIG1 and CONFIG2 registers:

```
mov   #$0A,CONFIG1   ;Enable the LVI 5V mode and STOP instruction
mov   #$01,CONFIG2   ;Select the internal bus clock for the SCI
```

FLASH Block Protection

The MC68HC908GP32 has the FLASH protection register (FLBPR) located at $FF7E. This register consists of FLASH and protects the user's code from unintentional programming and erasing. Freescale strongly recommends that the user protect the entire contents of FLASH. The protection register and the user memory can be programmed at the same time.

Here is an example of the recommended FLASH block protect setup code:

```
FlashProtect  equ  $00
              org  FLBPR
              db   FlashProtect  ;Protect a whole Flash array
```

CAUTION: *The presence of voltage V_{tst} on the IRQ pin will bypass the block protection in spite of the value in the FLASH block protect register. Do not apply V_{tst} to the $\overline{IRQ}$ pin unless in monitor mode or programming/erasing FLASH.*

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