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How to Calculate Instruction Times on the MC68HC16

By   Sharon Darley
     Austin, Texas

Introduction

The M68HC16 Family *CPU16 Reference Manual* Rev. 2, Motorola document order number CPU16RM/AD, explains how to calculate instruction timing in Chapter 8. This detailed chapter includes examples.

A supplement to Chapter 8, this engineering bulletin summarizes the most important points in the chapter and explains some of the examples in more detail.

In general, an important concept to remember when reading through this material is that memory accesses are made up of bus cycles, which are made up of clock periods. Execution time can be described by this expression:

$$\left[\left(\text{program access} \times \frac{\text{bus cycles}}{\text{program access}} \times \frac{\text{clocks}}{\text{bus cycle}}\right) + \left(\text{operand access} \times \frac{\text{bus cycles}}{\text{operand access}} \times \frac{\text{clocks}}{\text{bus cycle}}\right)\right] \times \frac{\text{seconds}}{\text{clock}}$$

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General Information

If you are using 2-clock bus cycles (fast termination), simply look up the instruction time in Table 6-3 in the *CPU16 Reference Manual*. This table lists the number of clock cycles (also referred to as clock periods) for each instruction. However, if your bus speed is slower (with more than two clock periods in each bus cycle), the instruction times will be longer than those given in Table 6-3. In this case, you must calculate the instruction time yourself.

To acquire a copy of the reference manual, order it from the Literature Distribution Center or find it on the Web at http://motorola.com.sps/.

Read Section 1. Execution Time Components in the reference manual and then read the summary in this bulletin. Repeat this process for each section in Chapter 8 that corresponds to the sections that follow here.

Execution Time Components

A memory access is made up of bus cycles. The number of bus cycles in each memory access depends on the size of the data bus, the size of the access, and whether the access is aligned or misaligned. All instructions are an even number of bytes. This means that an access will be aligned if the program begins on an even boundary and does not have any uneven gaps (such as space reserved for constants) in the middle.

Table 1 shows how to determine the number of bus cycles in a particular access.

A bus cycle is made up of clock periods. A bus cycle requires a minimum of two clock periods. Internal accesses and fast termination external accesses are examples of bus cycles that are two clock periods long. Other external accesses are longer. Each wait state adds one clock period to the bus cycle. Thus, zero wait states means a 3-clock bus cycle, one wait state means a 4-clock bus cycle, two wait states means a 5-clock bus cycle, and so on.

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The CPU16 executes only one instruction at a time. To calculate the total time to execute a particular set of instructions, sum the individual execution times of each instruction in the set.

Total execution time for an instruction is calculated using the expression:

$$CL_T = CL_P + CL_O + CL_I$$

Where:

CL_T = Total number of clock periods for the instruction

CL_P = Number of clock periods used for program access

CL_O = Number of clock periods used for operand access

CL_I = Number of clock periods used for internal operation

Program and Operand Access Time

Program Accesses   For all instructions except those that cause a change in program flow, there is one program access per instruction word. The actual number of bus cycles required for the program access will vary, depending on the bus size. Program accesses are always word sized and are always aligned with even byte boundaries.

Table 1 shows how to determine the number of bus cycles for a particular access, given the bus size. Keep in mind that this table gives the number of bus cycles, not the number of clock periods, in those bus cycles. See **Table 2** to determine the number of accesses for change of flow instructions.

Table 1. Number of Bus Cycles Per Access

Access Size	8-Bit Data Bus	16-Bit Data Bus Aligned	16-Bit Data Bus Misaligned
Byte	1	1	—
Word	2	1	2
Long word	4	2	4

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Operand Accesses

Most instructions require one operand access per operand. The exceptions are listed in the following paragraphs. Note that immediate operands are considered to be part of the instruction and do not contribute to the instruction execution time. Once you determine how many operand accesses are required for a particular instruction, use **Table 1** to determine how many bus cycles are in each access.

Read-Modify-Write Instructions

The instructions ASL, ASR, BCLR, BSET, COM, DEC, LSR, NEG, ROL, and ROR require two accesses per operand. Note that the mask used in bit clear and set instructions is considered to be an immediate operand.

Change-of-Flow Instructions

See **Table 2** for the number of accesses.

Table 2. Change-of-Flow Instruction Timing

Instruction	Operand Access	Program Access
BRA, BRN, LBRA, JMP	0	3
Short conditional branches	0	3/1*
LBRN	0	2
Long conditional branches	0	3/2*
BRCLR BRSET (IND8)	1	4/3*
BRCLR, BRSET (EXT/IND16)	1	5/3*
JSR, BSR, LBSR, RTS, RTI	2	3
SWI	3	3

* In program access values for conditional branches, the first value is for branch taken, and the second value is for branch not taken.

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Other Special Cases

See **Table 3** for the number of accesses for other special cases.

Table 3. Timing for Other Special Cases

Instruction	Operand Access	Program Access
PSHA/PSHB/PULA/PULB	1	1
PSHM	Num regs pushed	1
PULM	Num regs pulled + 1	1
PSHMAC/PULMAC	6	1
LPSTOP	1 (only when CCR S bit = 0)	1
WAI	0	1
MOVB/MOVW (IXP to EXT, EXT to IXP)	2	2
MOVB/MOVW (EXT to EXT)	2	3
MAC	2	1
RMAC	2N (N = num iterations)	1

Internal Operation Time

The number of clock periods required for internal operation during the execution of an instruction remains constant regardless of the bus speed.

$$CL_I = CL_T - (CL_P + CL_O)$$

For this calculation, assume that all program and operand accesses are aligned on a 16-bit data bus and that each bus cycle takes two clock periods.

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Calculating Execution Times for Slower Accesses

To calculate execution times for slower accesses, follow these steps:

1. First, look up CL_T for a 2-clock bus cycle in **Table 6-3** in the *CPU16 Reference Manual*.

2. Next, calculate CL_P and CL_O assuming a 2-clock bus cycle and a 16-bit aligned data bus.

3. Using these numbers, calculate CL_I as $CL_T - (CL_P + CL_O)$.

4. Now, recalculate CL_P and CL_O for the actual bus speed and size that you will be using.

5. Finally, calculate CL_T as $CL_P + CL_O + CL_I$.

Examples

LDD IND8, X In this example, assume a 16-bit operand data bus with two clocks per bus cycle (fast termination) and a misaligned access.

Assume an 8-bit program data bus with three clocks per bus cycle (0 wait states).

Table 6-3 in the *CPU16 Reference Manual* shows that CL_T for this instruction is six clock periods for fast termination.

Calculate CL_P and CL_O for fast termination, assuming that all program and operand accesses are aligned on a 16-bit data bus. Since the LDD instruction is not a special case, it requires one operand access and one program access. **Table 1** shows that for a 16-bit aligned data bus and a word access size, there is one bus cycle per access. Thus,

$$CL_O = (1 \text{ access}) \times \frac{(1 \text{ bus cycle})}{\text{access}} \times \frac{(2 \text{ clock periods})}{(\text{bus cycle})} = 2 \text{ clock periods}$$

Similarly, CL_P will also be two clock periods.

$$CL_T - (CL_P + CL_O) = 6 - (2 + 2) = CL_I = 2 \text{ clock periods}$$

Recalculate CL_P and CL_O for the actual bus speed and bus size. **Table 1** shows that for a 16-bit misaligned data bus and a word access size, there are two bus cycles per access. Likewise for an 8-bit data bus and a word access size, there are two bus cycles per access.

Thus,

$$CL_O = (1 \text{ access}) \times \frac{(2 \text{ bus cycles})}{\text{access}} \times \frac{(2 \text{ clock periods})}{(\text{bus cycle})} = 4 \text{ clock periods}$$

$$CL_P = (1 \text{ access}) \times \frac{(2 \text{ bus cycles})}{\text{access}} \times \frac{(3 \text{ clock periods})}{(\text{bus cycle})} = 6 \text{ clock periods}$$

$$CL_T = CL_P + CL_O + CL_I = 6 + 4 + 2 = 12 \text{ clock periods}$$

BNE

In this example, assume a 16-bit operand and program data bus with five clocks per bus cycle (two wait states). Assume that the accesses are aligned. Also assume that the branch is taken.

Table 6-3 in the *CPU16 Reference Manual* shows that CL_T for this instruction is six clock periods for fast termination and the branch taken.

Calculate CL_P and CL_O for fast termination, assuming that all program and operand accesses are aligned on a 16-bit data bus. **Table 2** shows that BNE requires 0 operand accesses and three program accesses for the branch taken. **Table 1** shows that for a 16-bit aligned data bus and a word access size, there is one bus cycle per access.

Thus,

$$CL_O = (0 \text{ accesses}) \times \frac{(1 \text{ bus cycle})}{\text{access}} \times \frac{(2 \text{ clock periods})}{(\text{bus cycle})} = 0 \text{ clock periods}$$

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$$CL_P = (3 \text{ accesses}) \times \frac{(1 \text{ bus cycle})}{\text{access}} \times \frac{(2 \text{ clock periods})}{(\text{bus cycle})} = 6 \text{ clock periods}$$

$$CL_T - (CL_P + CL_O) = 6 - (6 + 0) = CL_I = 0 \text{ clock periods}$$

Recalculate CL_P and CL_O for two wait states.

$$CL_O = (0 \text{ accesses}) \times \frac{(1 \text{ bus cycle})}{\text{access}} \times \frac{(5 \text{ clock periods})}{(\text{bus cycle})} = 0 \text{ clock periods}$$

$$CL_P = (3 \text{ accesses}) \times \frac{(1 \text{ bus cycle})}{\text{access}} \times \frac{(5 \text{ clock periods})}{(\text{bus cycle})} = 15 \text{ clock periods}$$

$$CL_T = CL_P + CL_O + CL_I = 15 + 0 + 0 = 15 \text{ clock periods}$$

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