EB00942

S32G3 NoC Configuration

Rev. 1.0 — 5 September 2024 Engineering bulletin

1 Introduction

Network-on-Chip (NoC) is an interconnect matrix that supports communication between various initiators and targets. In NoC interconnects, Quality of Service (QoS) is the statistical allocation of throughput and delay. It is defined in terms of bandwidth and latency to the transactions transported between the initiators and the targets.

This document provides NXP's updated configurations of the NoC interfaces on the controllers of the S32G3 family. These updated configurations are based on the device validation and are targeted to better ensure bandwidth availability for all transactions on the NoC. It is mandatory to apply these new settings.

Note: *These configurations are not applicable for S32G2, which uses the default configuration.*

2 Programming the updated NoC QoS settings

The default NoC settings are done in the NoC hardware design and are applied automatically at device reset. NXP mandates to overwrite these settings with the attached settings. These settings have gone through exhaustive testing during the validation of the device and have proven to be optimal for the part's intended target applications. Changes to these settings may result in degradation of system performance.

The attached settings should be written once after every reset (POR, destructive reset, functional reset, or Standby exit) and should be one of the first things that the software needs to perform, before there is any significant traffic on the NoC. Dynamic configuration of these parameters can cause system instabilities. Therefore, these configuration parameters should not be altered after they are initially set.

Any of the available cores (Cortex-A53® or Cortex-M7®) can initiate these writes. However, it is recommended that these settings are applied by the core that boots first, before there is any significant traffic on the NoC. The core can perform these register writes in any sequence. However, after every reset, it must be ensured that the configurations are not being written twice in a multi-core boot setup.

If the customer use case includes resetting RD1 (Software Reset Domain/Partition 1) on-the-fly at runtime, the application must check and update the corresponding NoC QoS settings, which may have reverted to the HW default values in a read-compare-update (if not set to the desired value) manner, after enabling (turning on) RD1 and before starting any core in RD1.

If the customer use case includes resetting RD2 (Software Reset Domain/Partition 2), RD3 (Software Reset Domain/Partition 3) or both on-the-fly at runtime, there is no need to update any NoC QoS setting after re-enabling (re-turning on) either of these domains (partitions).

In this document, the NoC QoS settings are divided into two groups, one for all domains (partitions) except RD1, and the other for RD1 only. The former group is referred to as FlexNocConfigs_M7 and the latter group is referred to as FlexNocConfigs_A53.

2.1 Prerequisites for programming the updated NoC QoS settings

The following are the prerequisites for programming the updated NoC QoS settings.

- To apply FlexNocConfigs_M7 on S32G3, the Interconnected Interfaces of RD2 and RD3 must be enabled through related RDC registers, to allow writing of the settings to the desired register spaces on NoC. Failing to do so may result in hard fault on M7 or Bus error on A53 because of the register inaccessibility.

- To apply FlexNocConfigs_A53 on S32G3, RD1 must be enabled (turned on), to allow writing of the settings to the desired spaces on NoC and Ncore. Failing to do so may result in hard fault on M7 or bus error on A53 because of the register inaccessibility.

Note:

To avoid potentially significant traffic going through the NoC during the update of the NoC registers, the following points should be noted.

- *If M7_0 is the first core to boot and run the bootloader, then M7_0 programs the updated NoC QoS settings in the bootloader. RD2, RD3, all other M7 cores in the Main Reset Domain, and all A53 cores in RD1 should remain off (reset), until the programming process is complete.*
- *If A53_0 is the first core to boot and run the bootloader, then A53_0 programs the updated NoC QoS settings in the bootloader. RD2, RD3, all M7 cores in the Main Reset Domain, and all other A53 cores in RD1 should remain off (reset), until the programming process is complete.*

2.2 Steps to program the updated NoC QoS settings using the NXP example bootloader

The following steps are required to program the updated NoC QoS settings using the NXP example bootloader.

1. Download the NXP example bootloader available within the GoldVIP for S32G3 1.13.0 release onwards.
   Note: *Due to the known software issues, NXP example bootloaders from GoldVIP (versions earlier than 1.13.0) or from S32G3 Platform Software Integration (versions till 2023.11) cannot work well with applying FlexNocConfigs_A53 on S32G3.*
2. To apply the updated NoC QoS configurations, make sure the checkbox - "Enable FlexNoC Registers" is enabled.
3. To ensure that all NoC QoS settings are updated before the bootloader starts any application (core), make sure the checkbox - “Start Applications Synchronously” is enabled.

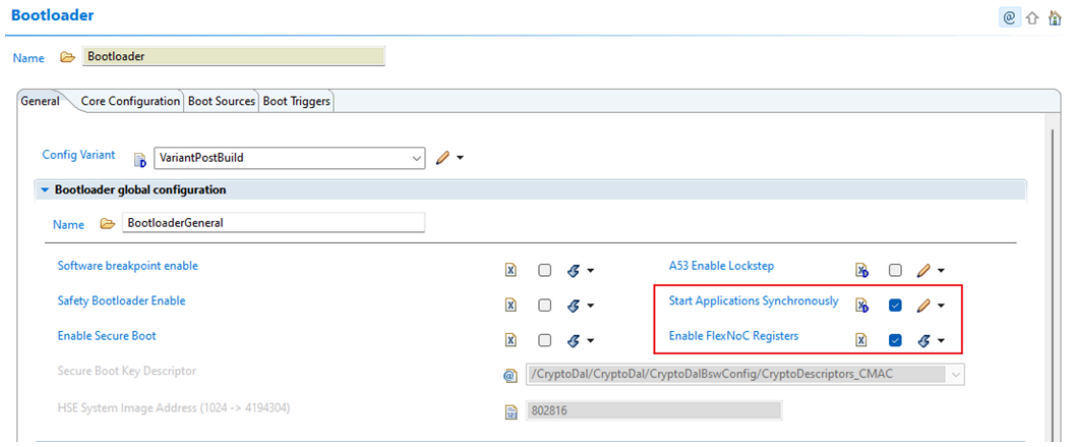

Figure 1. Enabling checkboxes in the bootloader plugin

4. Configure the core configuration for both M7_0 and A53_0.

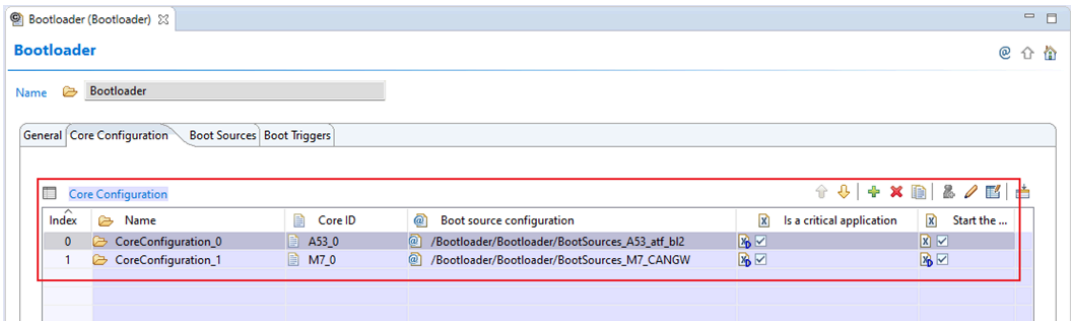

Figure 2. Core configuration in the bootloader plugin

Note: *In the NXP example bootloader, the FlexNocConfigs_M7 is only applied if M7_0 is correctly configured in the core configuration panel. The FlexNocConfigs_A53 is only applied if A53_0 is correctly configured in the core configuration panel.*

5. Optionally configure the core configuration for other cores based on actual usage.
6. Generate code for all configurations and build the bootloader.

After completing all the above steps, the bootloader will update FlexNocConfigs_M7 and FlexNocConfigs_A53 before starting any application (core).

2.3 Steps to program the updated NoC QoS settings using a custom bootloader

The following steps are required to program the updated NoC QoS settings using a custom bootloader.

1. Download FlexNOC_Init.h and FlexNOC_Init.c by either of the following methods.
   - Download the files from the attachments of this document.
   - Download the files from the NXP example bootloader available within the GoldVIP for S32G3 1.13.0 release onwards.

   The FlexNOC_Init.h and FlexNOC_Init.c contain the FlexNocConfigs_M7 and FlexNocConfigs_A53 in array form, and the function FlexNOC_InitNoc() which is used to apply FlexNocConfigs_M7 and FlexNocConfigs_A53.
2. To update NoC registers with FlexNocConfigs_M7, ensure the following:
   - Check the interconnect interface status of RD2. If the interconnect interface is not enabled, enable it before further operations.
   - Check the interconnect interface status of RD3. If the interconnect interface is not enabled, enable it before further operations.
   - Update the NoC registers with FlexNocConfigs_M7 by calling the function FlexNOC_InitNoc(CORE_ID_M7_0).

   The following function is an example of checking the interconnect interface status of a specific software reset domain and enabling the interconnect interface of that software reset domain if it is not enabled.

```c

/* Available Software Reset Domains */
typedef enum
{               /*--- Software Resettable Domains ---*/
    RD1 = 1,    /* Software Reset domain 1: Cortex-A53   */
    RD2 = 2,    /* Software Reset domain 2: PFE          */
    RD3 = 3     /* Software Reset domain 3: LLCE         */
} SoftwareResetDomainType;

#define E_NOT_OK                        0x01U
#define E_OK                            0x00U
#define TIMEOUT_CNT_INIT_VALUE          0xffffU
#define TIMEOUT_CNT_END_VALUE           0x0U
#define RD_INTERCONNECT_STAT_MASK       0x10U
#define RD_INTERCONNECT_DISABLE_MASK    0x8U
#define RD_CTRL_REG_UNLOCK_MASK         0x80000000U

StatusType EnableSRDInterconnectInterface(SoftwareResetDomainType domain)
{
    StatusType status = E_OK;
    uint16_t timeout = TIMEOUT_CNT_INIT_VALUE;
    __IO uint32_t *ctrlReg;
    __I uint32_t *statReg;

    switch (domain)
    {
        case RD1:
            ctrlReg = &IP_RDC->RD1_CTRL_REG;
            statReg = &IP_RDC->RD1_STAT_REG;
            break;

        case RD2:
            ctrlReg = &IP_RDC->RD2_CTRL_REG;
            statReg = &IP_RDC->RD2_STAT_REG;
            break;

        case RD3:
            ctrlReg = &IP_RDC->RD3_CTRL_REG;
            statReg = &IP_RDC->RD3_STAT_REG;
            break;

        default:
            return E_NOT_OK;
    }

    if ((*statReg & RD_INTERCONNECT_STAT_MASK) != 0U) /* not already enabled */
    {
        /* Unlock the software reset domain control register for writing */
        *ctrlReg |= RD_CTRL_REG_UNLOCK_MASK;

        /* Enable the interconnect interface of software reset domain */
        *ctrlReg &= ~RD_INTERCONNECT_DISABLE_MASK;

        /* Wait for software reset domain status register */
        /* to acknowledge interconnect interface enabled */
        while (((*statReg & RD_INTERCONNECT_STAT_MASK) != 0U) && (timeout--)) continue;

        if (TIMEOUT_CNT_END_VALUE != timeout) /* Reset domain init success */
        {
            status = E_OK;
        } else
        {
            status = E_NOT_OK;
        }

        /* Relock the software reset domain control register */
        *ctrlReg &= ~RD_CTRL_REG_UNLOCK_MASK;
    }

    return status;
}

```

Figure 3. Example function

3. To update NoC registers with FlexNocConfigs_A53, ensure the following:
   - Check if partition 1 is enabled (turned on). If partition 1 is not enabled (turned on), enable (turn on) it before further operations.
   - Update the NoC registers with FlexNocConfigs_A53 by calling the function FlexNOC_InitNoc(CORE_ID_A53_0).

   Refer to the S32G3 reference manual to enable (turn on) partition 1. Alternatively, refer to the function BI_EnablePartition() defined in Bootloader_Specific.c in the NXP example bootloader to enable (turn on) partition 1.

4. Start applications (cores).

For more SW implementation details, see the NXP example bootloader within the GoldVIP for S32G3 1.13.0 release onwards.

3 Revision history

Table 1. Revision history

Document ID	Release date	Description
EB00942 v. 1.0	5 September 2024	• Updated document title from “S32G3 NoC Recommendations” to “S32G3 NoC Configuration”. • Updated the title of Section 2 from "Programming new QoS settings" to "Programming the updated NoC QoS settings". • In Section 2 added three paragraphs on the clarifications on the sequence of registers. • Updated the title of Section 2.1 from "Prerequisites for programming the updated QoS settings" to "Pre-requisites for programming the updated NoC QoS settings". • Added sections Section 2.2 and Section 2.3. • Updated and modified the attachments FlexNOC_Init.c and FlexNOC_Init.h.
EB00942 v. 0	March 2023	Initial Revision

4 Note about the source code in the document

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