S32E27

S32E2 Data Sheet

Rev. 5 — 3 December 2024 Product Data Sheet

- This document provides electrical specifications for S32E2, which includes the Application Extension (AE) subsystem.
- For functional characteristics and the programming model, see the S32E2 Reference Manual.

1 Introduction: S32E2/S32Z2 Family

1.1 Overview

S32E2 and S32Z2 are 32-bit Arm®-based real-time processors. They target real-time applications that require low latency and high performance, including applications for:

- Braking
- Hybrid and electric vehicles (HEVs/EVs)
- Safety
- Chassis
- Domain control

S32E2 builds on and expands NXP's HEV/EV portfolio that includes products such as MPC5744P, MPC5777C, MPC5775B, and MPC5775E. S32E2 is an EV integration platform that supports applications such as:

- Electric traction motor control
- Hybrid control unit (HCU) control
- Advanced combustion engine management

S32Z2 is a safety and domain controller that supports applications such as:

- Drive-by-wire
- Chassis control
- Autonomous vehicle drive control
- Domain control
- Battery management systems (BMS)

S32E2 and S32Z2 are developed with 16 nm FinFET technology and target ISO 26262 Automotive Safety Integrity Level D (ASIL D).

1.2 Block diagram

Figure 1 shows the chip components. In this figure, orange component blocks vary across S32E2 and S32Z2. For details, see Feature summary.

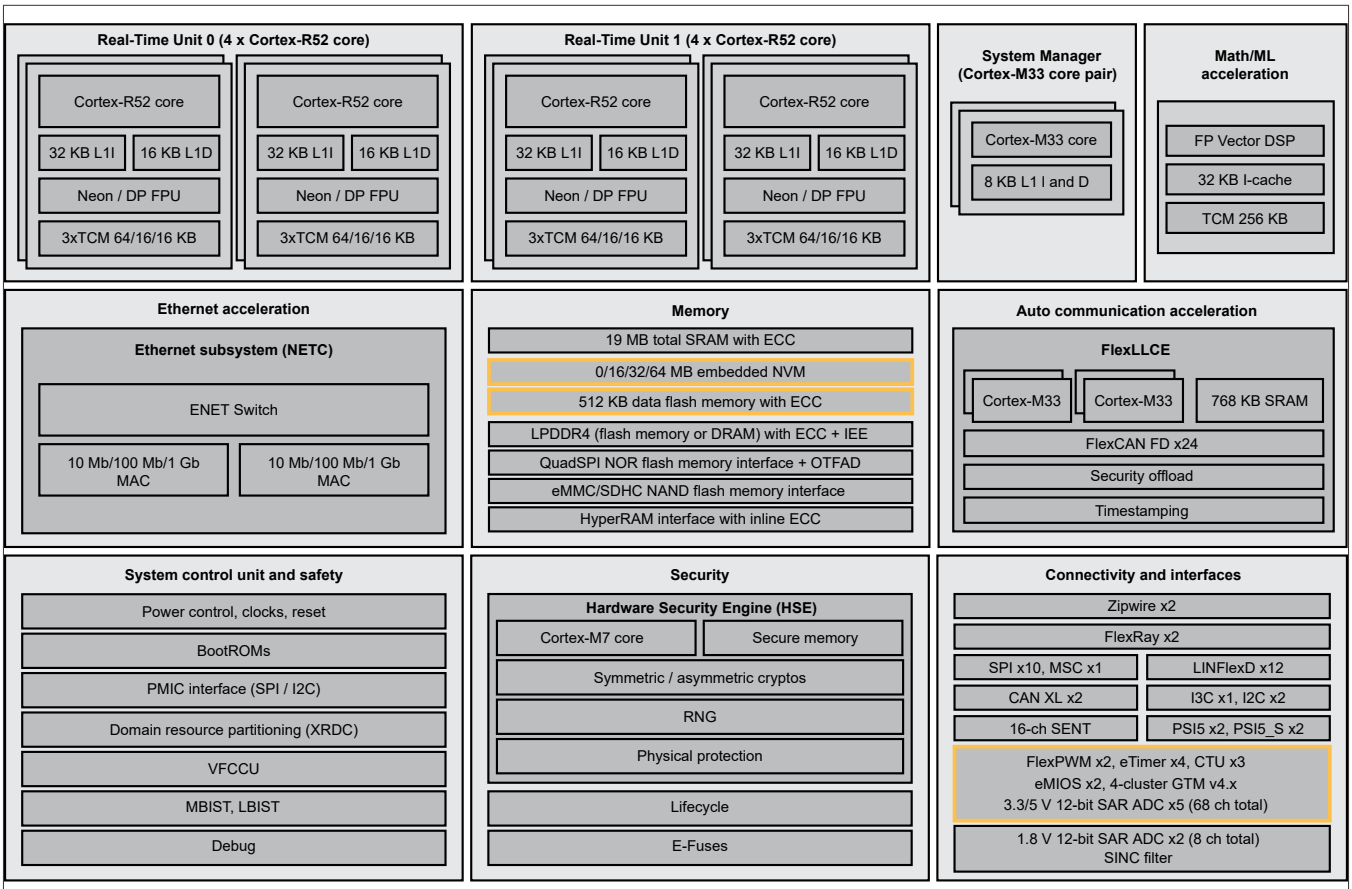

Figure 1. Chip block diagram

1.3 Feature summary

S32E2 and S32Z2 features include:

- Two core clusters, each of which:
  - Has four Arm Cortex®-R52 cores operating in two lockstep pairs, offering ASIL D performance with more than 6 kDMIPS
  - Can operate in non-lockstep, offering a total of up to 12 kDMIPS
- Arm Cortex-M33 system manager core operating in lockstep
- ISO 26262 ASIL D, including fail-operational modes, targeted throughout
- 25 GFLOPs math coprocessor and Arm Neon™ single instruction multiple data (SIMD) technology to execute advanced control algorithms
- Hardware support for virtualization throughout the system, from core to pin, to enable multi-application integration with freedom from interference
- Flash-memory options of 0, 16, 32, and 64 MB for S32E2 (all S32Z2 devices have 0 MB)
- Low-Power Double Data Rate flash-memory (LPDDR-F) interface supporting:
  - LPDDR flash memory for larger code footprints
  - LPDDR4 DRAM for temporary buffer storage
- Flexible low-latency communications engine (FlexLLCE), operating safely and securely with lockstep AES accelerator, to support CAN communications
- Zero-downtime over-the-air (OTA) updates
- Multiple options for motor control and combustion engine management:
  - GTM (optional for both S32E2 and S32Z2)
  - FlexPWM (S32E2 only)
  - eMIOS

Table 1. Feature summary

Feature	S32E2	S32Z2	
Package: MAPBGA with 0.8 mm pitch	27 mm × 27 mm with 975 balls	21 mm × 21 mm with 594 balls	17 mm × 17 mm with 400 balls
Core complex			
Cores	8 Arm Cortex-R52 processors arranged in 2 identical clusters • Each cluster contains 4 cores organized as 2 lockstep pairs: 2 usable cores and 2 shadow cores. • The 4 cores in each cluster can operate in a split-lock configuration, resulting in up to 8 usable cores.		
Core operating frequency	800 MHz (nominal) up to 1 GHz		
Core performance	• 8 non-lockstep cores: 13 kDMIPS (800 MHz), 16 kDMIPS (1 GHz) • 2 lockstep core pairs and 4 non-lockstep cores: 10 kDMIPS (800 MHz), 12 kDMIPS (1 GHz) • 4 lockstep core pairs: 6.5 kDMIPS (800 MHz), 8 kDMIPS (1 GHz)		

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Table 1. Feature summary*...continued*

Feature	S32E2	S32Z2	
Package: MAPBGA with 0.8 mm pitch	**27 mm × 27 mm with 975 balls**	**21 mm × 21 mm with 594 balls**	**17 mm × 17 mm with 400 balls**
Arm Neon SIMD technology	8 Neon—1 per core		
Floating-Point Unit (FPU)	1 single-precision FPU per core		
	1 double-precision FPU (Neon) per core		
Tightly Coupled Memory (TCM)	Per core:		
	TCM instance / **Size** / **Wait states**		
	TCMA / 64 KB / 1		
	TCMB / 16 KB / 0		
	TCMC / 16 KB / 1		
Cache memory	32 KB I-cache and 16 KB D-cache per core		
L2 cache memory	2 MB, reusable as code RAM: 1 MB per core cluster		
System manager core	1 Arm Cortex-M33 processor lockstep pair		
Memory			
Data RAM	2 MB arranged as 1 MB per core cluster		
Code RAM	14 MB arranged as 7 MB per core cluster		
System RAM	1 MB		
Flash memory	0, 16, 32, or 64 MB, with ECC Zero-downtime OTA support	—	
Electrically Erasable Programmable Read-Only Memory (EEPROM)	512 KB: arranged as eight 64 KB sectors, with 4 read-while-write partitions for EEPROM emulation	—	
Memory protection			
Core Memory Protection Unit (MPU)	Level 1: 20 regions		
	Level 2: 20 regions for hypervisor support		
Extended Resource Domain Controller (XRDC)	16 domains (region descriptors allocated for each peripheral and 16 for SRAM)		
Accelerators			
Math coprocessor (optional)	25 GFLOPs		
External memory interfaces			
LPDDR flash memory / DRAM interface	LPDDR4-1600 (×16, 800 MHz)		—

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Table 1. Feature summary*...continued*

Feature	S32E2	S32Z2	
Package: MAPBGA with 0.8 mm pitch	**27 mm × 27 mm with 975 balls**	**21 mm × 21 mm with 594 balls**	**17 mm × 17 mm with 400 balls**
Quad Serial Peripheral Interface (QuadSPI)	1 (2 on 0 MB flash memory version) supporting interfaces for: • NOR flash memory: up to 200 MHz DDR octal flash memory (×1, ×4, ×8 SDR/DDR possible) • HyperRAM: up to 166 MHz with inline ECC		
Ultra Secured Digital Host Controller (uSDHC)	1 (supports SD and eMMC)		
Enhanced Direct Memory Access (eDMA) modules			
System eDMA controller	1 lockstep pair with 32 channels and Cyclic Redundancy Check (CRC)		
Peripheral eDMA controllers	1 with 32 channels 3 with 16 channels each		
Application Extension eDMA (eDMA_AE)	1 with 16 channels	—	
Debug			
Trace	Aurora, 4 lanes, 5 Gbit/s per lane with data input through Zipwire		
Peripherals			
Analog-to-digital converters (ADCs): 3.3 V or 5.0 V	Five 12-bit Successive Approximation (SAR) ADCs (68 channels total)	—	
ADCs: 1.8 V	Two 12-bit SAR ADCs (8 channels total)		
Motor control peripherals	2 FlexPWMs (12 channels each)	—	
	4 eTimers (6 channels each)	—	
	3 Cross-Triggering Units (CTUs)	1 CTU	
	1 SINC (4 channels)		—
Timer modules	4-cluster Generic Timer Module (GTM4), up to 400 MHz, with high-resolution PWM support (optional)		
	2 Enhanced Modular Input/Output Subsystems (eMIOSs) (24 channels each)		
Logic Control Units (LCUs)	2		
Periodic Interrupt Timers (PITs)	14	13	
Software Watchdog Timers (SWTs)	13		
System Timer Modules (STMs)	13		
Semaphores2 (SEMA42)	9		

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Table 1. Feature summary*...continued*

Feature	S32E2	S32Z2	
Package: MAPBGA with 0.8 mm pitch	27 mm × 27 mm with 975 balls	21 mm × 21 mm with 594 balls	17 mm × 17 mm with 400 balls
Cyclic Redundancy Check (CRC)	8		
Communications			
CANEXCEL (CANXL)	2		
FlexCAN FD (CAN)	24		
FlexRay Communication Controller (FlexRay)	2 dual-channel		1 dual-channel or 2 single-channel
LINFlexD	12		
Ethernet (MAC)	2 Ethernet controllers supporting 10/100 Mbit/s MII/RMII and 10/100/1000 Mbit/s RGMII		
Ethernet switch	1		
Peripheral Sensor Interface (PSI5)	2 (4 channels each)		1 (4 channels)
Peripheral Sensor Interface-Support Module (PSI5_S)	2		1
Serial Peripheral Interface (SPI)	10		8
MicroSecond Channel (MSC)	1 that includes 1 LINFlexD and 1 LVDS deserial SPI (DSPI)		
Single Edge Nibble Transmission (SENT)	2 (8 channels each)		1 (8 channels)
Zipwire	2		1
Improved Inter-Integrated Circuit (I3C)	1		
Low-Power Inter-Integrated Circuit (LPI2C)	2		
Security			
Hardware Security Engine (HSE)	Yes		
Lockstep AES encryption module	Yes		
In-line Encryption Engine (IEE)	Yes		
Functional safety			
Safety	ISO 26262 Safety Element out of Context (SEooC) ASIL D		
	Flexible core recovery options		
Memory Built-In Self-Test (MBIST)	Yes		
On-chip temperature sensors and monitoring	Yes		
Packaging			
Temperature range	T_A = –40 °C to 125 °C		

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Table 1. Feature summary...*continued*

Feature	S32E2	S32Z2	
Package: MAPBGA with 0.8 mm pitch	27 mm × 27 mm with 975 balls	21 mm × 21 mm with 594 balls	17 mm × 17 mm with 400 balls
	T_J maximum = 150 °C		

2 Ordering information

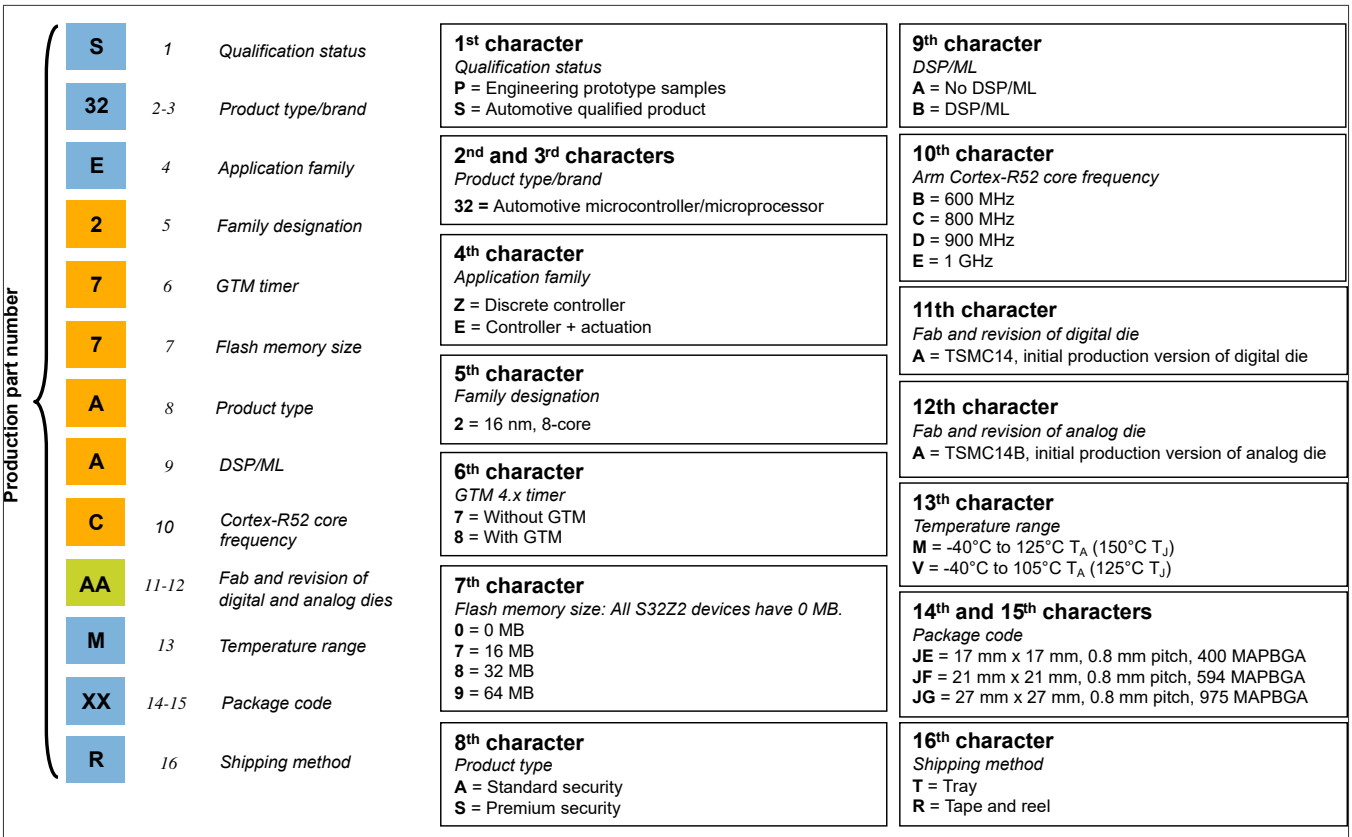

Figure 2. Ordering information

3 Electrostatic Discharge (ESD) Characteristics

The following table gives the ESD ratings and test conditions for the device.

Table 2. Electrostatic Discharge (ESD) Characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	ESD Human Body Model (HBM) [1,2,3]	—	—	2000	V	All pins	—
—	ESD Charged Device Model (CDM) [1,2,4]	—	—	250	V	All pins	—

1. Device failure is defined as: "If after exposure to ESD pulses, the device does not meet the device specification requirements."
2. All ESD testing conforms with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
3. This parameter is tested in conformity with AEC-Q100-002
4. This parameter is tested in conformity with AEC-Q100-011.

4 Maximum Ratings

4.1 Absolute Max Ratings

This table defines the absolute maximum ratings for the device in terms of reliability characteristics. Absolute maximum rating specifications are stress ratings only, and functional operation is not guaranteed under these conditions. Functional operating conditions are given in the Operating Conditions section of this document.

NOTE

All specifications associated with VIN are measured at the SoC pin.

Table 3. Absolute Max Ratings

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD	Core voltage Supply [1,2]	-0.3	—	0.96	V	—	—
VSS	Ground Supply [1]	-0.3	—	0.3	V	—	—
VDD_LV_PLL_AUR	Aurora PLL digital voltage supply [1,2]	-0.3	—	0.96	V	—	—
VDD_ANA	Supply detector high voltage supply for PMC, ADC voltage supply, TMU voltage supply [1,3]	-0.3	—	2.16	V	Reference to VSS_ADC for ADC	—
VDD_HV_FXOSC_PLL	FXOSC and PLL high voltage supply [1,3]	-0.3	—	2.16	V	Reference to VSS for FXOSC	—
VDD_FIRC	FIRC high voltage supply [1,3]	-0.3	—	2.16	V	—	—
VDD_EFUSE	EFUSE high voltage supply [1,3]	-0.3	—	2.16	V	—	—
VDD_IO_x	GPIO 3.3V supply [1,4]	-0.3	—	4	V	VDD_IO_A_J_POR, VDD_IO_B, VDD_IO_BF, VDD_IO_CD, VDD_IO_EG (21x21 and 17x17 packages), VDD_IO_EIG (27x27 package), VDD_IO_H, VDD_IO_I (21x21 and 17x17 packages)	—
VDD_IO_QSPI_0	QuadSPI_0 A I/O voltage supply [1,3]	-0.3	—	2.16	V	—	—

Table continues on the next page...

Table 3. Absolute Max Ratings...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_IO_QSPI_1	QuadSPI_1 A and B / uSDHC I/O voltage supply [1,4]	-0.3	—	4	V	—	—
VDD_HV_IO_LFAST	LFAST I/O voltage supply [1,3]	-0.3	—	2.16	V	—	—
VDD_IO_MSC	Microsecond channel IO voltage supply [1,3]	-0.3	—	2.16	V	—	—
VDD_IO_AUR	Aurora 1.8V I/O supply [1,3]	-0.3	—	2.16	V	—	—
VDD_IO_DDR0	DDR0 I/O voltage supply [1]	-0.3	—	2.16	V	—	—
VDD_IO_ETH_n	ETH n I/O 1.8/3.3V supply [1,4]	-0.3	—	4	V	—	—
VSS_ADC	ADC ground supply [1]	-0.3	—	0.3	V	Reference to VSS	—
VDD_HV_PLL_AUR	Aurora PLL high voltage supply [1,3]	-0.3	—	2.16	V	—	—
VDD_HV_PLL_DDR0	DDR PLL voltage supply [1,3]	-0.3	—	2.16	V	On the 17x17 package, VDD_HV_PLL_DDR0 must be connected to a 1.8V supply.	—
VDD_HV_LFASTPLL_n	LFAST PLL high voltage supply [1,3]	-0.3	—	2.16	V	—	—
VDD_DDR0	DDR0 high voltage supply [1,3]	-0.3	—	2.16	V	DDR PHY PLL + SoC DDR reference PLL	—
VEXTAL	FXOSC EXTAL input voltage range [1,3,5]	-0.3	—	2.16	V	—	—
VXTAL	FXOSC XTAL input voltage range [1,3,5]	-0.3	—	2.16	V	—	—
VREFH_ADCn	ADC reference high voltage (n=0, 1) [1,3]	-0.3	—	2.16	V	Reference to VREFL_ADCn	—
VREFL_ADCn	ADC reference low voltage (n=0, 1) [1]	-0.3	—	0.3	V	Reference to VSS	—
VCC_FLASH	Flash 1.8V voltage supply [1,3]	-0.3	—	2.16	V	—	—
VCCQ_FLASH	Flash 1.8V buffer voltage supply [1,3]	-0.3	—	2.16	V	—	—
VAD_INPUT	ADC input voltage range [1,6,7]	VSS_ADC -0.6	—	VDD_ANA +0.5	V	—	—

Table continues on the next page...

Table 3. Absolute Max Ratings...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIN	GPIO input voltage range [1,8,9,10]	VSS - 0.3	—	VDD_IO_* + 0.3	V	—	—
VIN_LVDS	LVDS input range [1,11]	VSS-0.3	—	VDD_HV_IO_LVDS + 0.35	V	VDD_HV_IO_LVDS <=1.92V	—
IINJ_D	Maximum DC current injection digital I/O pin [1,12]	-3	—	3	mA	—	—
IINJ_A	Maximum DC current injection analog input pin [1,7,13]	-1	—	1	mA	—	—
IINJ_LVDS	Max LVDS RX or TX pin injection current [1,14]	0	—	100	uA	—	—
IMAXSEG	Maximum RMS current per GPIO supply domain (VDD_IO_*) [1]	—	—	140	mA	—	—
TSTG	Storage temperature range [1]	-55	—	150	C	—	—
TSDR	Maximum solder temperature [1,15]	—	—	260	C	Pb free	—
MSL	Moisture Sensitivity Level [1,16]	—	—	3	—	—	—
V_OS_US_10	Voltage at 10 % of tSIGNAL [17]	-0.4	—	3.7	V	3.3V, See "SoC-pin overshoot/undershoot voltage for each GPIO pad type" figure below	—
V_OS_US_7p5	Voltage at 7.50 % of tSIGNAL [17]	-0.5	—	3.8	V	3.3V, See "SoC-pin overshoot/undershoot voltage for each GPIO pad type" figure below	—
V_OS_US_2p5	Voltage at 2.50 % of tSIGNAL [17]	-0.6	—	3.9	V	3.3V, See "SoC-pin overshoot/undershoot voltage for each GPIO pad type" figure below	—
V_OS_US_1p6	Voltage at 1.60 % of tSIGNAL [1,4,17]	-0.7	—	4	V	3.3V, See "SoC-pin overshoot/undershoot voltage for each GPIO pad type" figure below	—

Table continues on the next page...

Table 3. Absolute Max Ratings...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
V_OS_US_10	Voltage at 10 % of tSIGNAL [18]	-0.7	—	2.31	V	1.8V, See "SoC-pin overshoot/undershoot voltage for each GPIO pad type" figure below	—

1. Absolute maximum ratings are stress ratings only, and functional operation beyond the operating condition maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device. See the operating conditions table for functional specifications.
2. Allowed 0.88V – 0.96V for 60 seconds cumulative over lifetime with no operating restrictions, 2.0 hours cumulative over lifetime with device in reset, at maximum Tj = 150 °C
3. Allowed 1.92V - 2.16V for 60 seconds cumulative over lifetime with no operating restrictions, 2.6 hours cumulative over lifetime with device in reset, at maximum Tj = 150 °C
4. Allowed 3.52V - 4.0V for 60 seconds cumulative over lifetime with no operating restrictions, 2.6 hours cumulative over lifetime with device in reset, at maximum Tj = 150 °C
5. VEXTAL/ VXTAL (min) is for powered condition. VEXTAL/VXTAL (min) can be lower in unpowered condition.
6. The maximum input voltage on the ADC input pins tracks with the ADC supply maximum. For the injection current condition, the voltage on the pin equals the supply voltage plus the voltage drop across the internal ESD protection diode from ADC pin to supply. The diode voltage varies significantly across process and temperature, but a value of 0.5V can be used for nominal calculations.
7. Allowed for a cumulative duration of 50 hours operation over the lifetime of the device at maximum Tj, with VDD_ANA <= 1.92V, VSS_ADC = 0V. Allowed for unlimited duration if the device is unpowered.
8. DC case limit. Overshoot/Undershoot beyond this range is allowed, but only for the limited durations as constrained by temporal percentages of tSIGNAL.
9. Absolute minimum DC VIN level for a powered device is -0.3V. For unpowered devices, the allowed VIN min level is -0.9V. Unpowered devices must simultaneously follow IINJ_D unpowered current injection constraints.
10. Absolute maximum DC VIN levels for a powered device are 3.82V and 2.22V, for 3.3V and 1.8V domains, respectively. For powered devices when VIN ≥ VDD_IO*, VIN must simultaneously follow the constraint that VIN-VDD_IO* ≤ 0.3V for the DC case. For unpowered devices, the allowed VIN max level is +0.9V. Unpowered devices must simultaneously follow IINJ_D unpowered current injection constraints.
11. The maximum input voltage on the LVDS input pins tracks with the LVDS supply maximum. For the injection current condition, the voltage on the pin equals the supply voltage plus the voltage drop across the internal ESD protection diode from LVDS pin to supply. The diode voltage varies significantly across process and temperature, but a value of 0.35V can be used for nominal calculations.
12. IINJ_D specifications are per pin for an unpowered condition of the associated supply. The maximum simultaneous injection per supply is 30mA.
13. Non-disturb of ADC channels during current injection cannot be guaranteed. The degradation in channel performance cannot be specified due to the dynamic operation of the ADC input mux and potential for varying charge distribution. For the max +/-1mA DC injection quoted here, VAD_INPUT would be +0.5/-0.6V relative to VREFH_ADC/VREFL_ADC at max Tj. ADC Output of the channel into which injection occurs will saturate depending on the direction of injection and for the channels not subject to current injection Offset error would be -12 LSB to 6 LSB and TUE would be -12 LSB to 8 LSB.
14. Applies exclusively to ZipWire, differential DSPI, and Microsecond interfaces and does not apply to Aurora. Allowed for a cumulative of 14 hours over lifetime of the device, with the device either unpowered, during power up/down, or powered. If power cycling or fully powered, the device must be either in reset, or out of reset with LVDS disabled.
15. Solder profile per IPC/JEDEC J-STD-020D.
16. Moisture sensitivity per JEDEC test method A112.
17. For AC Signals in a 3.3V supply domain, if VDD_IO ≤ 3.3V, max VIN overshoot is limited to VDD_IO+20%. If VDD_IO > 3.3V, then max VIN overshoot is limited to 4V.
18. For AC Signals in a 1.8V supply domain, max VIN overshoot is limited to VDD_IO+20% for 10% of tSIGNAL.

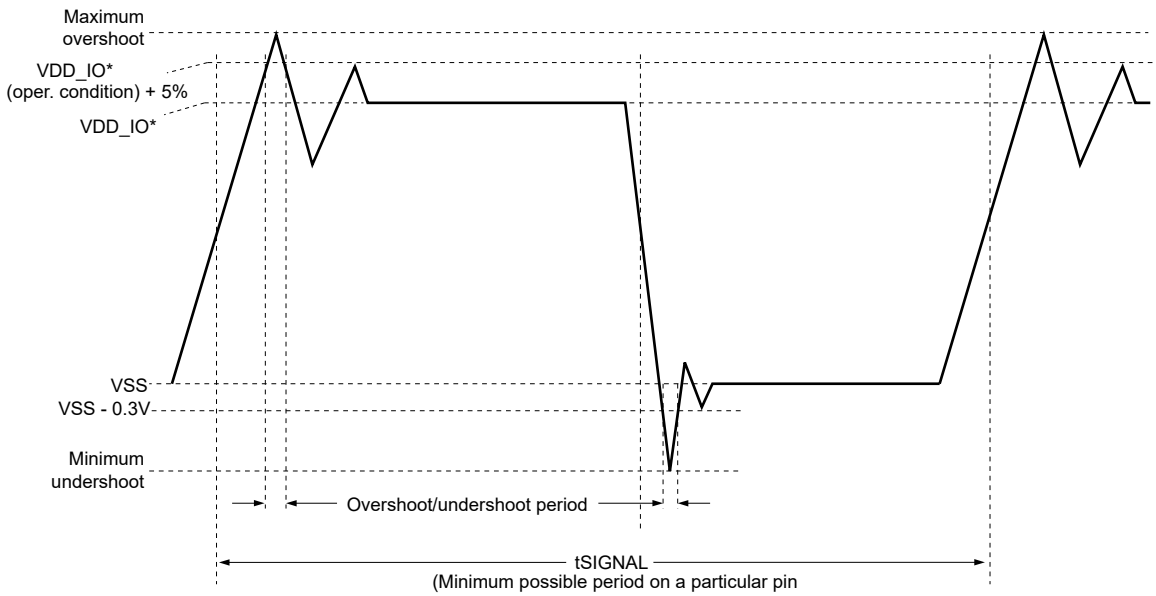

Figure 3. Soc-pin overshoot/undershoot voltage for each GPIO pad type

4.2 AE Absolute Maximum Ratings

This table defines the absolute maximum ratings for the AE device in terms of reliability characteristics. Absolute maximum rating specifications are stress ratings only, and functional operation is not guaranteed under these conditions. Functional operating conditions are given in the AE Operating Conditions section of this document.

Note: Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

Table 4. AE Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_HV_IO_D*	GPIO voltage supply [1]	-0.3	—	6.0	V	VDD_HV_IO_D1, VDD_HV_IO_D2	—
VDD_HV_REG	1.2V regulator supply voltage [2]	-0.3	—	4.5	V	—	—
VDD33	3.3V voltage supply (POR, LVD/HVD, flash) [2]	-0.3	—	4.5	V	—	—
VDDA	ADC voltage supply [2]	-0.3	—	4.5	V	Reference to VSSA	—
VSSA	ADC ground supply	-0.3	—	0.3	V	Reference to VSS	—
SAR*_VRH	ADC reference high voltage [1]	-0.3	—	6.0	V	Reference to SAR*_ VRL	—
SAR*_VRH_IO	ADC reference high voltage (shared IO supply) [1]	-0.3	—	6.0	V	Reference to SAR*_ VRL_IO	—

Table continues on the next page...

Table 4. AE Absolute Maximum Ratings...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
SAR*_VRL	ADC reference low voltage	-0.3	—	0.3	V	Reference to VSS	—
SAR*_VRL_IO	ADC reference low voltage (shared IO supply)	-0.3	—	0.3	V	Reference to VSS	—
VIN	GPIO input voltage range [1,3,4]	-0.3	—	6.0	V	—	—
VIN	GPIO input voltage range [1,5]	-0.3	—	—	V	Relative to VSS	—
VIN	GPIO input voltage range [2]	—	—	0.3	V	Relative to VDD_HV_IO_D*	—
VINA	Analog input voltage range [1,3,4]	-0.3	—	6.0	V	—	—

1. Allowed 5.5V – 6.0V for 60 seconds cumulative time with no restrictions, for 10 hours cumulative time device in reset, TJ =150 °C, remaining time at or below 5.5V.
2. Allowed 3.6V – 4.5V for 60 seconds cumulative time with no restrictions, for 10 hours cumulative time device in reset, TJ =150 °C, remaining time at or below 3.6V.
3. Relative voltage value can be exceeded as long as current injection limits are met.
4. The maximum input voltage on an I/O pin tracks with the associated I/O supply maximum. For the injection current condition on a pin, the voltage equals the supply plus the voltage drop across the internal ESD diode from I/O pin to supply. The diode voltage varies significantly across process and temperature, but a value of 0.3V can be used for nominal calculations.
5. Allowed 1.365V – 1.45V for 10 hours cumulative over lifetime at maximum Tj = 150 °C, remaining time defined in AE Operating Conditions .

5 Operating Conditions

5.1 Operating Conditions

The following table describes the functional operating conditions for the device, and for which all specifications in this datasheet are valid, except where explicitly noted. Device behavior is not guaranteed for operation outside of the conditions in this table.

NOTE

All specifications associated with VIN are measured at the SoC pin.

Table 5. Operating Conditions

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSYS_R52	Cortex-R52 core operating frequency [1,2,3]	—	—	1	GHz	TJ = 125 °C, part number 10th character = E and 13th character = V	—
fGTM	GTM clock frequency [1]	—	—	400	MHz	—	—

Table continues on the next page...

Table 5. Operating Conditions...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fHRESPWM	Digital NanoEdge clock frequency [1]	—	—	1620	MHz	—	—
Tj	Junction Temperature Range [1,4]	-40	—	150	C	—	—
Ta	Ambient Temperature Range [1]	-40	—	125	C	—	—
VSS	Ground Supply [1]	—	0	—	V	—	—
VDD	Core voltage Supply [1,5]	0.77	0.825	0.87	V	—	—
VDD_LV_PLL_AUR	Aurora PLL digital voltage supply [1]	0.77	0.825	0.87	V	—	—
VDD_IO_x	GPIO 3.3V supply [1,6]	3.08	3.3	3.52	V	VDD_IO_A_J_POR, VDD_IO_B, VDD_IO_BF, VDD_IO_CD, VDD_IO_EG (21x21 and 17x17 packages), VDD_IO_EIG (27x27 package), VDD_IO_H, VDD_IO_I (21x21 and 17x17 packages)	—
VDD_IO_ETH_n	ETH n I/O voltage supply [1]	3.08	3.3	3.52	V	3.3V	—
VDD_IO_ETH_n	ETH n I/O voltage supply [1]	1.68	1.8	1.92	V	1.8V	—
VDD_IO_QSPI_0	QuadSPI_0 A I/O voltage supply [1]	1.68	1.8	1.92	V	1.8V	—
VDD_IO_QSPI_1	QuadSPI_1 A / uSDHC I/O voltage supply [1]	1.68	1.8	1.92	V	1.8V	—
VDD_IO_QSPI_1	QuadSPI_1 A / uSDHC I/O voltage supply [1]	3.08	3.3	3.52	V	3.3	—
VDD_IO_QSPI_1	QuadSPI_1 B I/O voltage supply [1]	3.08	3.3	3.52	V	3.3	—
VDD_HV_IO_LFAST	LFAST I/O voltage supply [1]	1.68	1.8	1.92	V	—	—
VDD_IO_MSC	Microsecond channel I/O voltage supply [1]	1.68	1.8	1.92	—	—	—

Table continues on the next page...

Table 5. Operating Conditions...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_IO_AUR	Aurora 1.8V I/O supply [1]	1.68	1.8	1.92	V	Aurora LVDS Tx + ref clock	—
VDD_ANA	Analog supply [1]	1.68	1.8	1.92	V	—	—
VDD_IO_DDR0	LPDDR4 I/O voltage supply [1]	1.06	1.1	1.17	V	—	—
δVDD_IO_DDR0	LPDDR4 I/O supply ripple voltage [1]	-2.5	—	2.5	%	—	—
VDD_DDR0	DDR0 high voltage supply [1]	1.68	1.8	1.92	V	—	—
VDD_FIRC	FIRC high voltage supply [1]	1.68	1.8	1.92	V	—	—
VDD_EFUSE	EFUSE high voltage supply [1,7,8,9]	1.68	1.8	1.92	V	—	—
VDD_HV_PLL_AUR	Aurora PLL high voltage supply [1]	1.68	1.8	1.92	V	—	—
VDD_HV_PLL_DDR0	DDR PLL voltage supply [1]	1.68	1.8	1.92	V	On the 17x17 package, VDD_HV_PLL_DDR0 must be connected to a 1.8V supply.	—
δVDD_HV_PLL_DDR0	DDR PLL supply ripple voltage [1]	-2.5	—	2.5	%	—	—
VDD_HV_LFASTPLL_n	LFAST PLL high voltage supply [1]	1.68	1.8	1.92	V	—	—
VDD_HV_FXOSC_PLL	FXOSC and PLL high voltage supply [1]	1.68	1.8	1.92	V	—	—
VCC_FLASH	Flash 1.8V voltage supply [1]	1.7	1.8	1.92	V	—	—
VCCQ_FLASH	Flash 1.8V buffer voltage supply [1]	1.7	1.8	1.92	V	—	—
VREFH_ADCn	ADC reference high voltage (n=0, 1) [1]	1.68	1.8	1.92	V	—	—
VREFL_ADCn	ADC reference low voltage (n=0, 1) [1]	VSS_HV_ADC - 0.025	—	VSS_HV_ADC + 0.025	V	DC value	—
VIN_33	3.3V GPIO input voltage range [1,10,11,12]	VSS - 0.3	—	VDD_IO_* + 0.3	V	—	—
VIN_18	1.8V GPIO input voltage range [1,10,11,12]	VSS - 0.3	—	VDD_IO_* + 0.3	V	—	—

Table continues on the next page...

Table 5. Operating Conditions...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIN_LVDS	LVDS input voltage range [1,13]	VSS - 0.3	—	1.92	V	—	—
ΔVDD	0.8V supply voltage differential [1,14]	-25	—	25	mV	Applies to all 0.8V supplies on the device.	—
ΔVDD_HV_18_IO	1.8V I/O supply voltage differential group [1,14,15,16]	-25	—	25	mV	Applies to VDD_IO_QSPI_0, VDD_IO_QSPI_1 (A, 1.8V), VDD_IO_AUR	—
ΔVDD_HV_18_ANA	1.8V analog supply voltage differential group [1,14,15,17]	-25	—	25	mV	Applies to VDD_ANA, VREFH_ADC*, VDD_HV_PLL*, VDD_HV_FXOSC_PLL, VDD_FIRC, VDD_EFUSE	—
ΔVSS_HV_18	1.8V supply ground voltage differential	-25	—	25	mV	Applies to VSS, VREFL_ADCn, VSS_ADC	—
VRAMP_LV	LV supply voltage ramp-up rate [1,18]	0.001	—	10	V / ms	Applies to 0.8V supplies	—
VRAMP_HV	HV supply voltage ramp-up rate [1]	0.001	—	10	V / ms	Applies to 1.8V supplies, 3.3V I/O supplies, and the 5V ADC supply.	—
VAD_INPUT	ADC input voltage range [1,19]	VSS_ADC - 0.35	—	VDD_ANA + 0.25	V	—	—
IINJ_D	GPIO Input DC Injection Current [1,20]	-3	—	3	mA	Unpowered	—
IINJ_D	GPIO Input DC Injection Current [1,21]	0	—	5	uA	Powered	—
IINJ_A	SAR ADC Input DC Injection Current [1,22]	-20	—	20	uA	—	—
IINJ_LVDS	Max LVDS RX or TX pin injection current [1]	0	—	0	uA	—	—
IMAXSEG	Maximum RMS current per GPIO supply domain [1]	—	—	120	mA	—	—

1. The operating conditions in this table apply as required conditions for all other specifications in this document, unless explicitly noted as an exception in another section of this document.
2. Part numbers with a 10th character other than E have a lower maximum frequency at TJ = 150 °C or 125 °C (13th character = M or V). See the "Ordering information" section.
3. The stated maximum operating frequency must be observed when using the PLL with frequency modulation enabled. Center-spread modulation is supported in cases where the nominal operating frequency plus half the modulation depth is less than the stated maximum frequency.

4. Lifetime operation at Tj max not guaranteed. Standard automotive temperature profile assumed for performance and reliability guarantees.
5. Voltage regulation must be set to the 0.825V level to allow for load fluctuation within the minimum and maximum VDD values shown here and to achieve the power consumption specifications shown in this document.
6. The SAE J2716_2016 standard recommended circuit should be used when connecting SENT signals to the 3.3V VDD_IO_BF and VDD_IO_H input pads.
7. The VDD_EFUSE supply must be maintained within specification during fuse programming. Failure to do this may result in improper functionality of the device after fuse programming.
8. VDD_EFUSE must be grounded when not actively programming the fuses. This supply is not required to be powered for fuse reads. See device hardware design guidelines document for more details.
9. Refer to the Power Sequencing section for the relationship of VDD_EFUSE powering up/down relative to the core, high-voltage, and I/O supplies.
10. For AC signals, allowed max VIN ≤ VDD_IO* for lifetime operation. If AC overshoot beyond VDD_IO* occurs, then refer to the Abs Max duration constraints as a function of the amount of overshoot. For DC signals ≥ VDD_IO, VIN-VDD_IO* ≤ 0.3V is allowed for lifetime operation.
11. DC case limit. Overshoot/Undershoot beyond this range is allowed, but only for the limited durations as constrained by temporal percentages of tSIGNAL.
12. The min DC VIN level for a powered device is -0.3V. If AC undershoot below -0.3V occurs, then refer to the Abs Max duration constraints as a function of the amount of undershoot.
13. LVDS max input voltage defined by the common-mode voltage VCM_LVDS_RX and the differential swing divided by two (VDIFF_LVDS_RX/2).
14. The "voltage differential" refers to the difference between the lowest and highest voltages across all supplies within the supply group as defined under Condition column.
15. Applies only during power up while POR_B is asserted.
16. Applies to multi-voltage supplies when operating in 1.8V range.
17. VREFH_ADCn allows a differential voltage of +/-100mV.
18. On slow ramps, the RESET_B pin may be observed to be asserted multiple times during the supply ramping. In order to prevent these pulses from being propagated into the system, it is recommended that the PMIC drives RESET_B low during supply ramp or whenever POR_B is asserted.
19. The maximum input voltage on an I/O pin tracks with the associated I/O supply maximum. For the injection current condition on a pin, the voltage equals the supply plus the voltage drop across the internal ESD diode from I/O pin to supply.
20. IINJ_D specifications are per pin for an unpowered condition of the associated supply. The maximum simultaneous injection per supply is 30mA.
21. You must ensure that neither IINJ nor VIN specs are violated. Negligible DC injection currents are expected to flow during normal powered operation.
22. The SAR ADC electrical specifications are not guaranteed during any period when the operating injection current limit is violated. These specifications are at maximum Tj and VREFH_ADC=1.8V; the injected current will reduce with reduced Tj.

Footnote:
If ADC Supply (1.8 V) & ADC Reference are powered by different sources/regulators & ADC Reference comes up after ADC Supply as shown above, then the maximum number of power cycles allowed is:
No of allowed power cycles = (0.3*Life_Time)/(t1+t2)
Life_Time: Device life time in msec (12.000h)
t1: delay between ADC Reference & ADC Supply at power up in msec
t2: delay between ADC Reference & ADC Supply at power down in msec

Figure 4. ADC supply sequencing

5.2 AE Operating Conditions

The following table describes the functional operating conditions for the AE device, and for which all specifications in this datasheet are valid, except where explicitly noted. AE device behavior is not guaranteed for operation outside of the conditions in this table.

Table 6. AE Operating Conditions

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSYS_AE	AE system clock frequency	—	—	162	MHz	—	—
fSYS_MC	AE motor control clock frequency [1,2]	—	—	162	MHz	—	—
fGPIO	GPIO operating frequency	—	—	50	MHz	CLOAD = 25pF	—
Tj	Junction Temperature Range	-40	—	150	C	—	—
Ta	Ambient Temperature Range	-40	—	125	C	—	—
VDD_HV_IO_D*	GPIO voltage supply	3.135	—	3.465	V	—	—
VDD_HV_IO_D*	GPIO voltage supply	4.75	—	5.25	V	—	—
VDD_HV_REG	1.2V regulator voltage supply	1.68	—	1.92	V	—	—
VDD33	3.3V voltage supply (POR, LVD/HVD, flash)	3.135	—	3.465	V	—	—
VDDA	ADC voltage supply [3]	3.135	—	3.465	V	—	—
VSSA	ADC ground supply	0	—	0	V	—	—
SAR*_VRH	ADC reference high voltage	VDDA	—	5.5	V	—	—
SAR*_VRH_IO	ADC reference high voltage (shared IO supply)	VDDA	—	5.5	V	—	—
SAR*_VRL	ADC reference low voltage	VSSA - 10	—	VSSA + 10	mV	DC value	—
SAR*_VRL_IO	ADC reference low voltage (shared IO supply)	VSSA - 10	—	VSSA + 10	mV	DC value	—
VIN	GPIO input voltage range	0	—	VDD_HV_IO_D*	V	—	—
VINA	Analog input voltage range	SAR*_VRL	—	SAR*_VRH	V	—	—
IINJ	I/O DC injection current [4,5]	-3	—	3	mA	Applies to analog inputs and GPIO.	—

1. The motor control peripheral frequency is applicable to the eTimer, FlexPWM and the control logic of the CTU.
2. Motor Control Peripheral Frequency must be greater than or equal to ADC clock frequency.
3. VDDA must always be supplied even if the ADC is not used in the application.
4. I/O and analog input specifications are only valid if the injection current on adjacent pins is within these limits.

5. The I/O pins on the device are clamped to the I/O supply rails (VDDH for digital pins and VREFP for analog pins) for ESD protection. When the voltage of the input pin is above the supply rail, current will be injected through the clamp diode to the supply rail. For external RC network calculation, assume typical 0.3V drop across the active diode. The diode voltage drop varies with temperature.

6 Thermal Design, Characteristics, and Ratings

Thermal design and characteristics:

- Junction temperature of the device does not solely depend on package thermal resistance but is also a function of chip power dissipation, PCB attributes, environmental conditions (ambient temperature and air flow), and cumulative effects of other heat-generating ICs on the PCB.
- The appropriate thermal design must be implemented on the package so that it can safely dissipate the necessary amount of power needed for it to function properly. This design may involve adding a cooling solution on the package, creating thermal enhancements on the PCB, and improving environmental conditions.
- NXP encourages customers to use the package model to perform design and risk assessment through simulations. The sales team can provide package models in FloTHERM or Icepak formats under NDA.

Thermal ratings:

- The following table provides S32E27x package thermal ratings for the 27 mm x 27 mm MAPBGA package. These numbers are derived through simulations based on standardized tests as described in the footnotes.
- Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

Table 7. S32E27x, 27 mm x 27 mm 975 MAPBGA

Board type[1]	Symbol	Description	Value	Unit
JESD51-9, 2s2p	$R_{\theta JA}$	Junction to Ambient Thermal Resistance[2]	13.3	°C/W
JESD51-9, 2s2p	Ψ_{JT}	Junction-to-Top of Package Thermal Characterization Parameter[2]	0.1	°C/W
N/A	$R_{\theta JC}$ (top)	Junction to Case Thermal Resistance (top)[3]	2.8	°C/W

1. Thermal test board meets JEDEC specification for this package (JESD51-9).
2. Determined in accordance with JEDEC JESD51-2A natural convection environment.
3. Junction-to-Case (top) thermal resistance determined using an isothermal cold plate. Case temperature refers to the MAPBGA's mold surface temperature.

7 DC Electricals

7.1 Device Power and Operating Current Specifications

The device power consumption, operating current, and applicable conditions are given in the following table.

Table 8. Device Power and Operating Current Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
PLKG_SOC_TYP	SoC VDD typical static leakage power	—	1.7	—	W	VDD=0.825V, Tj = 150C	—
PDYN_SOC_BASE_TYP	SoC base typical dynamic power [1]	—	0.6	—	W	VDD=0.825V, 400MHz	—

Table continues on the next page...

Table 8. Device Power and Operating Current Specifications...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
PDYN_R52_TYP	Cortex-R52 core typical dynamic power [2]	—	0.8	—	W	VDD=0.825V, fsys_R52 = 800MHz	—
PDYN_R52_TYP	Cortex-R52 core typical dynamic power [2]	—	0.9	—	W	VDD=0.825V, fsys_R52=900MHz	—
PDYN_R52_TYP	Cortex-R52 core typical dynamic power [2]	—	1.0	—	W	VDD=0.825V, fsys_R52=1GHz	—
PDYN_DDR_TYP	DDR PHY & DRAM controller core supply typical dynamic power [3]	—	0.1	—	W	LPDDR4, VDD=0.825V, fsys_DDR = 1600MHz (1600MT/s), 60% access rate of 1 x 16-bit, (75% read, 25% write), 1 rank, DBI on, 1/2 data lines switching per read/write cycle, 60 Ohm transmit termination, does not include termination current.	—
PDYN_LLCE_TYP	FlexLLCE core supply typical dynamic power [4]	—	0.2	—	W	VDD=0.825V, 400MHz	—
IDD_LV_PLL_AUR	VDD_LV_PLL_AUR operating current	—	<10	—	mA	fPLL_VCO = 5GHz	—
IDD_HV_PLL_AUR	VDD_HV_PLL_AUR operating current	—	5	—	mA	fPLL_VCO = 5GHz, VDD_HV_PLL_AUR=1.8V	—
IDD_HV_PLL_DDR	VDD_HV_PLL_DDR 0 operating current (DDR reference PLL only)	—	2	—	mA	fPLL_DDR_REF = 1600MHz, 1.8V	—
IDD_HV_LFASTPLL	VDD_HV_LFASTPLL operating current	—	15.0	—	mA	per PLL, fPLL_VCO = 640MHz, VDD_HV_LFASTPLL=1.8V	—
IDD_VREF_DYN	ADC reference dynamic current consumption	—	25	50	uA	VREFH_ADC = 1.92V, Typ at 25C and Max at 150C, per ADC, 1Msps conversion rate	—

Table continues on the next page...

Table 8. Device Power and Operating Current Specifications*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IDD_VREF_LKG	ADC reference leakage/ESD current consumption	—	25	65	uA	VREFH_ADC = 1.92V, Typ at 25C and Max at 150C, per ADC, 1Msps conversion rate	—
IDD_FIRC	VDD_FIRC operating current	—	<1	—	mA	FIRC trimmed frequency (48MHz typical)	—
IDD_ANA	VDD_ANA operating current for PMC, TMU, ADC	—	10	—	mA	—	—
IDD_HV_FXOSC_PLL	Operating current for FXOSC and PLL	—	16	—	mA	fPLL_VCO = 2GHz, Core/Peripheral PLLs	—
IDD_EFUSE_PGM	VDD_EFUSE programming current	—	—	140	mA	VDD_EFUSE=1.89V, VDD=0.825V	—
IDD_DDR0	VDD_DDR0 operating current	—	5	—	mA	fDDR_PLL = 1600MHz, 1.8V	—
IDD_HV_IO_LFAST	VDD_HV_IO_LFAST operating current	—	<10	—	mA	320Mbps, VDD_HV_IO_LFAST=1.8V	—
IVDD_IO_ETH_0	Ethernet segment 0 when operating at 3.3V	—	—	120	mA	Tj=150C, RGMII 125MHz, clocks 100% activity rate, 50% data rate, 1/2 data switching per cycle. Capacitive load =15.5pF	—
IVDD_IO_ETH_0	Ethernet segment 0 when operating at 1.8V	—	—	56	mA	Tj=150C, RGMII 125MHz, clocks 100% activity rate, 50% data rate, 1/2 data switching per cycle. Capacitive load =15.5pF	—
IVDD_IO_ETH_1	Ethernet segment 1 when operating at 3.3V	—	—	120	mA	Tj=150C, RGMII 125MHz, clocks 100% activity rate, 50% data rate, 1/2 data switching per cycle. Capacitive load =15.5pF	—
IVDD_IO_ETH_1	Ethernet segment 1 when operating at 1.8V	—	—	56	mA	Tj=150C, RGMII 125MHz, clocks 100% activity rate, 50% data rate, 1/2 data switching per cycle. Capacitive load =15.5pF	—

Table continues on the next page...

Table 8. Device Power and Operating Current Specifications*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IDD_HV_AUR_LKG	VDD_HV_AUR leakage current	—	700	—	uA	Transmit pad disabled	—
IVDD_IO_QSPI_0	QuadSPI_0 A I/O voltage supply operating current	—	—	35	mA	1.8V, Tj = 150C, 200MHz Octal mode, DDR - clocks 100% activity rate, 50% data rate, 1/2 data switching per cycle, does not include power for other I/O pins on the VDD_IO_QSPI_0 supply.	—
IVDD_IO_QSPI_1	QuadSPI_1 A / uSDHC I/O voltage supply operating current	—	—	80	mA	1.8V, Tj = 150C, 166MHz Octal mode, DDR - clocks 100% activity rate, 50% data rate, 1/2 data switching per cycle, does not include power for other I/O pins on the VDD_IO_QSPI_1 supply.	—
IVDD_IO_QSPI_1	QuadSPI_1 A / uSDHC I/O voltage supply operating current	—	—	130	mA	3.3V, Tj = 150C, 100MHz Octal mode, DDR - clocks 100% activity rate, 50% data rate, 1/2 data switching per cycle, does not include power for other I/O pins on the VDD_IO_QSPI_1 supply.	—
IVDD_IO_QSPI_1	QuadSPI_1 B I/O voltage supply operating current	—	—	75	mA	3.3V, Tj = 150C, 50MHz Quad mode, SDR - clocks 100% activity rate, 50% data rate, 1/2 data switching per cycle, does not include power for other I/O pins on the VDD_IO_QSPI_1 supply.	—

1. Base dynamic power includes SMU, HSE, DMA, peripherals, and clocks. It excludes RTU, DDR, and FlexLLCE clocks and domains.
2. Cortex-R52 core typical dynamic power based on Dhrystone running with 80% activity factor on all eight Cortex-R52 cores and executing DMA on the platform with 100% activity factor. RTU0 and RTU1 each account for half the spec value.
3. Power includes MC_CGM_6 clocking current at 400MHz plus DDR access current and excludes IO_DDR.
4. FlexLLCE typical dynamic power includes FlexLLCE subsystem clocks and peripherals plus all cores running Dhrystone.

7.2 Static power specifications for I/O Domains

Table 9. Static power specifications for I/O Domains

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_IO_DDR0	DDR I/O Supply	—	0.8	2.4	mA	1.1V	—
VDD_IO_AUR	Aurora I/O Supply	—	0.3	0.6	mA	1.8V	—
VDD_IO_LFAST	LFAST I/O Supply	—	0.1	0.4	mA	1.8V	—
VDD_IO_MSC	Microsecond Channel I/O Supply	—	0.2	0.4	mA	1.8V	—
VDD_IO_QSPI_0	QuadSPI_0 I/O Supply	—	1.0	1.8	mA	1.8V	—
VDD_IO_QSPI_1	QuadSPI_1A I/O Supply	—	37.3	72.1	mA	1.8V	—
VDD_IO_QSPI_1	QuadSPI_1A I/O Supply	—	47.3	82.1	mA	3.3V	—
VDD_3V3_IO	GPIO Supply	—	1.3	1.8	mA	3.3V	—
VDD_IO_A_J_POR	GPIOA, GPIOJ, POR I/O Supply	—	2.0	2.7	mA	3.3V	—
VDD_IO_BF	GPIOB, GPIOF Supply	—	1.3	2.0	mA	3.3V	—
VDD_IO_ETH_0	ETH 0 I/O Supply	—	35.9	76.6	mA	1.8V	—
VDD_IO_ETH_1	ETH 1 I/O Supply	—	35.9	76.6	mA	1.8V	—
VDD_IO_ETH_0	ETH 0 I/O Supply	—	43.9	84.6	mA	3.3V	—
VDD_IO_ETH_1	ETH 1 I/O Supply	—	43.9	84.6	mA	3.3V	—
VDD_IO_H	GPIOH, QuadSPI_1B I/O Supply	—	0.6	0.9	mA	3.3V	—
VDD_IO_EG	GPIOE, GPIOG Supply	—	1.2	1.7	mA	3.3V	—
VDD_IO_I	GPIOI Supply	—	0.7	2.7	mA	3.3V	—
VDD_HV_IO_D0	AE I/O Supply	—	0.1	0.5	mA	3.3V	—
VDD_HV_IO_D1	AE I/O Supply	—	0.1	0.5	mA	3.3V	—
VDD_HV_IO_D0	AE I/O Supply	—	0.2	2.0	mA	5.0V	—
VDD_HV_IO_D1	AE I/O Supply	—	0.2	2.0	mA	5.0V	—
VDD_IO_EIG	GPIOE, GPIOI, GPIOG Supply	—	1.9	2.5	mA	3.3V	—

7.3 Total power specifications

The part is designed with a power distribution network that has two specifications: dynamic power and total supply rail power (dynamic power plus leakage power). At higher temperatures, the leakage is higher and the user must manage the dynamic

power to compensate. The user must ensure the total supply rail power is below the total power distribution network capacity. At lower temperatures, the leakage is reduced and the part can utilize the full dynamic power capacity. Exceeding either power specifications will result in IR drop issues and unpredictable operation of the device.

Table 10. Total power specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
PVDD_DOMAIN1	0.825 V supply rail power [1,2]	—	—	5.2	W	Core VDD, Tj=150C	—
PVDD_DOMAIN1	0.825 V supply rail power [1,2]	—	—	4.8	W	Core VDD, Tj=125C	—
PDYN_DOMAIN1	0.825 V total dynamic power [3]	—	—	2.0	W	Core VDD, Tj=150C, at maximum leakage	—
PDYN_DOMAIN1	0.825 V total dynamic power [3]	—	—	2.8	W	Core VDD, Tj=125C	—

1. The supply rail leakage and dynamic power cannot exceed the total supply rail power specification.
2. Total supply rail power is dynamic power plus leakage power.
3. The device cannot exceed the total dynamic power specification.

7.4 AE Device Power and Operating Current Specifications

The AE device power consumption, operating current, and applicable conditions are given in the following table.

Table 11. AE Device Power and Operating Current Specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
PVDD12	VDD core supply power	—	—	200	mW	Tj = 150C, VDD12 = 1.265V, fSYS_AE = 160MHz	—
PVDD_HV_REG	1.2V regulator supply power	—	—	300	mW	Tj = 150C, VDD_HV_REG = 1.8V, fSYS_AE = 160MHz	—
PVDD33	VDD33 supply power (POR, LVD/HVD, flash)	—	—	35	mW	Tj = 150C, VDD33 = 3.465V	—
IVDDA	VDDA voltage supply current	—	—	10	mA	Tj = 150C, VDDA = 3.465V, 5 ADCs enabled and converting, fAD_CK = 80MHz	—
ISAR_VRH	SAR*_VRH / SAR*_VRH_IO reference supply current	—	—	2	mA	per reference supply, Tj = 150C, SAR*_VRH / SAR*_VRH_IO = 5.5V, 2 ADCs active on the reference supply, fAD_CLK = 80MHz	—

8 Power Sequencing

8.1 Power-up

The following sequence has been validated by NXP and is to be followed when powering up the device. Contact NXP Semiconductor for more information on supply sequences that deviate from this sequence. Each supply within a step must be within its specified operating voltage range before the next step in the sequence is started.

1. Set POR_B input to low value.
2. Ramp up all GPIO supplies and ADC references powered to 5V
3. Ramp up all 3.3V supplies including GPIO supplies powered to 3.3V
4. Ramp up all 1.8V supplies including GPIO supplies powered to 1.8V
5. Ramp up all 1.1V supplies.
6. Ramp up all 0.8V supplies
7. Set POR_B input to high value

NOTE

T he 5V supplies can be powered after the 3.3V supplies with no issues on the device.

NOTE

While powering up the device, the VDD_EFUSE supply pin must be kept powered down. While the device is already powered up, the VDD_EFUSE supply pin can be powered up/down independent of the other supplies on the device.

8.2 Power-down

When powering down the SoC, it is recommended to use the reverse order from the power-up sequence. If this cannot be achieved, ensure that all supplies are below the Vpwrdwn level before powering up again.

Table 12. Power-down

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Vpwrdwn	Maximum voltage on a supply pin in powerdown mode	—	—	100	mV	—	—

9 Electromagnetic compatibility (EMC)

EMC measurements to IC-level IEC standards are available from NXP Semiconductor on request.

10 I/O Pad Characteristics

10.1 GPIO Pads

Table 13. GPIO Pads

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIH	Input high level DC voltage threshold	0.7 * VDD_IO_*	—	—	V	1.8V / 3.3V	—
VIL	Input low level DC voltage threshold	—	—	0.3 * VDD_IO_*	V	1.8V / 3.3V	—
VOL	GPIO output low voltage [1]	—	—	20% * VDD_IO_*	V	—	—
VOH	GPIO output high voltage [1]	80% * VDD_IO_*	—	—	V	—	—
VHYS_33	3.3V GPIO input hysteresis voltage	100	—	—	mV	Always enabled.	—
ILKG_18	1.8V GPIO pad input leakage current	-17	—	17	uA	1.8V, Tj = 150C	—
ILKG_33	3.3V GPI / GPIO pad input leakage current	-30	—	30	uA	3.3V, Tj = 150C	—
ILKG_3318	1.8V/3.3V GPIO pad input leakage current (3.3V)	-50	—	50	uA	3.3V, Tj = 150C	—
ILKG_3318	1.8V/3.3V GPIO pad input leakage current (1.8V)	-17	—	17	uA	1.8V, Tj = 150C	—
CIN_18	Input capacitance (1.8V GPIO)	—	6	8	pF	—	—
CIN_33	Input capacitance (3.3V GPI / GPIO)	—	7	11	pF	—	—
CIN_3318	Input capacitance (1.8V/3.3V GPIO)	—	7	11	pF	—	—
ISLEW	Input signal slew rate [2]	1	—	4	V/ns	—	—
ITR_TF	Input signal rise/fall time [2,3]	0.5	—	2	ns	—	—
TPW_MIN	Input minimum pulse width	2	—	—	ns	—	—

Table continues on the next page...

Table 13. GPIO Pads...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
FMAX_IN_18	1.8V GPIO maximum input frequency [4]	—	—	50	MHz	CMOS Receiver	—
FMAX_IN_18	1.8V GPIO maximum input frequency [4]	—	—	208	MHz	VREF Receiver	—
FMAX_IN_3318	1.8V/3.3V GPIO maximum input frequency [4]	—	—	208	MHz	1.8V	—
FMAX_IN_3318	1.8V/3.3V GPIO maximum input frequency [4]	—	—	166.7	MHz	3.3V	—
FMAX_IN_33	3.3V GPIO maximum input frequency [4]	—	—	50	MHz	—	—
IPU_18	1.8V GPIO pull up/down resistance	9	18	23	kΩ	pull up @ 0.3 * VDD_HV_IO, pull down @ 0.7 * VDD_HV_IO	—
IPU_33	3.3V GPIO pull up/down resistance	9	18	23	kΩ	pull up @ 0.3 * VDD_HV_IO, pull down @ 0.7 * VDD_HV_IO	—
IPU_3318	1.8V/3.3V GPIO pull up/down resistance	9	18	23	kΩ	pull up @ 0.3 * VDD_HV_IO, pull down @ 0.7 * VDD_HV_IO	—
RDSON_18	1.8V GPIO output impedance (NMOS & PMOS) [5]	27.0	36.3	48.0	Ω	SRE[2:0] = xxx, 50% * VDD_IO_*	—
RDSON_3318	1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 1.8V [5]	18.0	30.0	43.0	Ω	SRE[2:0] = 000, 50% * VDD_IO_*	—
RDSON_3318	1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 1.8V [5]	19.0	30.0	44.0	Ω	SRE[2:0] = 100, 50% * VDD_IO_*	—
RDSON_3318	1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 1.8V [5]	21.0	33.0	49.0	Ω	SRE[2:0] = 101, 50% * VDD_IO_*	—
RDSON_3318	1.8V/3.3V GPIO output impedance	23.0	37.5	58.0	Ω	SRE[2:0] = 110, 50% * VDD_IO_*	—

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Table 13. GPIO Pads...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	(NMOS & PMOS) at 1.8V [5]						
RDSON_3318	1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 1.8V [5]	24.0	37.5	57.0	Ω	SRE[2:0] = 111, 50% * VDD_IO_*	—
RDSON_3318	1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 3.3V [5]	18.0	30.0	43.0	Ω	SRE[2:0] = 000, 50% * VDD_IO_*	—
RDSON_3318	1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 3.3V [5]	19.0	30.0	44.0	Ω	SRE[2:0] = 100, 50% * VDD_IO_*	—
RDSON_3318	1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 3.3V [5]	21.0	33.4	50.0	Ω	SRE[2:0] = 101, 50% * VDD_IO_*	—
RDSON_3318	1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 3.3V [5]	23.0	39.5	61.0	Ω	SRE[2:0] = 110, 50% * VDD_IO_*	—
RDSON_3318	1.8V/3.3V GPIO output impedance (NMOS & PMOS) at 3.3V [5]	26.0	39.5	61.0	Ω	SRE[2:0] = 111, 50% * VDD_IO_*	—
RDSON_33	3.3V GPIO output impedance (NMOS & PMOS) [5]	16.5	26.5	42.0	Ω	SRE[2:0] = 100, 50% * VDD_IO_*	—
RDSON_33	3.3V GPIO output impedance (NMOS & PMOS) [5]	19.2	30.5	49.5	Ω	SRE[2:0] = 101, 50% * VDD_IO_*	—
RDSON_33	3.3V GPIO output impedance (NMOS & PMOS) [5]	24.5	38.0	61.5	Ω	SRE[2:0] = 110, 50% * VDD_IO_*	—
RDSON_33	3.3V GPIO output impedance (NMOS & PMOS) [5]	32.0	48.0	75.5	Ω	SRE[2:0] = 111, 50% * VDD_IO_*	—
IOH_18	1.8V GPIO output high current [5]	-15.0	—	-6.0	mA	SRE[2:0] = xxx, 80% * VDD_IO_*	—
IOL_18	1.8V GPIO output low current [5]	6.0	—	15.0	mA	SRE[2:0] = xxx, 20% * VDD_IO_*	—

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Table 13. GPIO Pads...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IOH_3318	1.8V/3.3V GPIO output high current at 1.8V [5]	-22	—	-8	mA	SRE[2:0] = 000, 80% * VDD_IO_*	—
IOH_3318	1.8V/3.3V GPIO output high current at 1.8V [5]	-21	—	-8	mA	SRE[2:0] = 100, 80% * VDD_IO_*	—
IOH_3318	1.8V/3.3V GPIO output high current at 1.8V [5]	-19	—	-6	mA	SRE[2:0] = 101, 80% * VDD_IO_*	—
IOH_3318	1.8V/3.3V GPIO output high current at 1.8V [5]	-17	—	-6	mA	SRE[2:0] = 110, 80% * VDD_IO_*	—
IOH_3318	1.8V/3.3V GPIO output high current at 1.8V [5]	-17	—	-6	mA	SRE[2:0] = 111, 80% * VDD_IO_*	—
IOL_3318	1.8V/3.3V GPIO output low current at 1.8V [5]	8	—	22	mA	SRE[2:0] = 000, 20% * VDD_IO_*	—
IOL_3318	1.8V/3.3V GPIO output low current at 1.8V [5]	8	—	21	mA	SRE[2:0] = 100, 20% * VDD_IO_*	—
IOL_3318	1.8V/3.3V GPIO output low current at 1.8V [5]	6	—	20	mA	SRE[2:0] = 101, 20% * VDD_IO_*	—
IOL_3318	1.8V/3.3V GPIO output low current at 1.8V [5]	6	—	18	mA	SRE[2:0] = 110, 20% * VDD_IO_*	—
IOL_3318	1.8V/3.3V GPIO output low current at 1.8V [5]	6	—	17	mA	SRE[2:0] = 111, 20% * VDD_IO_*	—
IOH_3318	1.8V/3.3V GPIO output high current at 3.3V [5]	-40	—	-14	mA	SRE[2:0] = 000, 80% * VDD_IO_*	—
IOH_3318	1.8V/3.3V GPIO output high current at 3.3V [5]	-40	—	-14	mA	SRE[2:0] = 100, 80% * VDD_IO_*	—
IOH_3318	1.8V/3.3V GPIO output high current at 3.3V [5]	-35	—	-10	mA	SRE[2:0] = 101, 80% * VDD_IO_*	—
IOH_3318	1.8V/3.3V GPIO output high current at 3.3V [5]	-32	—	-10	mA	SRE[2:0] = 110, 80% * VDD_IO_*	—

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Table 13. GPIO Pads...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IOH_3318	1.8V/3.3V GPIO output high current at 3.3V [5]	-32	—	-10	mA	SRE[2:0] = 111, 80% * VDD_IO_*	—
IOL_3318	1.8V/3.3V GPIO output low current at 3.3V [5]	15	—	40	mA	SRE[2:0] = 000, 20% * VDD_IO_*	—
IOL_3318	1.8V/3.3V GPIO output low current at 3.3V [5]	15	—	40	mA	SRE[2:0] = 100, 20% * VDD_IO_*	—
IOL_3318	1.8V/3.3V GPIO output low current at 3.3V [5]	13	—	36	mA	SRE[2:0] = 101, 20% * VDD_IO_*	—
IOL_3318	1.8V/3.3V GPIO output low current at 3.3V [5]	12	—	33	mA	SRE[2:0] = 110, 20% * VDD_IO_*	—
IOL_3318	1.8V/3.3V GPIO output low current at 3.3V [5]	11	—	32	mA	SRE[2:0] = 111, 20% * VDD_IO_*	—
IOH_33	3.3V GPIO output high current [5]	-40.1	—	-14.0	mA	SRE[2:0] = 100, 80% * VDD_IO_*	—
IOH_33	3.3V GPIO output high current [5]	-36.2	—	-12.1	mA	SRE[2:0] = 101, 80% * VDD_IO_*	—
IOH_33	3.3V GPIO output high current [5]	-32.0	—	-10.3	mA	SRE[2:0] = 110, 80% * VDD_IO_*	—
IOH_33	3.3V GPIO output high current [5]	-29.0	—	-9.0	mA	SRE[2:0] = 111, 80% * VDD_IO_*	—
IOL_33	3.3V GPIO output low current [5]	14.6	—	39.4	mA	SRE[2:0] = 000, 20% * VDD_IO_*	—
IOL_33	3.3V GPIO output low current [5]	14.6	—	39.4	mA	SRE[2:0] = 100, 20% * VDD_IO_*	—
IOL_33	3.3V GPIO output low current [5]	13.0	—	35.5	mA	SRE[2:0] = 101, 20% * VDD_IO_*	—
IOL_33	3.3V GPIO output low current [5]	11.2	—	32.0	mA	SRE[2:0] = 110, 20% * VDD_IO_*	—
IOL_33	3.3V GPIO output low current [5]	10.0	—	29.0	mA	SRE[2:0] = 111, 20% * VDD_IO_*	—
FMAX_18	1.8V GPIO maximum output frequency [5,6]	—	—	208	MHz	SRE[2:0] = 000	—

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Table 13. GPIO Pads...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
FMAX_18	1.8V GPIO maximum output frequency [5,6]	—	—	150	MHz	SRE[2:0] = 100	—
FMAX_18	1.8V GPIO maximum output frequency [5,6]	—	—	133	MHz	SRE[2:0] = 101	—
FMAX_18	1.8V GPIO maximum output frequency [5,6]	—	—	100	MHz	SRE[2:0] = 110	—
FMAX_18	1.8V GPIO maximum output frequency [5,6]	—	—	50	MHz	SRE[2:0] = 111	—
FMAX_33	3.3V GPIO maximum output frequency [5,6]	—	—	50	MHz	SRE[2:0] = 100	—
FMAX_33	3.3V GPIO maximum output frequency [5,6]	—	—	50	MHz	SRE[2:0] = 101, reduced slew relative to the SRE[2:0] = 100 setting for the same output load.	—
FMAX_33	3.3V GPIO maximum output frequency [5,6]	—	—	50	MHz	SRE[2:0] = 110	—
FMAX_33	3.3V GPIO maximum output frequency [5,6]	—	—	1	MHz	SRE[2:0] = 111	—
FMAX_3318	1.8V/3.3V GPIO maximum output frequency [5,6]	—	—	208	MHz	SRE[2:0] = 000, 1.8V	—
FMAX_3318	1.8V/3.3V GPIO maximum output frequency [5,6]	—	—	166.7	MHz	SRE[2:0] = 100, 1.8V	—
FMAX_3318	1.8V/3.3V GPIO maximum output frequency [5,6]	—	—	150	MHz	SRE[2:0] = 101, 1.8V	—
FMAX_3318	1.8V/3.3V GPIO maximum output frequency [5,6]	—	—	133.3	MHz	SRE[2:0] = 110, 1.8V	—
FMAX_3318	1.8V/3.3V GPIO maximum output frequency [5,6]	—	—	100	MHz	SRE[2:0] = 111, 1.8V	—

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Table 13. GPIO Pads...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
FMAX_3318	1.8V/3.3V GPIO maximum output frequency [5,6]	—	—	166.7	MHz	SRE[2:0] = 000, 3.3V	—
FMAX_3318	1.8V/3.3V GPIO maximum output frequency [5,6]	—	—	150	MHz	SRE[2:0] = 100, 3.3V	—
FMAX_3318	1.8V/3.3V GPIO maximum output frequency [5,6]	—	—	133.3	MHz	SRE[2:0] = 101, 3.3V	—
FMAX_3318	1.8V/3.3V GPIO maximum output frequency [5,6]	—	—	100	MHz	SRE[2:0] = 110, 3.3V	—
FMAX_3318	1.8V/3.3V GPIO maximum output frequency [5,6]	—	—	83.3	MHz	SRE[2:0] = 111, 3.3V	—
TR_TF_3318	1.8V/3.3V GPIO rise/fall time at 1.8V [5,6,7]	1.0	—	5.5	V/ns	SRE[2:0] = 000	—
TR_TF_3318	1.8V/3.3V GPIO rise/fall time at 1.8V [5,6,7]	1.0	—	5.75	V/ns	SRE[2:0] = 100	—
TR_TF_3318	1.8V/3.3V GPIO rise/fall time at 1.8V [5,6,7]	0.75	—	4.75	V/ns	SRE[2:0] = 101	—
TR_TF_3318	1.8V/3.3V GPIO rise/fall time at 1.8V [5,6,7]	0.5	—	4.5	V/ns	SRE[2:0] = 110	—
TR_TF_3318	1.8V/3.3V GPIO rise/fall time at 1.8V [5,6,7]	0.5	—	4.0	V/ns	SRE[2:0] = 111	—
TR_TF_3318	1.8V/3.3V GPIO rise/fall time at 3.3V [5,6,7]	2.0	—	10.5	V/ns	SRE[2:0] = 000	—
TR_TF_3318	1.8V/3.3V GPIO rise/fall time at 3.3V [5,6,7]	2.0	—	9.25	V/ns	SRE[2:0] = 100	—
TR_TF_3318	1.8V/3.3V GPIO rise/fall time at 3.3V [5,6,7]	1.5	—	9.5	V/ns	SRE[2:0] = 101	—
TR_TF_3318	1.8V/3.3V GPIO rise/fall time at 3.3V [5,6,7]	0.75	—	7.5	V/ns	SRE[2:0] = 110	—
TR_TF_3318	1.8V/3.3V GPIO rise/fall time at 3.3V [5,6,7]	0.75	—	7.25	V/ns	SRE[2:0] = 111	—
TR_TF_18	1.8V GPIO rise/fall time [5,6,7]	0.75	—	3.75	V/ns	SRE[2:0] = 000	—
TR_TF_18	1.8V GPIO rise/fall time [5,6,7]	0.75	—	3.75	V/ns	SRE[2:0] = 100	—

Table continues on the next page...

Table 13. GPIO Pads...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TR_TF_18	1.8V GPIO rise/fall time [5,6,7]	0.75	—	3.25	V/ns	SRE[2:0] = 101	—
TR_TF_18	1.8V GPIO rise/fall time [5,6,7]	0.75	—	3.25	V/ns	SRE[2:0] = 110	—
TR_TF_18	1.8V GPIO rise/fall time [5,6,7]	0.25	—	3.25	V/ns	SRE[2:0] = 111	—
TR_TF_33	3.3V GPIO rise/fall time [5,6,7]	1.90	—	9.0	V/ns	SRE[2:0] = 100	—
TR_TF_33	3.3V GPIO rise/fall time [5,6,7]	1.00	—	8.50	V/ns	SRE[2:0] = 101	—
TR_TF_33	3.3V GPIO rise/fall time [5,6,7]	0.50	—	7.30	V/ns	SRE[2:0] = 110	—
TR_TF_33	3.3V GPIO rise/fall time [5,6,7]	0.40	—	6.0	V/ns	SRE[2:0] = 111	—
VISE_33	3.3V GPIO pad indeterminate state end threshold	—	2.35	—	V	See 1.8V and 3.3V GPIO pad detailed behavior diagram below	—
VISE_3318	1.8V/3.3V GPIO pad indeterminate state end threshold	—	1.53	—	V	See 1.8V/3.3V GPIO pad detailed behavior diagram below	—
VISE_18	1.8V GPIO pad indeterminate state end threshold	—	0.6	—	V	See 1.8V and 3.3V GPIO pad detailed behavior diagram below	—

1. For current at this voltage see IOL/IOH specs respectively.
2. Fastest slew rate and lowest rise/fall time constraint required to meet high-speed interface timing such as QSPI, RGMII, and uSDHC. Slower input transitions can be used for input signals with slow switching rates (<40 MHz).
3. The ISLEW has precedence over ITR_TF if the ITR_TF violates the implied range for a given ISLEW.
4. Input slew rate and rise/fall time limits must be adhered to in conjunction with the max input frequency limits given for proper operation.
5. GPIO output transition time information can be obtained from the device IBIS model. IBIS models are recommended for system level simulations, as discrete values for I/O transition times are not representative of the I/O pad behavior when connected to an actual transmission line load.
6. I/O timing specifications are valid for the un-terminated 50ohm transmission line reference load given in the figure below. A lumped 8pF load is assumed at the end of a 5 inch microstrip trace on standard FR4 with approximately 3.3pF/inch. For signals with frequency greater than 63MHz, a maximum 2 inch PCB trace is assumed. For best signal integrity, the series resistance in the transmission line should be matched closely to the selected RDSON of the I/O pad output.
7. Rise/fall time specifications are derived from simulation model for the defined operating points (between 20% and 80% of VDD_HV_IO level). Actual application rise/fall time should be extracted from IBIS model simulations with the microcontroller models and application PCB. Actual application rise fall times extracted from simulation must meet the TR_TF specification.

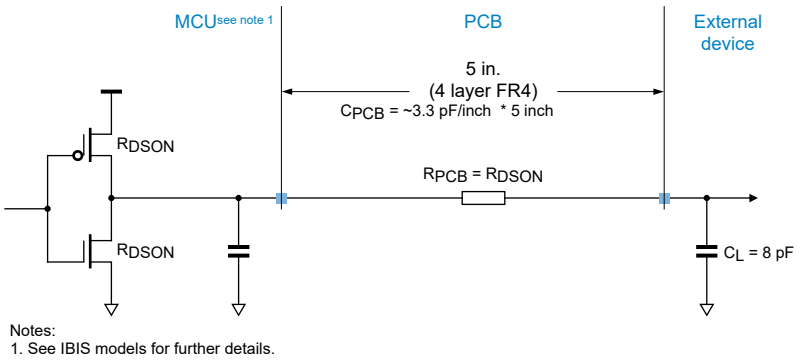


Figure 5. Reference Load Diagram

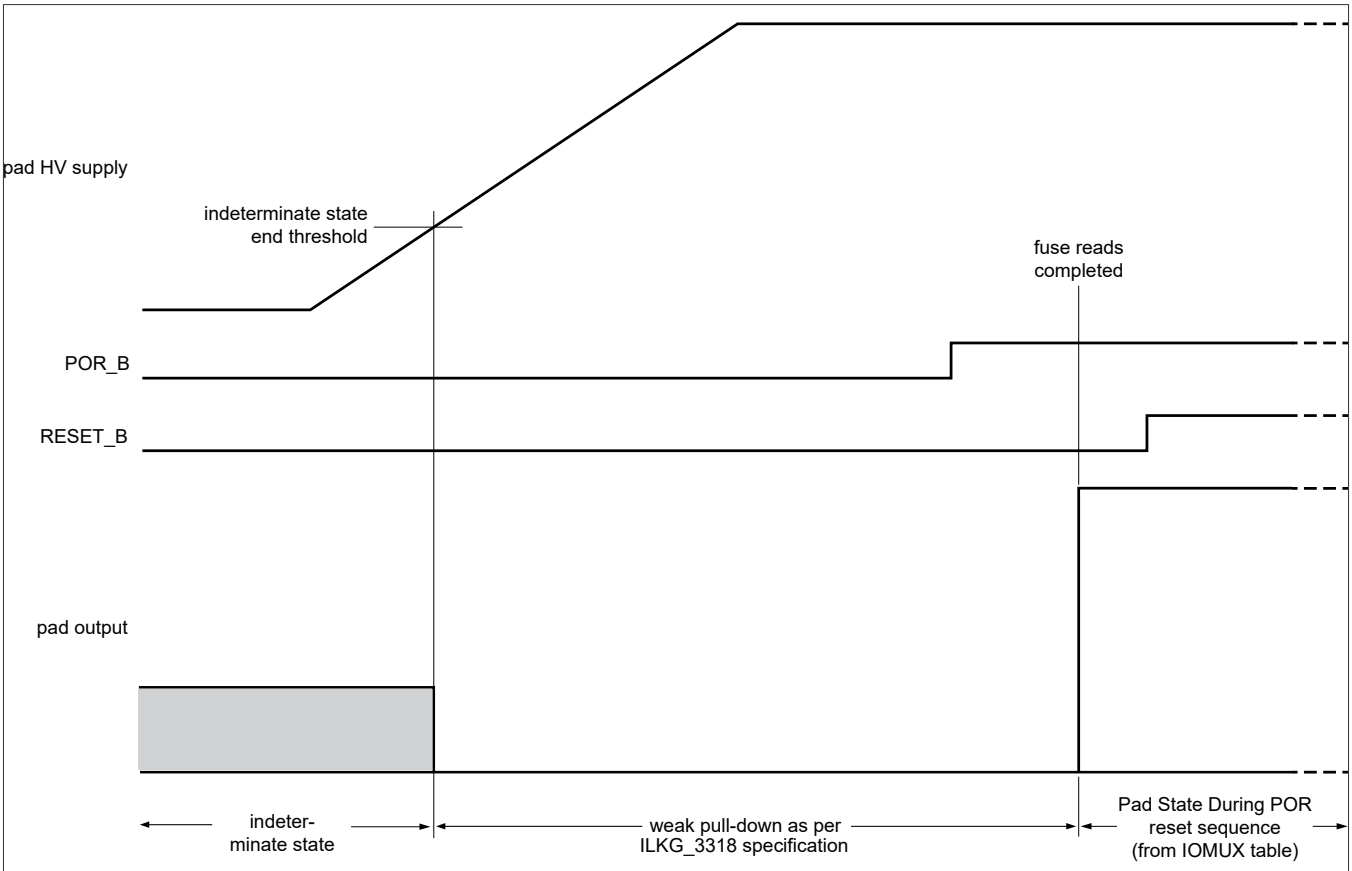


Figure 6. 1.8V/3.3V GPIO pad detailed behavior during power up

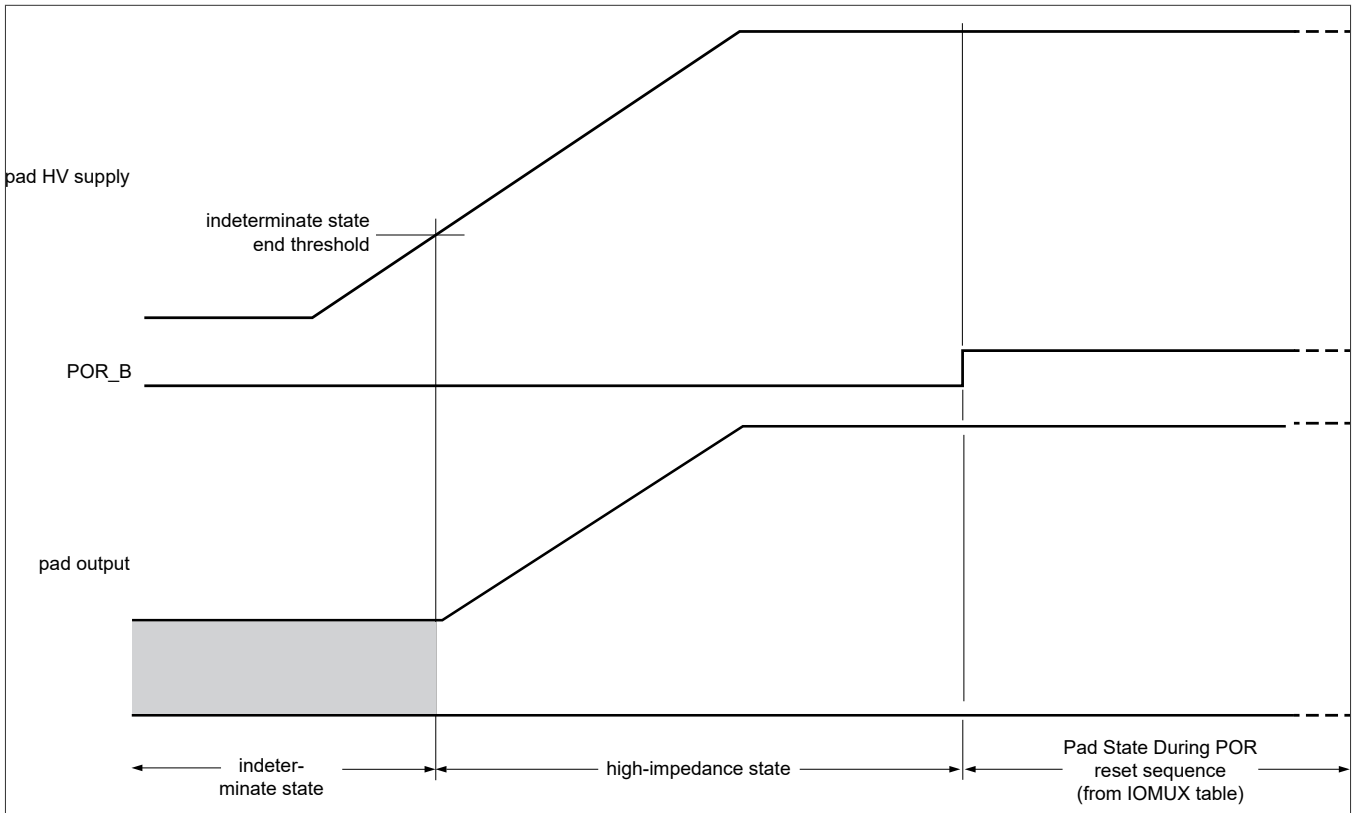


Figure 7. 1.8V and 3.3V GPIO pad detailed behavior during power up

The high-impedance state level is shown based on the external pull-up being on the corresponding pad supply.

10.2 LVDS Pads

The table below gives the specifications for the LVDS transmitter and receiver pads. The LVDS pads are used for the Aurora reference clock receiver, the CLKOUT LVDS transmitter, MSC, SPI and ZipWire.

Table 14. LVDS Pads

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fLVDS	Data Rate	—	—	420	Mbps	100ohm external termination at receiver	—
VFAULT_RX_FALL	LVDS Receiver Input Fall voltage threshold for channel open fault detection assertion	50	—	250	mV	Open transmitter	—
VFAULT_RX_RISE	LVDS Receiver Input Rise voltage threshold for channel open fault detection de-assertion	50	—	250	mV	Open transmitter	—

Table continues on the next page...

Table 14. LVDS Pads...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDIFF_LVDS_TX	Transmitter Differential output voltage	180	300	450	mV	max fLVDS, 100ohm external termination / 50ohm Tx line delay, matched network	—
VCM_LVDS_TX	Transmitter Output Common mode voltage	0.775	—	1.025	V	Applies to Aurora, CLKOUT LVDS TX and Zipwire	—
VCM_LVDS_TX	Transmitter Output Common mode voltage	1.05	—	1.37	V	Applies to SPI/MSC	—
CLOAD_LVDS	Maximum transmission line load(Not lumped but distributed over the Tline)	—	—	10	pF	—	—
RTERM_LVDS	Internal termination resistance	80	100	130	Ohm	transmitter and receiver	—
VSLEW_LVDS	Differential output slew rate	0.2	—	—	V/nS	max fLVDS	—
TSTARTUP_ LVDS_TX	Transmitter startup time (transmitter ready after enabling)	—	—	1.5	us	Includes reference startup time	—
TEYE_LVDS	Valid data region	0.8	—	—	UI	transmitter, max fLVDS, includes PLL jitter	—
VOH_LVDS	Transmitter output high indicator	LVDS I/O Supply / 2 + 0.1	—	—	V	100ohm termination	—
VOL_LVDS	Transmitter output low indicator	—	—	LVDS I/O Supply / 2 - 0.1	V	100ohm termination	—
VCM_LVDS_RX	Receiver Input signal common mode range [1]	0.225	—	VDD_HV _IO_LFA ST - 0.225	V	—	—
VDIFF_LVDS_RX	Receiver differential input voltage [1,2]	100	—	450	mV	—	—
ΔF_RX_PAD_ CORE	Duty Cycle output from Receiver pad to core side port	40	—	60	%	—	—

Table continues on the next page...

Table 14. LVDS Pads*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TSTARTUP_ LVDS_RX	Receiver startup time (receiver ready after enabling)	—	—	1	us	Includes reference startup time	—
CIN	Differential input capacitance	—	3.5	6	pF	—	—
Pin_leakage(PAD_ P/PAD_N)_ DISABLED	Pin Leakage(pad_p/ pad_n) with Rx disabled (ipp_ibe_lv = 0) [3]	-5	—	5	uA	Ipp_ibe_lv=0	—
Pin_leakage(PAD_ P/PAD_N)_ ENABLED	Pin Leakage(pad_p/ pad_n) with Rx enabled (ipp_ibe_lv = 1)	-5	—	100	uA	Ipp_ibe_lv=1	—
Ipin_leakage(PAD_ P/PAD_N)	Pin leakage (pad_p,pad_n) When Transmitter disabled [4]	-5	—	5	uA	Ipp_obe_lv=0	—

1. The LVDS input pin maximum voltage given in the operating conditions section of the datasheet must be obeyed when setting the common-mode and differential swing voltages seen by the LVDS receiver.
2. The high gain configuration is selected by programming MSCR501[RXCB] for Zipwire_0 and MSCR503[RXCB] for Zipwire_1 in SIUL2_1. High gain setting is used for 420Mbps operation and the low gain setting is used for up to 320Mbps operation.
3. When measuring leakage, both pad_p and pad_n should be shorted together and driven to 1.8V supply or ground
4. For pin leakage drive both pad_p and pad_n to high or low together and measure pin current

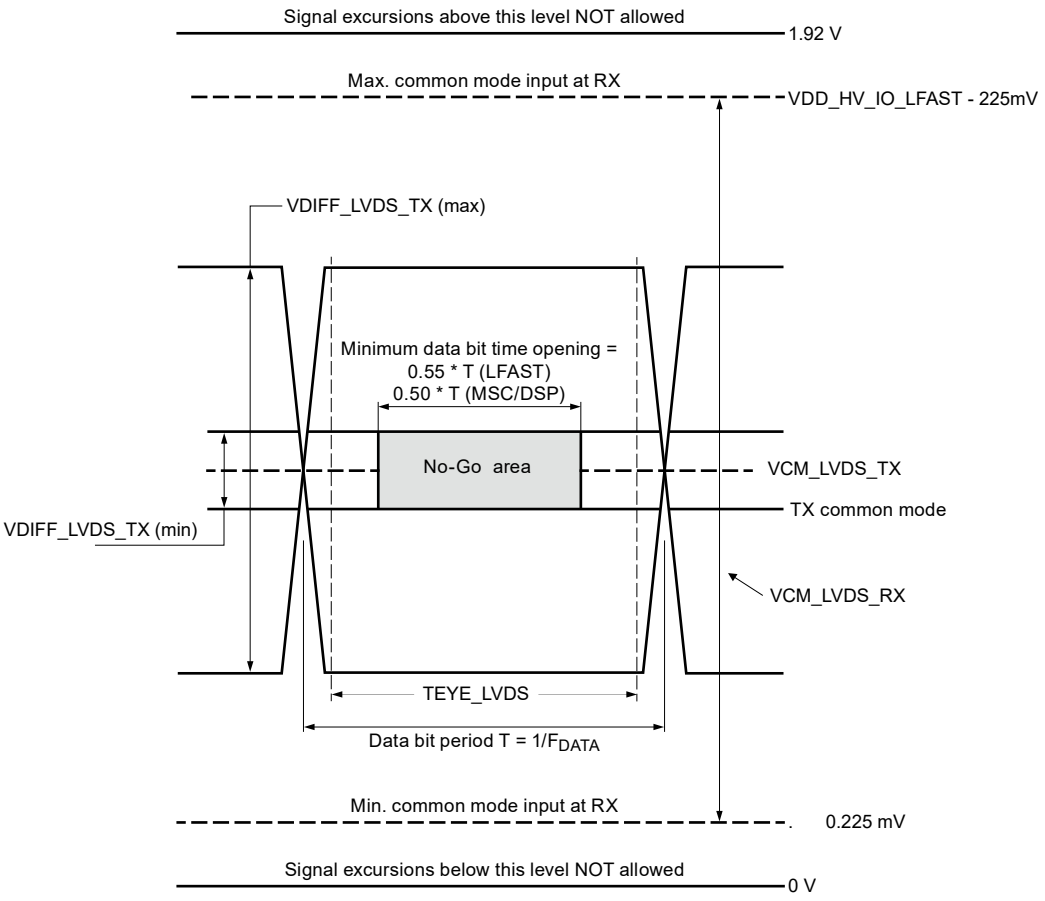


Figure 8. LFAST timing definition

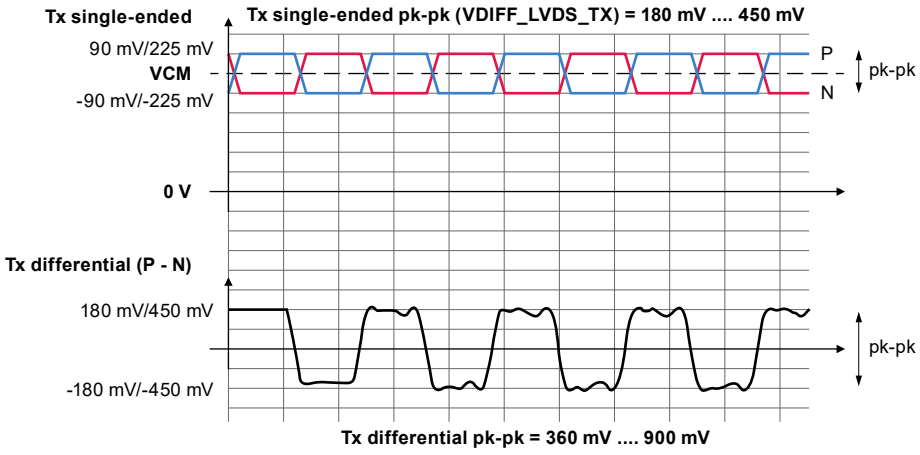


Figure 9. VDIFF_LVDS_TX pk-pk in single ended and differential mode

10.3 Reset related pad electrical characteristics

The following table gives the characteristics of the POR_B and RESET_B pads.

Values not explicitly listed in this table can be found in the 'GPIO Pads' section.

Table 15. Reset related pad electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
ISLEW_POR_B	POR_B slew rate	30e-06	—	4	V/ns	—	—
ISLEW_RESET_B	RESET_B slew rate [1]	30e-06	—	4	V/ns	Noise on RESET_B <100mV peak-peak.	—
VISE_RESET_B	RESET_B pad indeterminate state end threshold	—	2.35	—	V	See RESET_B pad detailed behavior diagram below	—
VRSE_RESET_B	RESET_B pad ramp-up state end threshold	—	460	—	mV	See RESET_B pad detailed behavior diagram below	—
WF_RESET_B	RESET_B input filtered pulse	—	—	17	ns	—	—
WNF_RESET_B	RESET_B input not filtered pulse	400	—	—	ns	—	—
MLP_POR_B	POR_B minimum low pulse	5	—	—	us	—	—

1. ISLEW_RESET_B(Min) = MAX[30e-06, 0.002 * Vnoise_p_p * Fnoise], where Vnoise_p_p is peak-peak noise magnitude (in V) and Fnoise is max noise frequency (in MHz).

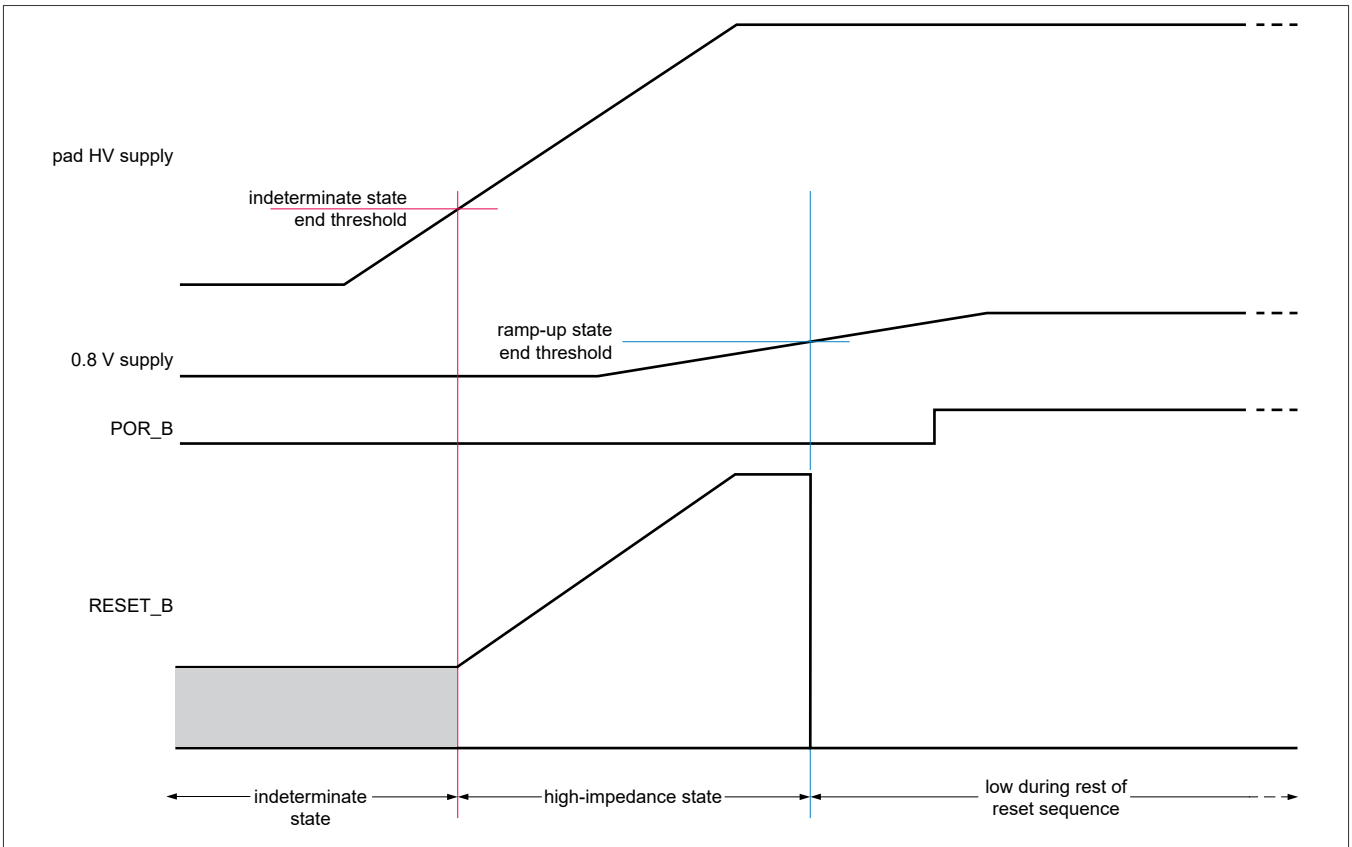


Figure 10. RESET_B pad detailed behavior

The RESET_B pad behavior described in the diagram and the related VRSE_RESET_B parameter spec also apply to the case of core VDD droop after power-up.

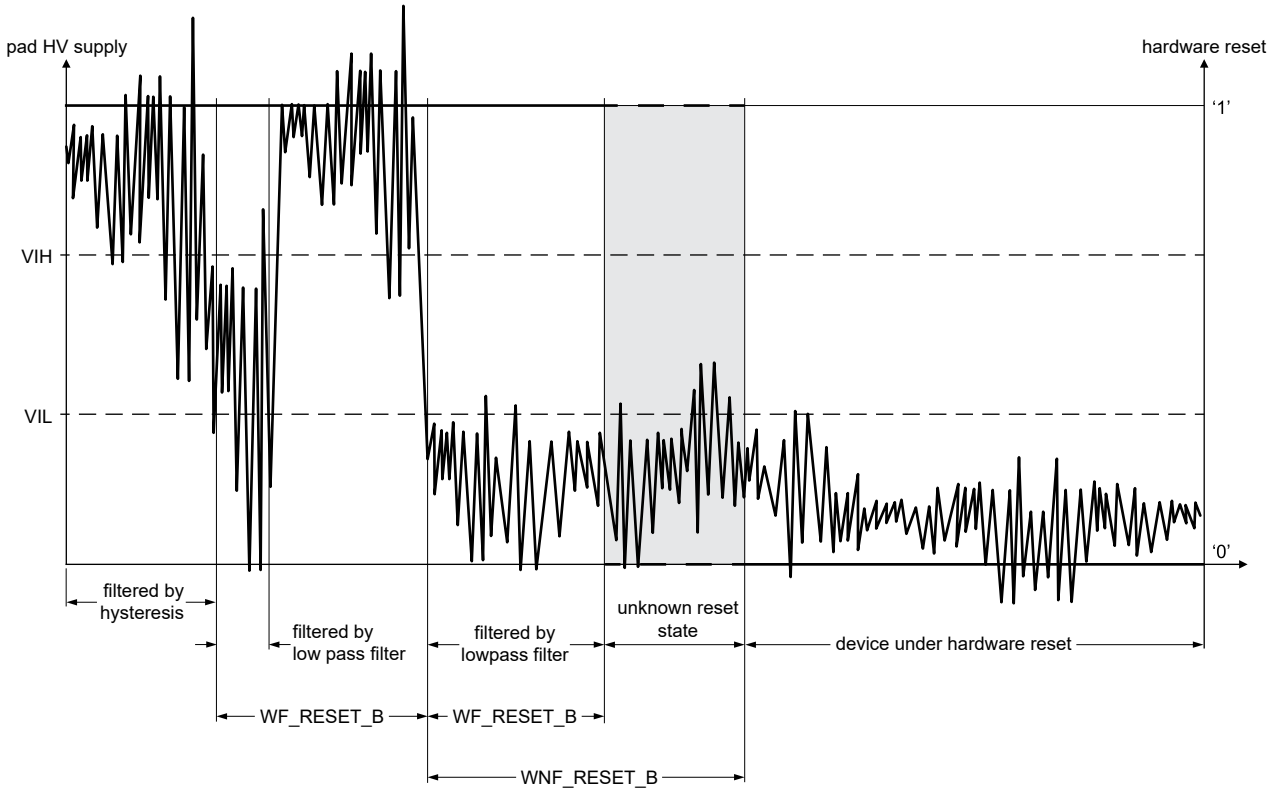


Figure 11. Noise filtering on RESET_B pad

During SoC power-up, the PMIC asserts the POR_B input before the SoC supplies are turned on and kept asserted until all SoC supplies have reached their operational levels (i.e., all the corresponding voltage monitors in the PMIC have been satisfied) and any required PMIC BIST has completed. See the 'Power Sequencing' section for details.

The PMIC asserts the POR_B input whenever one of its voltage detectors detects an SoC supply's voltage is outside its operational range (i.e., a corresponding PMIC LVD or HVD event occurs).

10.4 AE GPIO Input DC

Table 16. AE GPIO Input DC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIH	GPIO Input high level DC voltage threshold [1]	0.65 * VDDH	—	VDDH + 0.3	V	with hysteresis	—
VIL	GPIO Input low level DC voltage threshold [1]	VSS - 0.3	—	0.35 * VDDH	V	with hysteresis	—
VIH	GPIO Input high level DC voltage threshold [1]	0.55 * VDDH	—	VDDH + 0.3	V	without hysteresis	—

Table continues on the next page...

Table 16. AE GPIO Input DC...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIL	GPIO Input low level DC voltage threshold [1]	VSS - 0.3	—	0.4 * VDDH	V	without hysteresis	—
VHYS	GPIO Input hysteresis voltage [1]	0.1 * VDDH	—	—	V	—	—
ILKG	GPO Input leakage current	-2.5	—	2.5	uA	pull up/down disabled	—
CIN	GPIO Input pin capacitance	—	—	6	pF	—	—

1. VDDH = VDD_HV_IO_D0 | VDD_HV_IO_D1

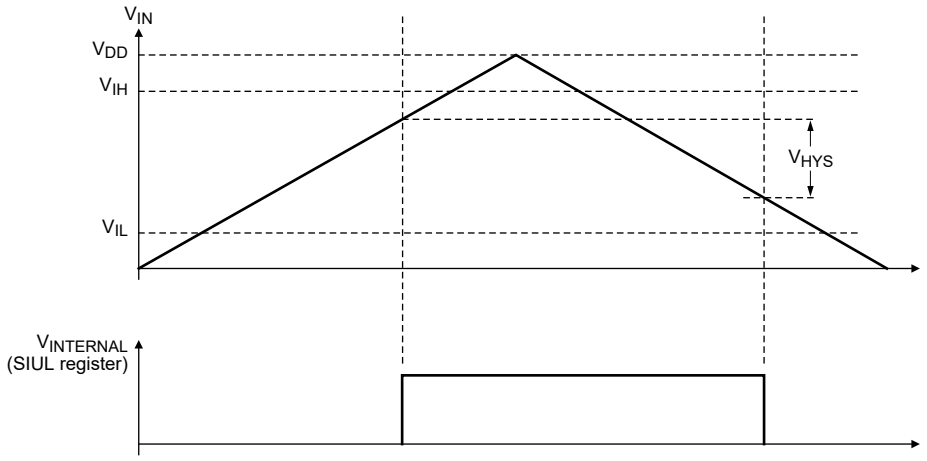


Figure 12. GPIO Input DC Characteristics

10.5 AE GPIO Output DC

Table 17. AE GPIO Output DC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VOH	GPIO output high voltage [1]	0.8 * VDDH	—	—	V	—	—
VOL	GPIO output low voltage [1]	—	—	0.2 * VDDH	V	—	—
|IWPU|	GPIO weak pull up current (absolute value)	10	—	55	uA	—	—
|IWPD|	GPIO weak pull down current (absolute value)	10	—	55	uA	—	—

1. VDDH = VDD_HV_IO_D0 | VDD_HV_IO_D1

10.6 AE GPIO Output AC

Table 18. AE GPIO Output AC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IOH	GPIO output high current [1,2]	18	—	70	mA	full drive (SIUL_ MSCRx[SRE] = 0b11), VDDH = 3.465V	—
IOL	GPIO output low current [1,2]	21	—	120	mA	full drive (SIUL_ MSCRx[SRE] = 0b11), VDDH = 3.465V	—
IOH	GPIO output high current [1,2]	38	—	132	mA	full drive (SIUL_ MSCRx[SRE] = 0b11), VDDH = 5.25V	—
IOL	GPIO output low current [1,2]	48	—	220	mA	full drive (SIUL_ MSCRx[SRE] = 0b11), VDDH = 5.25V	—
IAV	GPIO average output current [1,2,3]	—	—	13	mA	full drive (SIUL_ MSCRx[SRE] = 0b11), CLOAD = 25pF, VDDH = 3.465V, fmax = 83.3MHz	—
IRMS	GPIO RMS output current [1,2,3]	—	—	37	mA	full drive (SIUL_ MSCRx[SRE] = 0b11), CLOAD = 25pF, VDDH = 3.465V, fmax = 83.3MHz	—
IAV	GPIO average output current [1,2,3]	—	—	16	mA	full drive (SIUL_ MSCRx[SRE] = 0b11), CLOAD = 50pF, VDDH = 3.465V, fmax = 66.7MHz	—
IRMS	GPIO RMS output current [1,2,3]	—	—	36	mA	full drive (SIUL_ MSCRx[SRE] = 0b11), CLOAD = 50pF, VDDH = 3.465V, fmax = 66.7MHz	—
IAV	GPIO average output current [1,2,3]	—	—	36	mA	full drive (SIUL_ MSCRx[SRE] = 0b11), CLOAD = 25pF, VDDH = 5.25V, fmax = 111MHz	—
IRMS	GPIO RMS output current [1,2,3]	—	—	83	mA	full drive (SIUL_ MSCRx[SRE] = 0b11), CLOAD = 25pF, VDDH = 5.25V, fmax = 111MHz	—

Table continues on the next page...

Table 18. AE GPIO Output AC*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IAV	GPIO average output current [1,2,3]	—	—	42	mA	full drive (SIUL_ MSCRx[SRE] = 0b11), CLOAD = 50pF, VDDH = 5.25V, fmax = 98MHz	—
IRMS	GPIO RMS output current [1,2,3]	—	—	89	mA	full drive (SIUL_ MSCRx[SRE] = 0b11), CLOAD = 50pF, VDDH = 5.25V, fmax = 98MHz	—
fmax	GPIO output frequency [1,2,3]	—	—	83.3	MHz	full drive (SIUL_ MSCRx[SRE] = 0b11), VDDH = 3.465V, CLOAD = 25pF	—
fmax	GPIO output frequency [1,2,3]	—	—	66.7	MHz	full drive (SIUL_ MSCRx[SRE] = 0b11), VDDH = 3.465V, CLOAD = 50pF	—
fmax	GPIO output frequency [1,2,3]	—	—	111	MHz	full drive (SIUL_ MSCRx[SRE] = 0b11), VDDH = 5.25V, CLOAD = 25pF	—
fmax	GPIO output frequency [1,2,3]	—	—	98	MHz	full drive (SIUL_ MSCRx[SRE] = 0b11), VDDH = 5.25V, CLOAD = 50pF	—
TRISE / TFALL	GPIO output rise/fall time [1,2,3,4]	—	—	1.5/1.5	ns	full drive (SIUL_ MSCRx[SRE] = 0b11), VDDH = 3.465V, CLOAD = 25pF	—
TRISE / TFALL	GPIO output rise/fall time [1,2,3,4]	0.9/0.9	—	3/3	ns	full drive (SIUL_ MSCRx[SRE] = 0b11), VDDH = 3.465V, CLOAD = 50pF	—
TRISE / TFALL	GPIO output rise/fall time [1,2,3,4]	—	—	1.2/1.2	ns	full drive (SIUL_ MSCRx[SRE] = 0b11), VDDH = 5.25V, CLOAD = 25pF	—
TRISE / TFALL	GPIO output rise/fall time [1,2,3,4]	—	—	2/2	ns	full drive (SIUL_ MSCRx[SRE] = 0b11), VDDH = 5.25V, CLOAD = 50pF	—

Table continues on the next page...

Table 18. AE GPIO Output AC*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IOH	GPIO output high current [1,2]	9	—	35	mA	half drive (SIUL_ MSCRx[SRE] = 0b10), VDDH = 3.465V	—
IOL	GPIO output low current [1,2]	10.5	—	60	mA	half drive (SIUL_ MSCRx[SRE] = 0b10), VDDH = 3.465V	—
IOH	GPIO output high current [1,2]	19	—	66	mA	half drive (SIUL_ MSCRx[SRE] = 0b10), VDDH = 5.25V	—
IOL	GPIO output low current [1,2]	24	—	110	mA	half drive (SIUL_ MSCRx[SRE] = 0b10), VDDH = 5.25V	—
IAV	GPIO average output current [1,2,3]	—	—	8	mA	half drive (SIUL_ MSCRx[SRE] = 0b10), CLOAD = 25pF, VDDH = 3.465V, fmax = 62.5MHz	—
IRMS	GPIO RMS output current [1,2,3]	—	—	20	mA	half drive (SIUL_ MSCRx[SRE] = 0b10), CLOAD = 25pF, VDDH = 3.465V, fmax = 62.5MHz	—
IAV	GPIO average output current [1,2,3]	—	—	9	mA	half drive (SIUL_ MSCRx[SRE] = 0b10), CLOAD = 50pF, VDDH = 3.465V, fmax = 43.4MHz	—
IRMS	GPIO RMS output current [1,2,3]	—	—	21	mA	half drive (SIUL_ MSCRx[SRE] = 0b10), CLOAD = 50pF, VDDH = 3.465V, fmax = 43.4MHz	—
IAV	GPIO average output current [1,2,3]	—	—	25	mA	half drive (SIUL_ MSCRx[SRE] = 0b10), CLOAD = 25pF, VDDH = 5.25V, fmax = 95MHz	—
IRMS	GPIO RMS output current [1,2,3]	—	—	53	mA	half drive (SIUL_ MSCRx[SRE] = 0b10), CLOAD = 25pF, VDDH = 5.25V, fmax = 95MHz	—

Table continues on the next page...

Table 18. AE GPIO Output AC*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IAV	GPIO average output current [1,2,3]	—	—	21	mA	half drive (SIUL_ MSCRx[SRE] = 0b10), CLOAD = 50pF, VDDH = 5.25V, fmax = 62.5MHz	—
IRMS	GPIO RMS output current [1,2,3]	—	—	44	mA	half drive (SIUL_ MSCRx[SRE] = 0b10), CLOAD = 50pF, VDDH = 5.25V, fmax = 62.5MHz	—
fmax	GPIO output frequency [1,2,3]	—	—	62.5	MHz	half drive (SIUL_ MSCRx[SRE] = 0b10), VDDH = 3.465V, CLOAD = 25pF	—
fmax	GPIO output frequency [1,2,3]	—	—	43.4	MHz	half drive (SIUL_ MSCRx[SRE] = 0b10), VDDH = 3.465V, CLOAD = 50pF	—
fmax	GPIO output frequency [1,2,3]	—	—	95	MHz	half drive (SIUL_ MSCRx[SRE] = 0b10), VDDH = 5.25V, CLOAD = 25pF	—
fmax	GPIO output frequency [1,2,3]	—	—	62.5	MHz	half drive (SIUL_ MSCRx[SRE] = 0b10), VDDH = 5.25V, CLOAD = 50pF	—
TRISE / TFALL	GPIO output rise/fall time [1,2,3,4]	0.6/0.8	—	3.5/3.5	ns	half drive (SIUL_ MSCRx[SRE] = 0b10), VDDH = 3.465V, CLOAD = 25pF	—
TRISE / TFALL	GPIO output rise/fall time [1,2,3,4]	1.8/1.2	—	6.5/6.5	ns	half drive (SIUL_ MSCRx[SRE] = 0b10), VDDH = 3.465V, CLOAD = 50pF	—
TRISE / TFALL	GPIO output rise/fall time [1,2,3,4]	—	—	2/2	ns	half drive (SIUL_ MSCRx[SRE] = 0b10), VDDH = 5.25V, CLOAD = 25pF	—
TRISE / TFALL	GPIO output rise/fall time [1,2,3,4]	—	—	4/4	ns	half drive (SIUL_ MSCRx[SRE] = 0b10), VDDH = 5.25V, CLOAD = 50pF	—

Table continues on the next page...

Table 18. AE GPIO Output AC*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fmax	GPIO output frequency [1,2,3]	—	—	11	MHz	fast slew rate (SIUL_ MSCRx[SRE] = 0b01), VDDH = 3.465V, CLOAD = 50pF	—
fmax	GPIO output frequency [1,2,3]	—	—	18.5	MHz	fast slew rate (SIUL_ MSCRx[SRE] = 0b01), VDDH = 5.25V, CLOAD = 50pF	—
TRISE / TFALL	GPIO output rise/fall time [1,2,3,4]	4/3.5	—	25/25	ns	fast slew rate (SIUL_ MSCRx[SRE] = 0b01), VDDH = 3.465V, CLOAD = 50pF	—
TRISE / TFALL	GPIO output rise/fall time [1,2,3,4]	—	—	12/12	ns	fast slew rate (SIUL_ MSCRx[SRE] = 0b01), VDDH = 5.25V, CLOAD = 50pF	—
fmax	GPIO output frequency [1,2,3]	—	—	6.7	MHz	slow slew rate (SIUL_ MSCRx[SRE] = 0b00), VDDH = 3.465V, CLOAD = 50pF	—
fmax	GPIO output frequency [1,2,3]	—	—	12.5	MHz	slow slew rate (SIUL_ MSCRx[SRE] = 0b00), VDDH = 5.25V, CLOAD = 50pF	—
TRISE / TFALL	GPIO output rise/fall time [1,2,3,4]	6.8/6	—	40/40	ns	slow slew rate (SIUL_ MSCRx[SRE] = 0b00), VDDH = 3.465V, CLOAD = 50pF	—
TRISE / TFALL	GPIO output rise/fall time [1,2,3,4]	—	—	24/24	ns	slow slew rate (SIUL_ MSCRx[SRE] = 0b00), VDDH = 5.25V, CLOAD = 50pF	—

1. GPIO pad specifications are derived from Spice simulations and are not production tested.
2. VDDH = VDD_HV_IO_D0 | VDD_HV_IO_D1.
3. C LOAD is the total of the external load plus the output driver and package parasitic capacitance.
4. Measured in relation to V OH /V OL .

11 Aurora Specifications

11.1 Aurora Pads

Table 19. Aurora Pads

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fAURORA	Data Rate	0.05	—	5.0	Gbps	100Ω external termination (Not on board but inside receiver after AC coupling)	—
IDD_HV_AUR	Transmitter HV supply current consumption (No pre-emphasis)	18	22	31	mA	max fAURORA per active transmit lane	—
IDD_HV_AUR	Transmitter HV supply current consumption (pre-emphasis enabled , pre-emphasis gain=11)	25	30	40	mA	max fAURORA per active transmit lane	—
VOD_AURORA_AC	Transmitter Differential output voltage (end termination) [1,2,3]	400	600	900	mV	max fAURORA, 100Ω termination, 100Ω differential transmission line delay, matched network	—
VOD_AURORA_DC	DC range for the VOD (Transmitter Differential Output Voltage)	800	—	—	mV	ipp_obe=1 DC condition	—
VOD_AURORA_AC_PRE_EMPH	Transmitter Differential output voltage (end termination, preemph=11) [1,2,4]	600	900	1200	mV	max fAURORA, 100Ω termination, 100Ω differential transmission line delay, matched network	—
VCM_AURORA	Transmitter Common mode voltage	0.775	—	1.025	V	—	—
VCM_LVDS_RX	Receiver input signal common mode range	0.6	—	1.0	V	—	—
VDIFF_LVDS_RX	Receiver input differential signal	400	—	—	mV	—	—
CLOAD_AURORA	Maximum transmission line load (Lumped Load	—	—	0.1	pF	—	—

Table continues on the next page...

Table 19. Aurora Pads...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	at any point on Tline)						
RTERM_AURORA	Internal termination resistance	80	100	130	Ohm	enabled	—
VSLEW_AURORA	Differential output slew rate	—	30	50	ps / 200mV	max fAURORA	—
TSTARTUP_AURORA	Transmitter startup time (assertion of ipp_obe to common mode settling of differential output)	—	—	500	ns	—	—
TEYE_AURORA	Valid data region (Including PLL Jitter for Aurora) [5]	0.55	—	—	UI	max fAURORA	—
VOH_AURORA	Transmitter output high indicator [6]	VDD_IO/ 2 + 0.2	—	—	V	100Ω termination at receiver end	—
VOL_AURORA	Transmitter output low indicator [6]	—	—	VDD_IO/ 2 - 0.2	V	100Ω termination at receiver end	—
PAD_P_BIAS	Pad_p voltage output level when Tx disabled	—	—	0.6	V	Ipp_obe_lv=0 Ipp_term_en_lv=0	—
PAD_N_BIAS	Pad_n voltage output level when Tx disabled	1.1	—	—	V	Ipp_obe_lv=0 Ipp_term_en_lv=0	—

1. When operating at max speed, there will be losses and differential output will be smaller as against DC condition. Aurora Interface Min differential swing is 400mV which is always guaranteed but the max limit is dependent on board design/ losses. For boards with negligible losses , if differential output (P-N) goes higher than 800mV (Aurora max differential input spec) , user must use “dual termination” scheme as highlighted in the Source Termination Circuit Figure to get the differential swing back within Range. The termination in the source side can be enabled through software in the transmitter pad design. Direct end termination without AC coupling is not allowed.
2. Termination scheme as shown in the End Termination Circuit Figure. Direct end termination without AC coupling is not allowed.
3. Differential output is with pre-emphasis disabled, and a 10mA output stage current.
4. Differential output is with pre-emphasis enabled, and a ~15mA avg output stage current
5. UI @ 5Gbps equals 200ps. The valid eye is expected to be > 110ps in width. ISI jitter spec is 20-30ps for the LVDS transmitter across PVT in a delay matched differential transmission line impedance of 100Ω.
6. VDD_IO maps to corresponding supply name on the device.

Termination scheme as shown in “End Termination Circuit” applies to debug tool hardware and is not recommended to be placed on the PC.

Source termination Circuit – Transmitter side 100 ohm termination is present inside the Tx pad and should not be placed on the PCB.

Direct 100 ohm board termination not allowed between AUR_TXn_N and AUR_TXn_N (n=0,1,2,3). Source termination is only allowed through the internal termination inside LVDS Tx pad.

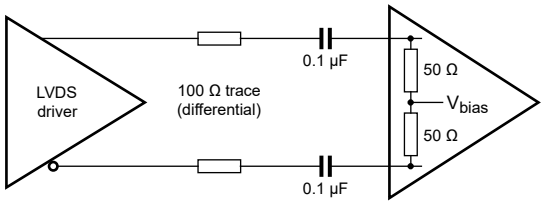


Figure 13. End Termination Circuit

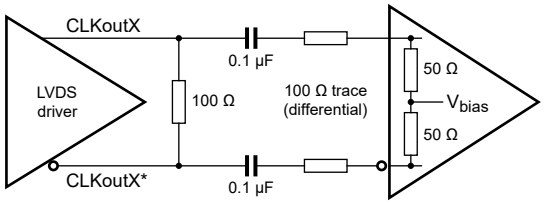


Figure 14. Source Termination Circuit

11.2 Aurora Port Timing

The following table gives the Aurora Port interface timing specifications for the device.

Table 20. Aurora Port Timing

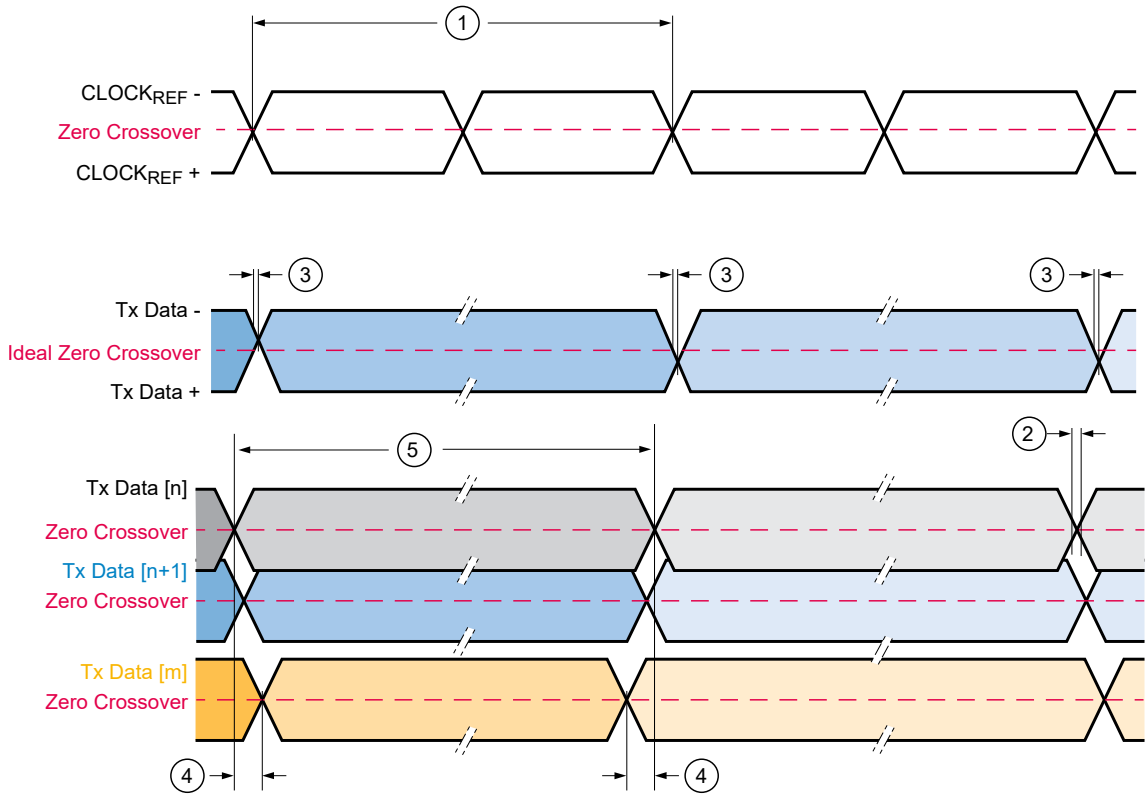
Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
BER	Bit Error Rate	—	—	10e-12	—	—	—
JD	Transmit line deterministic jitter	—	—	0.17	OUI	data rate <=3.0 Gbps	—
JD	Transmit line deterministic jitter	—	—	0.25	OUI	3.0Gbps < data rate <= 5.0Gbps	—
JT	Transmit line total jitter	—	—	0.35	OUI	data rate <= 3.0 Gbps	2
JT	Transmit line total jitter	—	—	0.45	OUI	3.0Gbps < data rate <= 5.0Gbps	2
SO	Differential output skew	—	—	20	ps	—	3
SMO	Lane to lane output skew	—	—	1000	ps	—	4
OUI	Aurora lane unit interval [1,2]	—	500	—	ps	2.0 Gbps	5
OUI	Aurora lane unit interval [1,2]	—	400	—	ps	2.5 Gbps	5
OUI	Aurora lane unit interval [1,2]	—	333	—	ps	3.0 Gbps	5
OUI	Aurora lane unit interval [1,2]	—	294	—	ps	3.4 Gbps	5

Table continues on the next page...

Table 20. Aurora Port Timing...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
OUI	Aurora lane unit interval [1,2]	—	250	—	ps	4.0 Gbps	5
OUI	Aurora lane unit interval [1,2]	—	200	—	ps	5.0 Gbps	5

1. +/- 100 PPM.
2. The Aurora interface supports data rates of 2.0, 2.5, 3.0, 3.4, 4.0, and 5.0 Gbps.



For spec number 1, see Aurora PLL specifications
For rest, see Aurora port specifications

Figure 15. Aurora Debug Port Timing

11.3 Aurora PLL

The following table gives the operating frequencies and characteristics of the Aurora PLL. The operating frequencies correspond to the supported Aurora data trace lane speed. The Aurora PLL works from an external 100MHz input reference clock, and achieves a maximum output frequency of 5GHz.

Table 21. Aurora PLL

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fPLL_CLKIN	Aurora PLL Input Reference Clock Frequency [1,2,3]	40	—	100	MHz	—	—
fPLL_CLKIN_PFD	Aurora PLL Phase Detector Clock Frequency [4]	—	100	—	MHz	—	—
ΔfPLL_CLKIN	Aurora PLL Input Reference Clock Duty Cycle [1]	40	—	60	%	—	—
JRCDC	Reference clock period jitter	—	—	5	ps	RMS, 0.5MHz - 20MHz	—
fPLL_VCO	Aurora PLL VCO Frequency Range	3000	—	5000	MHz	—	—
fPLL_CLKOUT0	Aurora PLL Output Clock 0 Frequency Range [5]	—	—	5000	MHz	5.0Gbps Aurora lane data rate, VCO frequency divided by 1	—
fPLL_CLKOUT0	Aurora PLL Output Clock 0 Frequency Range [5]	—	—	4000	MHz	4.0Gbps Aurora lane data rate, VCO frequency divided by 1	—
fPLL_CLKOUT0	Aurora PLL Output Clock 0 Frequency Range [5]	—	—	3400	MHz	3.4Gbps Aurora lane data rate, VCO frequency divided by 1	—
fPLL_CLKOUT0	Aurora PLL Output Clock 0 Frequency Range [5]	—	—	3000	MHz	3.0Gbps Aurora lane data rate, VCO frequency divided by 1	—
fPLL_CLKOUT0	Aurora PLL Output Clock 0 Frequency Range [5]	—	—	2500	MHz	2.5Gbps Aurora lane data rate, VCO frequency divided by 2.	—
fPLL_CLKOUT0	Aurora PLL Output Clock 0 Frequency Range [5]	—	—	2000	MHz	2.0Gbps Aurora lane data rate, VCO frequency divided by 2.	—
fPLL_CLKOUT0	Aurora PLL Output Clock 0 Frequency Range	—	—	500	MHz	No tool connected - trace logic clock with FXOSC reference clock.	—
tLOCK	Aurora PLL Lock Time	—	—	150	us	—	—
PER_jitter	Aurora PLL Period Jitter	-21	—	21	ps	fPLL_CLKIN = 40MHz | 100MHz, VCO = 5GHz, fPLL_CLKOUT = 5GHz, 6-sigma wirebond L < 2nH	—

Table continues on the next page...

Table 21. Aurora PLL...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
LT_jitter	Aurora PLL Long Term Jitter	-120	—	120	ps	Saturated, 6-sigma	—

1. Refer to the LVDS Pad specifications for additional Aurora PLL reference clock electrical specifications. Also see " Aurora Debug Port Timing" figure for fPLL_CLKIN as spec number 1.
2. 100MHz is the only input reference frequency supported for the Aurora PLL.
3. 40MHz is the only internal input reference frequency supported for the Aurora PLL.
4. It is Aurora PLL Input Reference Clock Frequency after pre-divider.
5. The Aurora PLL is only validated at the frequencies specified within this table - these frequencies correspond to the limited set of Aurora data lane rates that are supported for the device.

12 Power Management

12.1 PMC Bandgap

Table 22. PMC Bandgap

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VBG_SCALED	Scaled version of bandgap reference voltage measured by SAR ADC [1]	1.127	1.150	1.173	V	Both bandgap and buffer are trimmed	—

1. ADC conversion error must be included when reading the bandgap reference voltage via the chip ADC.

12.2 AE PMC Regulator

Table 23. AE PMC Regulator

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
REG12_VDD12	1.2V Regulator DC output voltage	1209	1273	1337	mV	Excluding transients, trimmed	—
REG12_CLOAD	1.2V Regulator external bypass capacitor [1]	1.1	2.2	—	uF	—	—

1. Degradation to 1.1uF is possible due to tolerance and aging.

12.3 AE Supply Monitoring

Table 24. AE Supply Monitoring

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
POR_VDDC	Core supply power-on reset detector, coarse	540	720	900	mV	rising	—
POR_VDDC	Core supply power-on reset detector, coarse	500	660	860	mV	falling	—
POR081_C	Core supply low range low voltage detector	812	855	898	mV	rising	—
POR081_C	Core supply low range low voltage detector	812	855	898	mV	falling	—
LVD114_C	Core supply low voltage detector	1074	1131	1188	mV	untrimmed, rising	—
LVD114_C	Core supply low voltage detector	1074	1131	1188	mV	untrimmed, falling	—
LVD114_C	Core supply low voltage detector	1140	1169	1198	mV	trimmed, rising	—
LVD114_C	Core supply low voltage detector	1140	1169	1198	mV	trimmed, falling	—
LVD114_F	Flash core supply low voltage detector	1071	1127	1183	mV	untrimmed, rising	—
LVD114_F	Flash core supply low voltage detector	1071	1127	1183	mV	untrimmed, falling	—
LVD114_F	Flash core supply low voltage detector	1099	1127	1155	mV	trimmed, rising	—
LVD114_F	Flash core supply low voltage detector	1099	1127	1155	mV	trimmed, falling	—
HVD140_C	Core supply high voltage detector	1381	1454	1527	mV	untrimmed, rising	—
HVD140_C	Core supply high voltage detector	1381	1454	1527	mV	untrimmed, falling	—
HVD140_C	Core supply high voltage detector	1384	1419	1454	mV	trimmed, rising	—
HVD140_C	Core supply high voltage detector	1384	1419	1454	mV	trimmed, falling	—

Table continues on the next page...

Table 24. AE Supply Monitoring...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
POR_VDDREG	PMC 3.3V supply power-on reset detector, coarse	1.598	2.13	2.7	V	rising	—
POR_VDDREG	PMC 3.3V supply power-on reset detector, coarse	1.498	2.03	2.562	V	falling	—
LVD280_C	PMC supply low voltage detector	2.736	2.88	3.024	V	untrimmed, rising	—
LVD280_C	PMC supply low voltage detector	2.689	2.83	2.972	V	untrimmed, falling	—
LVD280_C	PMC supply low voltage detector	2.75	2.88	2.952	V	trimmed, rising	—
LVD280_C	PMC supply low voltage detector	2.74	2.83	2.901	V	trimmed, falling	—
LVD280_F	Flash high voltage supply low voltage detector	2.736	2.88	3.024	V	untrimmed, rising	—
LVD280_F	Flash high voltage supply low voltage detector	2.689	2.83	2.972	V	untrimmed, falling	—
LVD280_F	Flash high voltage supply low voltage detector	2.75	2.88	2.952	V	trimmed, rising	—
LVD280_F	Flash high voltage supply low voltage detector	2.74	2.83	2.901	V	trimmed, falling	—

13 Reset Duration

The durations specified "Reset Duration" table and the corresponding figures refer to standard reset sequences. A reset sequence is no longer standard when it is interrupted by another power-on or destructive reset event, in which case the reset sequence restarts from the beginning of the reset sequence corresponding to that event, and the total duration is the time already spent in reset plus the duration of the new sequence.

The diagrams in this section are not to scale.

Table 25. Reset Duration

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TFR	Functional Reset Sequence Duration	—	—	545	us	FIRC_CLK, trimmed	—

Table continues on the next page...

Table 25. Reset Duration...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TDR	Destructive Reset Sequence Duration	—	—	1370	us	FIRC_CLK, trimmed during destructive reset phase	—
POR	Power On Reset Sequence Duration	—	—	1500	us	FIRC_CLK, trimmed during destructive reset phase	—

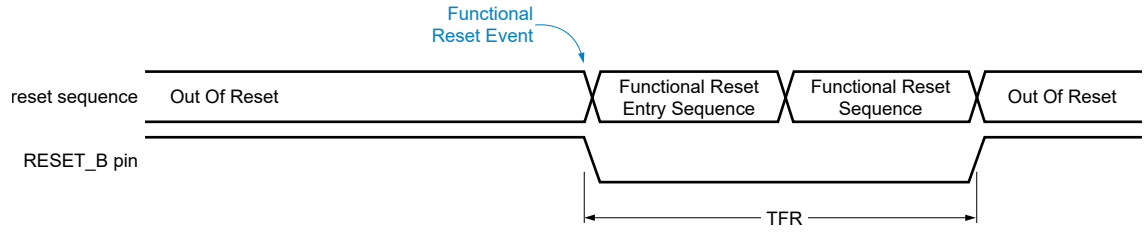


Figure 16. Functional reset

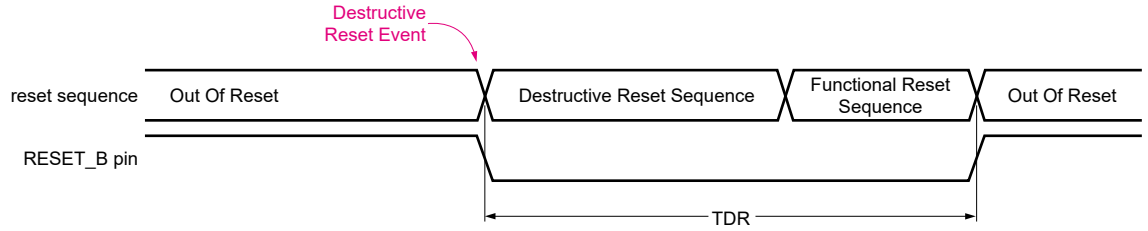


Figure 17. Destructive reset

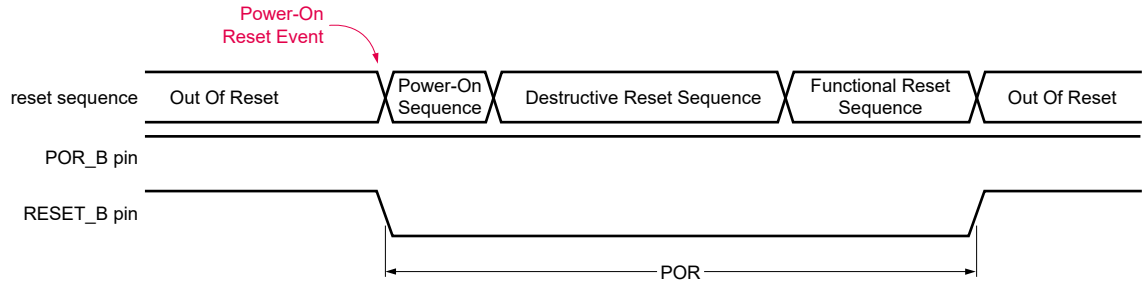


Figure 18. POR due to internal POR event

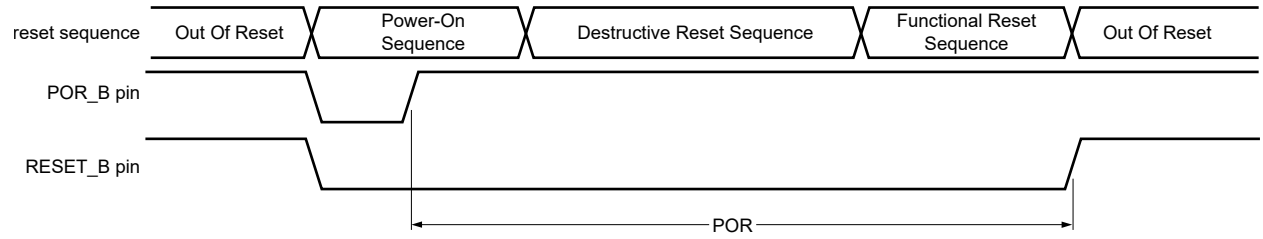


Figure 19. POR due to POR_B pin assertion

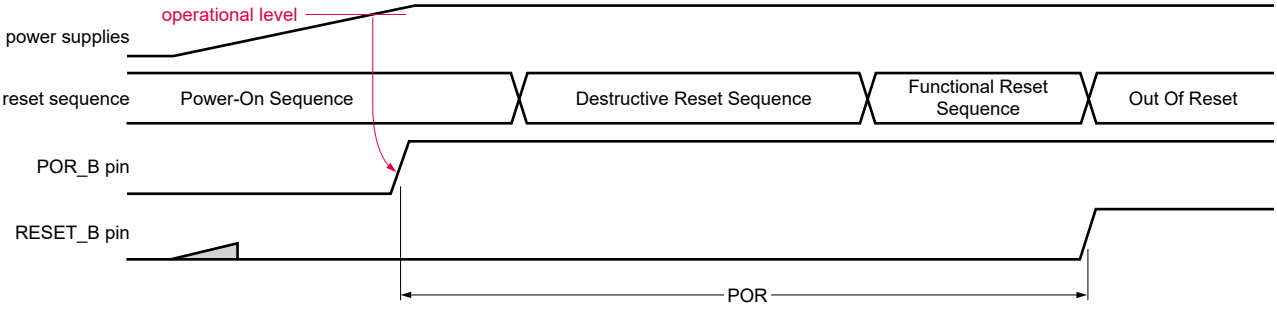


Figure 20. Initial power-up

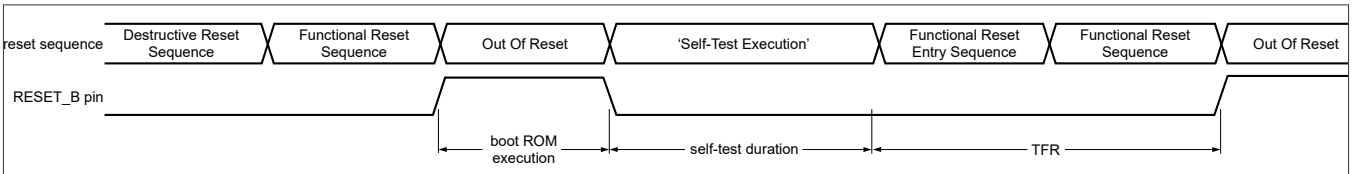


Figure 21. Start-up self-test

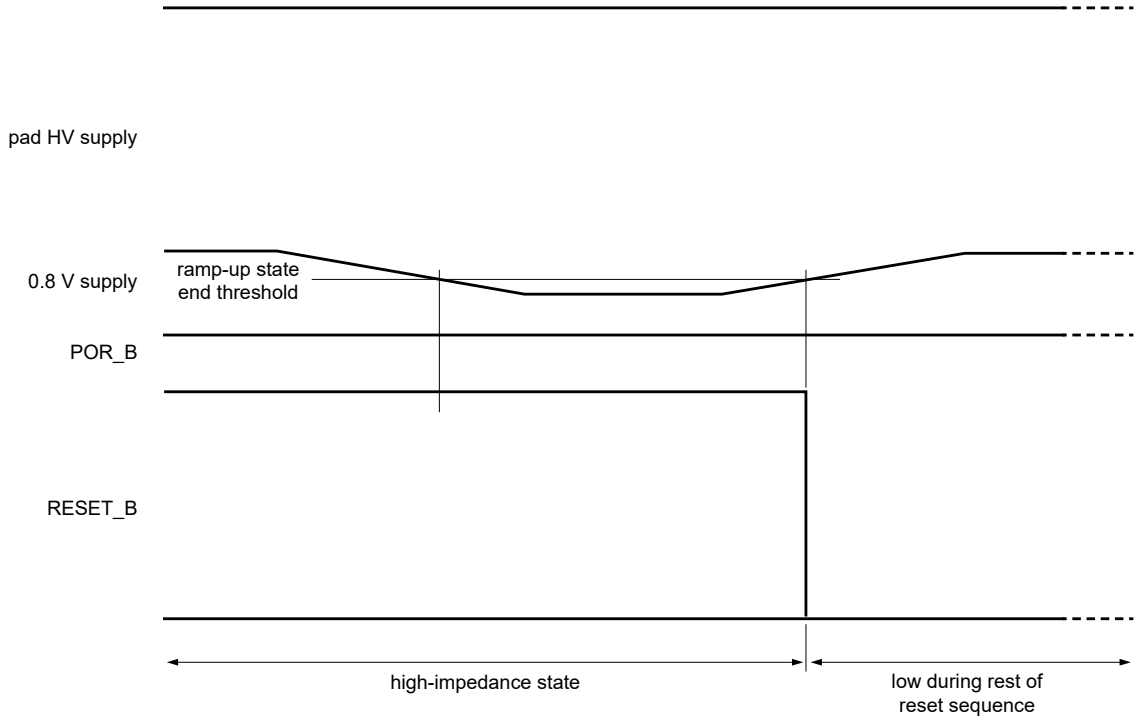


Figure 22. Reset_b pad detailed behavior during core supply brownout

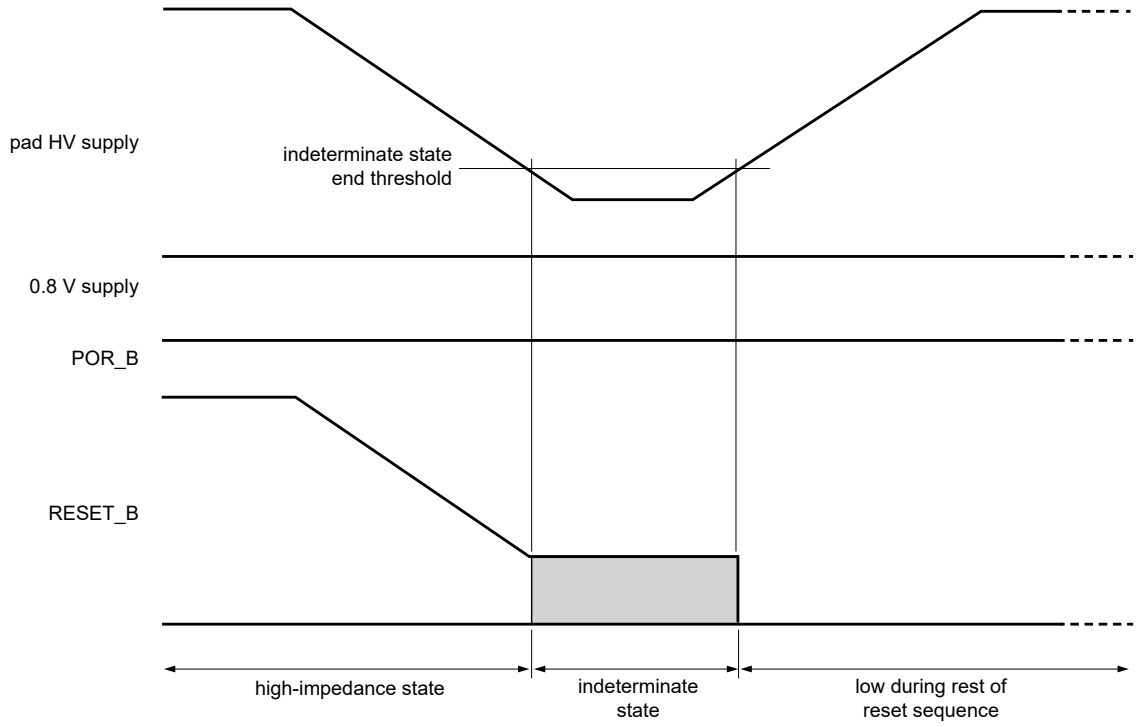


Figure 23. Reset_b pad detailed behavior during pad HV supply brownout

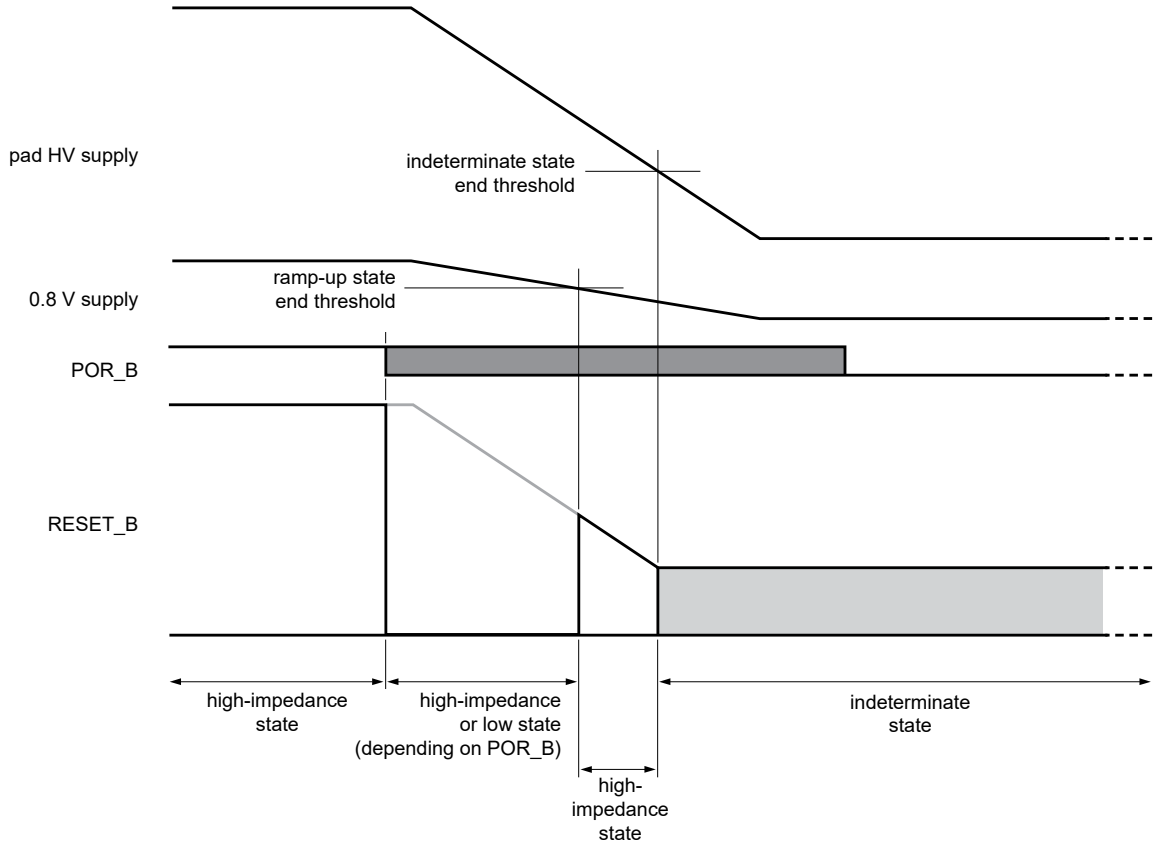


Figure 24. Reset_b pad detailed behavior during power down

14 Peripheral Specifications

14.1 Clock and PLL Interfaces

14.1.1 Clock frequency ranges

The following table gives the frequency range minimum and maximums to use when programming the clock dividers on the device.

Table 26. Clock frequency ranges

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fP0_CTU_PER_CLK	CTU clock frequency	—	—	81	MHz	P0_CTU_PER_CLK	—
fP0_DSPI_CLK	SPI_0 and SPI_1 clock frequency	—	—	102	MHz	P0_DSPI_CLK	—
fP0_DSPI_MSC_CLK	Micro second channel clock frequency	—	—	135	MHz	P0_DSPI_MSC_CLK	—
fP0_EMIOS_LCU_CLK	eMIOS_0 clock frequency	—	—	162	MHz	P0_EMIOS_LCU_CLK	—

Table continues on the next page...

Table 26. Clock frequency ranges*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fP0_FR_PE_CLK	FlexRay protocol engine clock frequency	—	—	81	MHz	P0_FR_PE_CLK	—
fP0_GTM_CLK	GTM clock frequency	—	—	405	MHz	P0_GTM_CLK	—
fP0_GTM_NOC_CLK	GTM NoC interface clock frequency	—	—	405	MHz	P0_GTM_NOC_CLK	—
fP0_GTM_TS_CLK	GTM time stamp clock frequency	—	—	81	MHz	P0_GTM_TS_CLK	—
fP0_LIN_BAUD_CLK	LINFlexD baud clock frequency	—	—	135	MHz	P0_LIN_BAUD_CLK	—
fP0_LIN_CLK	LINFlexD clock frequency	—	—	67.5	MHz	P0_LIN_CLK	—
fP0_NANO_CLK	Digital NanoEdge clock frequency	—	—	1620	MHz	P0_NANO_CLK	—
fP0_PSI5_125K_CLK	PSI5 189K clock frequency	—	—	4.05	MHz	P0_PSI5_125K_CLK	—
fP0_PSI5_189K_CLK	PSI5 125K clock frequency	—	—	6.0606	MHz	P0_PSI5_189K_CLK	—
fP0_PSI5_1US_CLK	PSI5 1us clock frequency	—	—	1.01	MHz	P0_PSI5_1US_CLK	—
fP0_PSI5_S_BAUD_CLK	PSI5_S baud clock frequency	—	—	50.625	MHz	P0_PSI5_S_BAUD_CLK	—
fP0_PSI5_S_CORE_CLK	PSI5_S core clock frequency	—	—	25.3	MHz	P0_PSI5_S_CORE_CLK	—
fP0_PSI5_S_TRIG_CLK0	PSI5_S_0 trigger clock 0 frequency	—	—	1.01	MHz	P0_PSI5_S_TRIG_CLK0	—
fP0_PSI5_S_TRIG_CLK1	PSI5_S_0 trigger clock 1 frequency	—	—	1.01	MHz	P0_PSI5_S_TRIG_CLK1	—
fP0_PSI5_S_TRIG_CLK2	PSI5_S_0 trigger clock 2 frequency	—	—	1.01	MHz	P0_PSI5_S_TRIG_CLK2	—
fP0_PSI5_S_TRIG_CLK3	PSI5_S_0 trigger clock 3 frequency	—	—	1.01	MHz	P0_PSI5_S_TRIG_CLK3	—
fP0_PSI5_S_UART_CLK	PSI5_S UART clock frequency	—	—	50.625	MHz	P0_PSI5_S_UART_CLK	—
fP0_PSI5_S_UTIL_CLK	PSI5_S UTIL clock frequency	—	—	1.01	MHz	P0_PSI5_S_UTIL_CLK	—
fP0_PSI5_S_WDOG_CLK0	PSI5_S_0 watchdog clock 0 frequency	—	—	1.01	MHz	P0_PSI5_S_WDOG_CLK0	—

Table continues on the next page...

Table 26. Clock frequency ranges*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fP0_PSI5_S_WDOG_CLK1	PSI5_S_0 watchdog clock 1 frequency	—	—	1.01	MHz	P0_PSI5_S_WDOG_CLK1	—
fP0_PSI5_S_WDOG_CLK2	PSI5_S_0 watchdog clock 2 frequency	—	—	1.01	MHz	P0_PSI5_S_WDOG_CLK2	—
fP0_PSI5_S_WDOG_CLK3	PSI5_S_0 watchdog clock 3 frequency	—	—	1.01	MHz	P0_PSI5_S_WDOG_CLK3	—
fP0_REG_INTF_2X_CLK	P0 register interface 2X clock frequency	—	—	133.33	MHz	P0_REG_INTF_2X_CLK	—
fP0_REG_INTF_CLK	P0 register interface clock frequency	—	—	133.33	MHz	P0_REG_INTF_CLK	—
fP0_SYS_CLK	P0 system clock frequency	—	—	405	MHz	P0_SYS_CLK	—
fP1_DSPI60_CLK	SPI_3 and SPI_4 clock frequency	—	—	120	MHz	P1_DSPI60_CLK	—
fP1_DSPI_CLK	SPI_2 clock frequency	—	—	102	MHz	P1_DSPI_CLK	—
fP1_LIN_BAUD_CLK	LINFlexD baud clock frequency	—	—	135	MHz	P1_LIN_BAUD_CLK	—
fP1_LIN_CLK	LINFlexD clock frequency	—	—	67.5	MHz	P1_LIN_CLK	—
fP1_NETC0_REF_RMII_CLK	ETH_0 RMII mode reference clock frequency	—	—	50	MHz	P1_NETC0_REF_RMII_CLK	—
fP1_NETC0_RX_MII_CLK	ETH_0 MII mode receive clock frequency	—	—	25	MHz	P1_NETC0_RX_MII_CLK	—
fP1_NETC0_RX_RGMII_CLK	ETH_0 RGMII mode receive clock frequency	—	—	125.75	MHz	P1_NETC0_RX_RGMII_CLK	—
fP1_NETC0_TX_LPBK_CLK	ETH_0 RGMII mode transmit loopback clock frequency	—	—	125.75	MHz	P1_NETC0_TX_LPBK_CLK	—
fP1_NETC0_TX_MII_CLK	ETH_0 MII mode transmit clock frequency	—	—	25	MHz	P1_NETC0_TX_MII_CLK	—
fP1_NETC0_TX_RGMII_CLK	ETH_0 RGMII mode transmit clock frequency	—	—	125.75	MHz	P1_NETC0_TX_RGMII_CLK	—

Table continues on the next page...

Table 26. Clock frequency ranges*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fP1_NETC1_REF_RMII_CLK	ETH_1 RMII mode reference clock frequency	—	—	50	MHz	P1_NETC1_REF_RMII_CLK	—
fP1_NETC1_RX_MII_CLK	ETH_1 MII mode receive clock frequency	—	—	25	MHz	P1_NETC1_RX_MII_CLK	—
fP1_NETC1_RX_RGMII_CLK	ETH_1 RGMII mode receive clock frequency	—	—	125.75	MHz	P1_NETC1_RX_RGMII_CLK	—
fP1_NETC1_TX_LPBK_CLK	ETH_1 RGMII mode transmit loopback clock frequency	—	—	125.75	MHz	P1_NETC1_TX_LPBK_CLK	—
fP1_NETC1_TX_MII_CLK	ETH_1 MII mode transmit clock frequency	—	—	25	MHz	P1_NETC1_TX_MII_CLK	—
fP1_NETC1_TX_RGMII_CLK	ETH_1 RGMII mode transmit clock frequency	—	—	125.75	MHz	P1_NETC1_TX_RGMII_CLK	—
fP1_NETC_AXI_CLK	Ethernet AXI bus clock frequency	—	—	330	MHz	P1_NETC_AXI_CLK	—
fP1_NETC_TS_CLK	Ethernet time stamp clock frequency	—	—	202.5	MHz	P1_NETC_TS_CLK	—
fP1_NETC_TS_DIV4_CLK	Ethernet time stamp div4 clock frequency	—	—	50.625	MHz	P1_NETC_TS_DIV4_CLK	—
fP1_REG_INTF_CLK	P1 register interface clock frequency	—	—	133.33	MHz	P1_REG_INTF_CLK	—
fP1_SYS_CLK	P1 system clock frequency	—	—	405	MHz	P1_SYS_CLK	—
fP1_SYS_DIV2_CLK	P1 system div2 clock freqeuncy	—	—	202.5	MHz	P1_SYS_DIV2_CLK	—
fP1_SYS_DIV4_CLK	P1 system div4 clock frequency	—	—	101.25	MHz	P1_SYS_DIV4_CLK	—
fP2_DBG_ATB_CLK	P2 debug ATB clock frequency	—	—	500	MHz	P2_DBG_ATB_CLK	—
fP2_MATH_CLK	P2 Math accelerator clock frequency	—	—	405	MHz	P2_MATH_CLK	—
fP2_MATH_DIV3_CLK	P2 Math accelerator div3 clock frequency	—	—	135	MHz	P2_MATH_DIV3_CLK	—
fP2_REG_INTF_CLK	P2 register interface clock frequency	—	—	135	MHz	P2_REG_INTF_CLK	—

Table continues on the next page...

Table 26. Clock frequency ranges*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fP2_SYS_CLK	P2 system clock frequency	—	—	400	MHz	P2_SYS_CLK	—
fP2_SYS_DIV2_CLK	P2 system div2 clock freqeuncy	—	—	200	MHz	P2_SYS_DIV2_CLK	—
fP2_SYS_DIV4_CLK	P2 system div4 clock frequency	—	—	100	MHz	P2_SYS_DIV4_CLK	—
fP3_AES_CLK	Reference for AES_ACCEL timers	—	—	1.01	MHz	P3_AES_CLK	—
fP3_CAN_PE_CLK	CAN protocol engine clock frequency	—	—	81	MHz	P3_CAN_PE_CLK	—
fP3_DBG_TS_CLK	Debug time stamp clock frequency	—	—	101.15	MHz	P3_DBG_TS_CLK	—
fP3_REG_INTF_CLK	P3 register interface clock frequency	—	—	133.33	MHz	P3_REG_INTF_CLK	—
fP3_SYS_CLK	P3 system clock frequency	—	—	405	MHz	P3_SYS_CLK	—
fP3_SYS_DIV2_NOC_CLK	P3 system div2 NoC clock freqeuncy	—	—	202.5	MHz	P3_SYS_DIV2_NOC_CLK	—
fP3_SYS_DIV4_CLK	P3 system div4 clock frequency	—	—	101.25	MHz	P3_SYS_DIV4_CLK	—
fCE_SYS_DIV2_CLK	FlexLLCE system div2 clock frequency	—	—	202.5	MHz	CE_SYS_DIV2_CLK	—
fCE_SYS_DIV4_CLK	FlexLLCE system div4 clock frequency	—	—	101.25	MHz	CE_SYS_DIV4_CLK	—
fP4_DSPI60_CLK	SPI_5 and SPI_6 clock frequency	—	—	120	MHz	P4_DSPI60_CLK	—
fP4_DSPI_CLK	SPI_7 clock frequency	—	—	102	MHz	P4_DSPI_CLK	—
fP4_EMIOS_LCU_CLK	eMIOS_1 clock frequency	—	—	162	MHz	P4_EMIOS_LCU_CLK	—
fP4_LIN_BAUD_CLK	LINFlexD baud clock frequency	—	—	135	MHz	P4_LIN_BAUD_CLK	—
fP4_LIN_CLK	LINFlexD clock frequency	—	—	67.5	MHz	P4_LIN_CLK	—
fP4_PSI5_125K_CLK	PSI5 189K clock frequency	—	—	4.05	MHz	P4_PSI5_125K_CLK	—
fP4_PSI5_189K_CLK	PSI5 125K clock frequency	—	—	6.048	MHz	P4_PSI5_189K_CLK	—

Table continues on the next page...

Table 26. Clock frequency ranges*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fP4_PSI5_1US_CLK	PSI5 1us clock frequency	—	—	1.01	MHz	P4_PSI5_1US_CLK	—
fP4_PSI5_S_BAUD_CLK	PSI5_S baud clock frequency	—	—	50.625	MHz	P4_PSI5_S_BAUD_CLK	—
fP4_PSI5_S_CORE_CLK	PSI5_S core clock frequency	—	—	25.3	MHz	P4_PSI5_S_CORE_CLK	—
fP4_PSI5_S_TRIG_CLK0	PSI5_S_0 trigger clock 0 frequency	—	—	1.01	MHz	P4_PSI5_S_TRIG_CLK0	—
fP4_PSI5_S_TRIG_CLK1	PSI5_S_0 trigger clock 1 frequency	—	—	1.01	MHz	P4_PSI5_S_TRIG_CLK1	—
fP4_PSI5_S_TRIG_CLK2	PSI5_S_0 trigger clock 2 frequency	—	—	1.01	MHz	P4_PSI5_S_TRIG_CLK2	—
fP4_PSI5_S_TRIG_CLK3	PSI5_S_0 trigger clock 3 frequency	—	—	1.01	MHz	P4_PSI5_S_TRIG_CLK3	—
fP4_PSI5_S_UART_CLK	PSI5_S UART clock frequency	—	—	50.625	MHz	P4_PSI5_S_UART_CLK	—
fP4_PSI5_S_UTIL_CLK	PSI5_S UTIL clock frequency	—	—	1.01	MHz	P4_PSI5_S_UTIL_CLK	—
fP4_PSI5_S_WDOG_CLK0	PSI5_S_0 watchdog clock 0 frequency	—	—	1.01	MHz	P4_PSI5_S_WDOG_CLK0	—
fP4_PSI5_S_WDOG_CLK1	PSI5_S_0 watchdog clock 1 frequency	—	—	1.01	MHz	P4_PSI5_S_WDOG_CLK1	—
fP4_PSI5_S_WDOG_CLK2	PSI5_S_0 watchdog clock 2 frequency	—	—	1.01	MHz	P4_PSI5_S_WDOG_CLK2	—
fP4_PSI5_S_WDOG_CLK3	PSI5_S_0 watchdog clock 3 frequency	—	—	1.01	MHz	P4_PSI5_S_WDOG_CLK3	—
fP4_QSPI0_1X_CLK	QuadSPI_0 1X clock frequency	—	—	202.5	MHz	P4_QSPI0_1X_CLK	—
fP4_QSPI0_2X_CLK	QuadSPI_0 2X clock frequency	—	—	405	MHz	P4_QSPI0_2X_CLK	—
fP4_QSPI1_1X_CLK	QuadSPI_1 1X clock frequency	—	—	166.25	MHz	P4_QSPI1_1X_CLK	—
fP4_QSPI1_2X_CLK	QuadSPI_1 2X clock frequency	—	—	332.5	MHz	P4_QSPI1_2X_CLK	—
fP4_REG_INTF_2X_CLK	P4 register interface 2x clock frequency	—	—	133.33	MHz	P4_REG_INTF_2X_CLK	—
fP4_REG_INTF_CLK	P4 register interface clock frequency	—	—	133.33	MHz	P4_REG_INTF_CLK	—

Table continues on the next page...

Table 26. Clock frequency ranges*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fP4_SDHC_CLK	SDHC protocol clock frequency	—	—	405	MHz	P4_SDHC_CLK	—
fP4_SDHC_IP_CLK	SDHC controller clock frequency	—	—	270	MHz	P4_SDHC_IP_CLK	—
fP4_SDHC_IP_DIV2_CLK	SDHC controller div2 clock frequency	—	—	135	MHz	P4_SDHC_IP_DIV2_CLK	—
fP4_SYS_CLK	P4 system clock frequency	—	—	400	MHz	P4_SYS_CLK	—
fP4_SYS_DIV2_CLK	P4 system div2 clock freqeuncy	—	—	200	MHz	P4_SYS_DIV2_CLK	—
fHSE_SYS_DIV2_CLK	P4 system div4 clock frequency	—	—	200	MHz	HSE_SYS_DIV2_CLK	—
fP5_AE_CLK	AE clock frequency	—	—	162	MHz	P5_AE_CLK	—
fP5_CANXL_CHI_CLK	CANXL bus clock frequency	—	—	270	MHz	P5_CANXL_CHI_CLK	—
fP5_CANXL_PE_CLK	CANXL protocol engine clock frequency	—	—	202.5	MHz	P5_CANXL_PE_CLK	—
fP5_DIPORT_CLK	diPortSD clock frequency	—	—	960	MHz	P5_DIPORT_CLK	—
fP5_DSPI_CLK	SPI_8 and SPI_9 clock frequency	—	—	102	MHz	P5_DSPI_CLK	—
fP5_LIN_BAUD_CLK	LINFlexD baud clock frequency	—	—	135	MHz	P5_LIN_BAUD_CLK	—
fP5_LIN_CLK	LINFlexD clock frequency	—	—	67.5	MHz	P5_LIN_CLK	—
fP5_REG_INTF_CLK	P5 register interface clock frequency	—	—	135	MHz	P5_REG_INTF_CLK	—
fP5_SYS_CLK	P5 system clock frequency	—	—	400	MHz	P5_SYS_CLK	—
fP5_SYS_DIV2_CLK	P5 system div2 clock freqeuncy	—	—	200	MHz	P5_SYS_DIV2_CLK	—
fP5_SYS_DIV4_CLK	P5 system div4 clock frequency	—	—	100	MHz	P5_SYS_DIV4_CLK	—
fP6_DDR_CLK	DDR controller clock frequency	—	—	400	MHz	P6_DDR_CLK	—
fP6_REG_INTF_CLK	DDR controller register interface clock frequency	—	—	135	MHz	P6_REG_INTF_CLK	—

Table continues on the next page...

Table 26. Clock frequency ranges...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fRTU0_CORE_CLK	RTU0 core clock frequency [1]	—	—	1	GHz	RTU0_CORE_CLK, TJ = 125 °C, part number 10th character = E and 13th character = V	—
fRTU0_CORE_DIV2_CLK	RTU0 core div2 clock frequency [1]	—	—	500	MHz	RTU0_CORE_DIV2_CLK, TJ = 125 °C, part number 10th character = E and 13th character = V	—
fRTU0_REG_INTF_CLK	RTU0 register interface clock frequency	—	—	135	MHz	RTU0_REG_INTF_CLK	—
fRTU1_CORE_CLK	RTU1 core clock frequency [1]	—	—	1	GHz	RTU1_CORE_CLK, TJ = 125 °C, part number 10th character = E and 13th character = V	—
fRTU1_CORE_DIV2_CLK	RTU1 core div2 clock frequency [1]	—	—	500	MHz	RTU1_CORE_DIV2_CLK, TJ = 125 °C, part number 10th character = E and 13th character = V	—
fRTU1_REG_INTF_CLK	RTU1 register interface clock frequency	—	—	135	MHz	RTU1_REG_INTF_CLK	—
fTCK	TCK clock frequency	—	—	50	MHz	TCK	—
fCLKOUT_0	CLKOUT_0 clock frequency	—	—	40.5	MHz	CLKOUT_0	—
fCLKOUT_1	CLKOUT_1 clock frequency	—	—	42	MHz	CLKOUT_1	—
fCLKOUT_2	CLKOUT_2 clock frequency	—	—	40.5	MHz	CLKOUT_2	—
fCLKOUT_3	CLKOUT_3 clock frequency	—	—	40	MHz	CLKOUT_3	—
fCLKOUT_4	CLKOUT_4 clock frequency	—	—	50	MHz	CLKOUT_4	—

1. Part numbers with a 10th character other than E have a lower maximum frequency at TJ = 150 °C or 125 °C (13th character = M or V). See the "Ordering information" section.

14.1.2 PLL

The following table gives the operating frequencies and characteristics of the PLL, and applies to all instances on the device. Actual operating frequencies for the device are constrained to the values given below.

PLL refers to the Core, Peripheral, and DDR reference PLLs on the device.

Spread spectrum clock modulation is only available on the Core PLL and DDR reference PLLs.

Table 27. PLL

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fPLL_CLKIN	PLL Input Clock Frequency [1]	—	40	—	MHz	Before PLL input divider.	—
fPLL_CLKIN_PFD	PLL Phase Detector Clock Frequency [2]	20	—	40	MHz	After PLL input divider.	—
fPLL_CORE_VCO	Core PLL VCO Frequency Range [3,4,5,6]	1300	—	2400	MHz	CORE_VCO_CLK, without center-spread SSCG enabled	—
fPLL_CORE_PHI0	Core PLL PHI0 Frequency [5,7]	40	—	1000	MHz	CORE_PLL_PHI0_CLK, without center-spread SSCG enabled, TJ = 125 °C, part number 10th character = E and 13th character = V	—
fPLL_PER_VCO	Peripheral PLL VCO Frequency Range	1300	—	2400	MHz	PERIPH_PLL_VCO_CLK	—
fPLL_PER_PHI0	Peripheral PLL PHI0 Frequency	40	—	1620	MHz	PERIPH_PLL_PHI0_CLK	—
fPLL_PER_PHI1	Peripheral PLL PHI1 Frequency	40	—	102	MHz	PERIPH_PLL_PHI1_CLK	—
fPLL_PER_PHI2	Peripheral PLL PHI2 Frequency	40	—	120	MHz	PERIPH_PLL_PHI2_CLK	—
fPLL_PER_PHI3	Peripheral PLL PHI3 Frequency	40	—	270	MHz	PERIPH_PLL_PHI3_CLK	—
fPLL_PER_PHI4	Peripheral PLL PHI4 frequency	40	—	202.5	MHz	PERIPH_PLL_PHI4_CLK	—
fPLL_PER_PHI5	Peripheral PLL PHI5 Frequency	40	—	162	MHz	PERIPH_PLL_PHI5_CLK	—
fPLL_PER_PHI6	Peripheral PLL PHI6 frequency	40	—	810	MHz	PERIPH_PLL_PHI6_CLK	—
fPLL_DDR_VCO	DDR PLL VCO Frequency Range [3,5]	1300	—	1620	MHz	DDR_PLL_VCO_CLK, without center-spread SSCG enabled	—
fPLL_DDR_PHI0	DDR PLL PHI0 Frequency [8]	266	—	266	MHz	DDR_PLL_PHI0_CLK (1066 MT/s). No SSCG support in this mode.	—
fPLL_DDR_PHI0	DDR PLL PHI0 Frequency [8]	333	—	333	MHz	DDR_PLL_PHI0_CLK (1333 MT/s). No SSCG support in this mode.	—

Table continues on the next page...

Table 27. PLL*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fPLL_DDR_PHI0	DDR PLL PHI0 Frequency [5,8]	400	—	400	MHz	DDR_PLL_PHI0_CLK (1600 MT/s)	—
fPLL_DDR_PHI0	DDR PLL PHI0 Frequency [5,8]	405	—	405	MHz	DDR_PLL_PHI0_CLK (1600 MT/s), FLASH only, not applicable for DRAM.	—
tLOCK	PLL Lock Time	—	—	100	us	—	—
PER_jitter	PLL Period Jitter [9,10,11,12]	-23	—	23	ps	fPLL_CLKIN = 40MHz, fVCO = 2GHz, 6-sigma, SSCG & Frac mode disabled	—
LT_jitter	PLL Long Term Jitter [9,10,13]	-120	—	120	ps	Saturated, 6-sigma	—
fPLL_MOD	Spread Spectrum Clock Modulation Frequency	30	—	64	KHz	—	—

1. This refers to spec number 1 which is shown in the figure in Aurora port specifications
2. This specification is PLL input reference clock frequency after pre-divider.
3. Same min frequency value applies for center-spread SSCG enabled as provided for center-spread SSCG disabled.
4. The frequencies are the nominal frequencies (i.e., what the PLL's VCO is configured to).
5. The max frequency in case of center-spread SSCG enabled for a modulation depth can be calculated as: Max frequency(with center-spread SSCG disabled) – (Modulation Depth(in %)/(2*100))* Max frequency (with center-spread SSCG disabled). For details, see section “Frequency modulation programming” in reference manual.
6. Duty cycle of the PLL clock when output on an external pin is given in the I/O pad specifications.
7. Part numbers with a 10th character other than E have a lower maximum frequency at TJ = 150 °C or 125 °C (13th character = M or V). See the "Ordering information" section.
8. The DDR PHY internally multiplies the PLL_DDR_PHI0 by factor of two.
9. Jitter is dependent on supply noise. Specified jitter values are valid for the FXOSC reference clock input only - not valid for FIRC reference clock input.
10. Jitter value does not apply when a PLL clock is output on an external pin. In this case, the rise and fall time variations in the I/O pad are orders of magnitude more than the PLL and SoC mux jitter contributions.
11. Jitter is dependent on the period of the PLL output clock, and the division ratio of the clock at the destination module.
12. For chip clocks that are further divided down from the PLL output clock, the jitter is multiplied by a factor of SQRT(N), where N is the ratio of the PLL output clock and destination clock periods.
13. This specification is valid when all clock sources are stable.

14.1.3 DFS

The following table specifies the output frequency ranges and characteristics of the Digital Frequency Synthesizer (DFS).

Table 28. DFS

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fDFS_CLKIN	DFS Input Clock Frequency	1300	—	2400	MHz	—	—

Table continues on the next page...

Table 28. DFS...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fDFS_CORE_CLK0	Core DFS Output Clock 0 Frequency [1]	40	—	1000	MHz	CORE_DFS0_CLK, TJ = 125 °C, part number 10th character = E and 13th character = V	—
fDFS_CORE_CLK1	Core DFS Output Clock 1 Frequency	40	—	405	MHz	CORE_DFS1_CLK	—
fDFS_CORE_CLK2	Core DFS Output Clock 2 Frequency	40	—	405	MHz	CORE_DFS2_CLK	—
fDFS_CORE_CLK3	Core DFS Output Clock 3 Frequency	40	—	503	MHz	CORE_DFS3_CLK	—
fDFS_CORE_CLK4	Core DFS Output Clock 4 Frequency	40	—	400	MHz	CORE_DFS4_CLK	—
fDFS_CORE_CLK5	Core DFS Output Clock 5 Frequency	40	—	405	MHz	CORE_DFS5_CLK	—
fDFS_PER_CLK0	Peripheral DFS Output Clock 0 Frequency	40	—	800	MHz	PERIPH_DFS0_CLK	—
fDFS_PER_CLK1	Peripheral DFS Output Clock 1 Frequency	40	—	960	MHz	PERIPH_DFS1_CLK	—
fDFS_PER_CLK2	Peripheral DFS Output Clock 2 Frequency	40	—	664	MHz	PERIPH_DFS2_CLK	—
fDFS_PER_CLK3	Peripheral DFS Output Clock 3 Frequency	40	—	503	MHz	PERIPH_DFS3_CLK	—
fDFS_PER_CLK4	Peripheral DFS Output Clock 4 Frequency	40	—	503	MHz	PERIPH_DFS4_CLK	—
fDFS_PER_CLK5	Peripheral DFS Output Clock 5 Frequency	40	—	330	MHz	PERIPH_DFS5_CLK	—
PER_jitter	DFS Period Jitter [2,3]	-30	—	30	ps	Even MFN	—
PER_jitter	DFS Period Jitter [2,3]	-45	—	45	ps	fDFS_CLKIN = 2000 MHz, Odd MFN	—
PER_Jitter	DFS Period Jitter [2,3]	-30	—	30	ps	fDFS_CLKIN = 2400 MHz, Odd MFN	—
PER_jitter	DFS Period Jitter [2,3]	-60	—	60	ps	fDFS_CLKIN = 1300 MHz, Odd MFN	—

1. Part numbers with a 10th character other than E have a lower maximum frequency at TJ = 150 °C or 125 °C (13th character = M or V). See the "Ordering information" section.

2. For SoC clocks that are further divided down from the DFS output clock, the jitter is multiplied by a factor of SQRT(N), where N is the ratio of the DFS output clock and destination clock periods.
3. Jitter value does not apply when the DFS clock is output on an external pin. In this case, the rise and fall time variations in the I/O pad are orders of magnitude more than the DFS and SoC mux jitter contributions.

Peripheral DFS output clock min jitter=Min(PER_jitter(PLL))*(sqrt(N))+Min(PER_jitter(DFS)). Peripheral DFS output clock max jitter=Max(PER_jitter(PLL))*(sqrt(N)) +Max(PER_jitter(DFS)). Where N is the DFS division factor. All jitter numbers are in ps.

14.1.4 FXOSC

Table 29. FXOSC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fXTAL	Input Frequency Range [1,2]	20	—	40	MHz	Crystal mode	—
TCST	Crystal Startup Time	—	—	2	ms	Crystal mode - time to stable duty cycle when EOCV is set to 1 ms period	—
fBYP_SE	FXOSC Bypass Frequency	20	—	40	MHz	single-ended bypass mode	—
VIH_EXTAL	EXTAL Input High Level [3]	VCM_SE + 0.3	—	VDD_HV_FXOSC_PLL	V	Single-ended bypass mode	—
VIL_EXTAL	EXTAL Input Low Level [3]	0	—	VCM_SE - 0.3	V	Single-ended bypass mode	—
ΔfXTAL_CLK	Input Clock Duty Cycle	47.5	—	52.5	%	Bypass mode	—
CLOAD	XTAL/EXTAL pin load capacitance [4]	—	8	—	pF	Crystal mode	—
CS_XTAL	XTAL/EXTAL pin on-chip stray capacitance [4]	—	—	3	pF	—	—
VCM_SE	Common Mode Voltage for Single ended Bypass	—	VDD_HV_FXOSC_PLL / 2	—	mV	—	—
Leakage_injection	EXTAL injection current	-50	—	100	nA	Mean current flowing into EXTAL in crystal mode	—
Leakage_extal	External Leakage on EXTAL Pin	-20	—	20	nA	Bypass mode, 0.5V	—
EXTAL_AMP	EXTAL_amplitude (pk-pk)	300	—	900	mV	Crystal mode	—
LT_Jitter	Long term jitter	-120	—	120	ps	gm_sel=1111 with 40MHz crystal (NX5032GA and NX3225GA)	—

1. All specifications only valid for this frequency range if the correct FXOSC transconductance setting is used.
2. Recommended crystal frequencies are 20MHz, 24MHz, 25MHz and 40MHz.
3. The input clock signal should be symmetric around common mode voltage.
4. Account for on-chip stray capacitance (CS_XTAL) and PCB capacitance in the total XTAL/EXTAL pin load capacitance. CS_XTAL don't include miller capacitance.

In crystal mode NX5032GA crystal at 20 MHz has a load cap of 8 pF and configure gm_sel[3:0]=4'b0100 and NX3225GA crystal has a load cap of 8 pF and configure gm_sel[3:0]=4'b100.

In crystal mode NX5032GA crystal at 24 MHz has a load cap of 8 pF and configure gm_sel[3:0]=4'b0101 and NX3225GA has a load cap of 8 pF and configure gm_sel[3:0]=4'b0110.

In crystal mode NX5032GA and NX3225GA crystal at 40 MHz (ALC enable) has a load cap of 8 pF and configure gm_sel[3:0]=4'b1111.

In ALC disable mode the minimum crystal drive level should be greater than 500uW.

Duty cycle of the FXOSC clock when output on either the single-ended or LVDS CLKOUT pins is given in the I/O pad specifications.

RGMII specifications require clock source to have tolerance of +/- 50ppm. When using this mode, the crystal selected for system clock (FXOSC) should adhere to this specification.

14.1.5 FIRC

Table 30. FIRC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fFIRC	FIRC Target Frequency	—	48	—	MHz	—	—
ðfVAR	FIRC Frequency Variation [1]	-5	—	5	%	Trimmed	—
TSTART	Startup Time	—	10	20	us	After valid supply level reached	—

1. ðfVAR defines how much the output frequency can shift over the specified temperature and voltage ranges of the device after initial factory trim.

14.1.6 SIRC

Table 31. SIRC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSIRC	SIRC Target Frequency Trimmed	—	32	—	KHz	Trimmed	—
PTA	SIRC Trimming Resolution [1]	-1	—	1	%	Trimmed 32KHz, 25C, 0.8V Core	—
ðfVAR	SIRC Frequency Variation [2]	-5	—	5	%	Frequency variation across voltage and temperature range after trimming.	—
TSTART	SIRC Startup Time	—	—	50	us	—	—

1. PTA defines how close the output frequency is to target after the initial factory trim.

2. ðfVAR defines how much the output frequency can shift over the specified temperature and voltage ranges of the device.

14.1.7 LFAST PLL

Table 32. LFAST PLL

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fPLL_CLKIN	PLL Input Clock Frequency (after pre-divider)	10	—	26	MHz	—	—
DCREF	PLL Input Reference Clock Duty Cycle	45	—	55	%	—	—
REF_PER_Jitter	Input Reference Clock Period Jitter	-100	—	100	ps	—	—
TIE	Input Clock Time Interval Error	—	—	500	ps	—	—
fLFAST_PLL_VCO_CLK	PLL VCO Frequency Range	624	—	840	MHz	624 MHz with fRF_REF = 26MHz, fLFAST_CLK=fLFAST_PLL_VCO_CLK/2	—
fLFAST_CLK	PLL Output Clock Frequency Range	312	—	420	MHz	—	—
tLOCK	PLL Lock Time [1]	—	—	40	us	—	—
PER_jitter	PLL Period Jitter (RMS) [2]	—	—	40	ps	fRF_REF = 26MHz	—
RJ	PLL Long Term Random Jitter [2]	—	84	—	ps	VCO clock measured over 100us acquisition period with a transmit load of 100ohm.	—
DJ	PLL Long Term Deterministic Jitter [2]	—	80	—	ps	VCO clock measured over 100us acquisition period with a transmit load of 100ohm.	—
TOT_jitter	Total Jitter [2]	—	1.09	1.31	ns	BER = 10e-9	—

1. 40us max tLOCK assumes fPLL_CLKIN = 26MHz and default compare_clk_cycle value of 1040. Slower fPLL_CLKIN frequencies will increase tLOCK. tLOCK = (1/fPLL_CLKIN) * compare_clock_cycles, where register bits PLLCR[PLCKCW] select compare_clock_cycles from values:00-1040 (default), 01-520, 10-320, 11-200
2. Specification not valid when the LFAST PLL input clock is FIRC_CLK.

14.1.8 AE IRC

Table 33. AE IRC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fFIRC	IRC target frequency	—	16	—	MHz	—	—

Table continues on the next page...

Table 33. AE IRC...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
ðfVAR	IRC frequency variation	-4	—	4	%	Trimmed, no temperature compensation	—
TSTART	Startup Time	—	—	5	us	After valid supply level reached	—

14.2 Timer Modules

14.2.1 eMIOS

Table 34. eMIOS

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tMIPW	eMIOS input pulse width [1]	4	—	—	tPER_CLK	—	—
tMOPW	eMIOS output pulse width [1,2]	1	—	—	tPER_CLK	—	—

1. tPER_CLK is the period of the peripheral clock (PER_CLK) on the device.
2. Actual output pulse may be larger when considering a slow transitioning output.

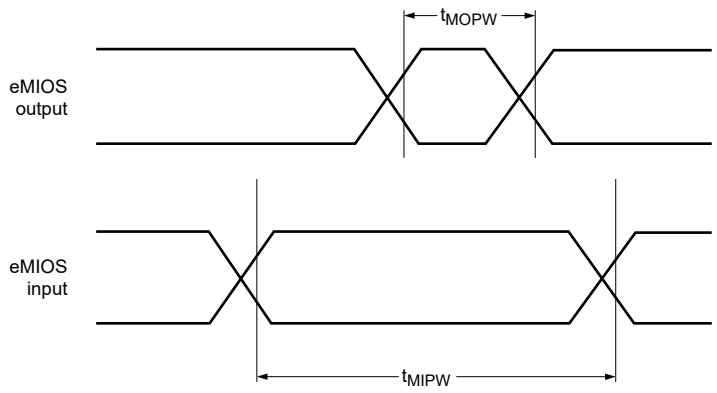


Figure 25. EMIOS Timing

14.3 Communication Modules

14.3.1 I3C

On this chip, the I3C module supports features and functionality of only the I2C protocol. It does not support additional features and functionality of the I3C protocol.

14.3.1.1 I3C timing when communicating with Legacy I2C devices

Table 35. I3C timing when communicating with Legacy I2C devices

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCL	SCL clock frequency	0	—	0.4	MHz	400 kHz/FM	—
fSCL	SCL clock frequency	0	—	1	MHz	1 MHz/FM+	—
tSU_STA	Setup time for repeated START	600	—	—	ns	400 kHz/FM	—
tSU_STA	Setup time for repeated START	260	—	—	ns	1 MHz/FM+	—
tHD_STA	Hold time for repeated START	600	—	—	ns	400 kHz/FM	—
tHD_STA	Hold time for repeated START	260	—	—	ns	1 MHz/FM+	—
tLOW	SCL clock low period	1300	—	—	ns	400 kHz/FM	—
tLOW	SCL clock low period	500	—	—	ns	1 MHz/FM+	—
tDIG_L	SCL clock low period	tLOW+trCL	—	—	ns	400 kHz/FM	—
tDIG_L	SCL clock low period	tLOW+trCL	—	—	ns	1 MHz/FM+	—
tHIGH	SCL clock high period	600	—	—	ns	400 kHz/FM	—
tHIGH	SCL clock high period	260	—	—	ns	1 MHz/FM+	—
tDIG_H	SCL clock high period	tHIGH+trCL	—	—	ns	400 kHz/FM	—
tDIG_H	SCL clock high period	tHIGH+trCL	—	—	ns	1 MHz/FM+	—
tSU_DAT	Data setup time	100	—	—	ns	400 kHz/FM	—
tSU_DAT	Data setup time	50	—	—	ns	1 MHz/FM+	—
tHD_DAT	Data hold time	100	—	900	ns	400 kHz/FM	—
tHD_DAT	Data hold time	50	—	450	ns	1 MHz/FM+	—
trCL	SCL signal rise time [1]	—	—	300	ns	400 kHz/FM	—
trCL	SCL signal rise time	—	—	120	ns	1 MHz/FM+	—
tfCL	SCL signal fall time [1]	—	—	300	ns	400 kHz/FM	—
tfCL	SCL signal fall time [1]	—	—	120	ns	1 MHz/FM+	—
trDA	SDA signal rise time [1]	—	—	300	ns	400 kHz/FM	—

Table continues on the next page...

Table 35. I3C timing when communicating with Legacy I2C devices...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
trDA	SDA signal rise time	—	—	120	ns	1 MHz/FM+	—
tfDA	SDA signal fall time [1]	—	—	300	ns	400 kHz/FM	—
tfDA	SDA signal fall time [1]	—	—	120	ns	1 MHz/FM+	—
tSU_STO	Setup time for STOP	600	—	—	ns	400 kHz/FM	—
tSU_STO	Setup time for STOP	260	—	—	ns	1 MHz/FM+	—
tBUF	Bus free time between a stop and a start	1.3	—	—	us	400 kHz/FM	—
tBUF	Bus free time between a stop and a start	0.5	—	—	us	1 MHz/FM+	—

1. Minimum time depends on bus loading. SRE of 111b should be used.

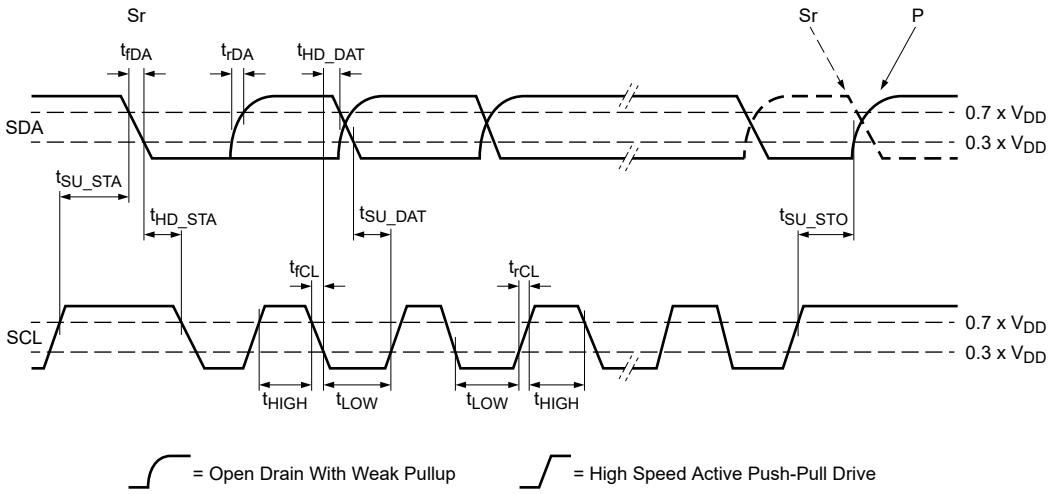


Figure 26. Legacy mode timing

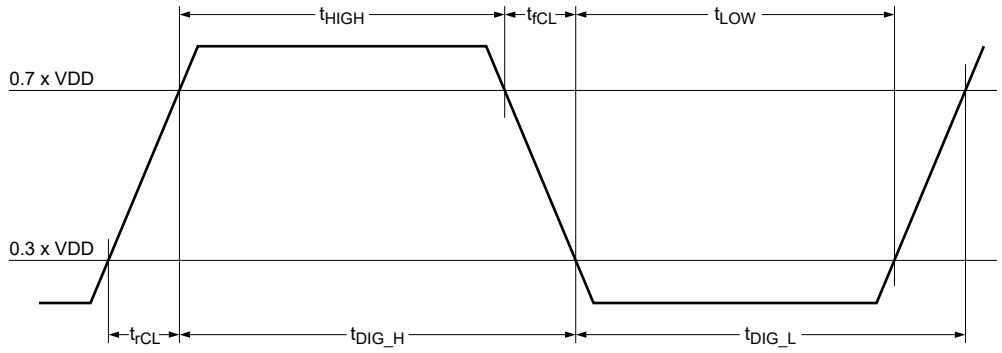


Figure 27. tDIG_H and tDIG_L

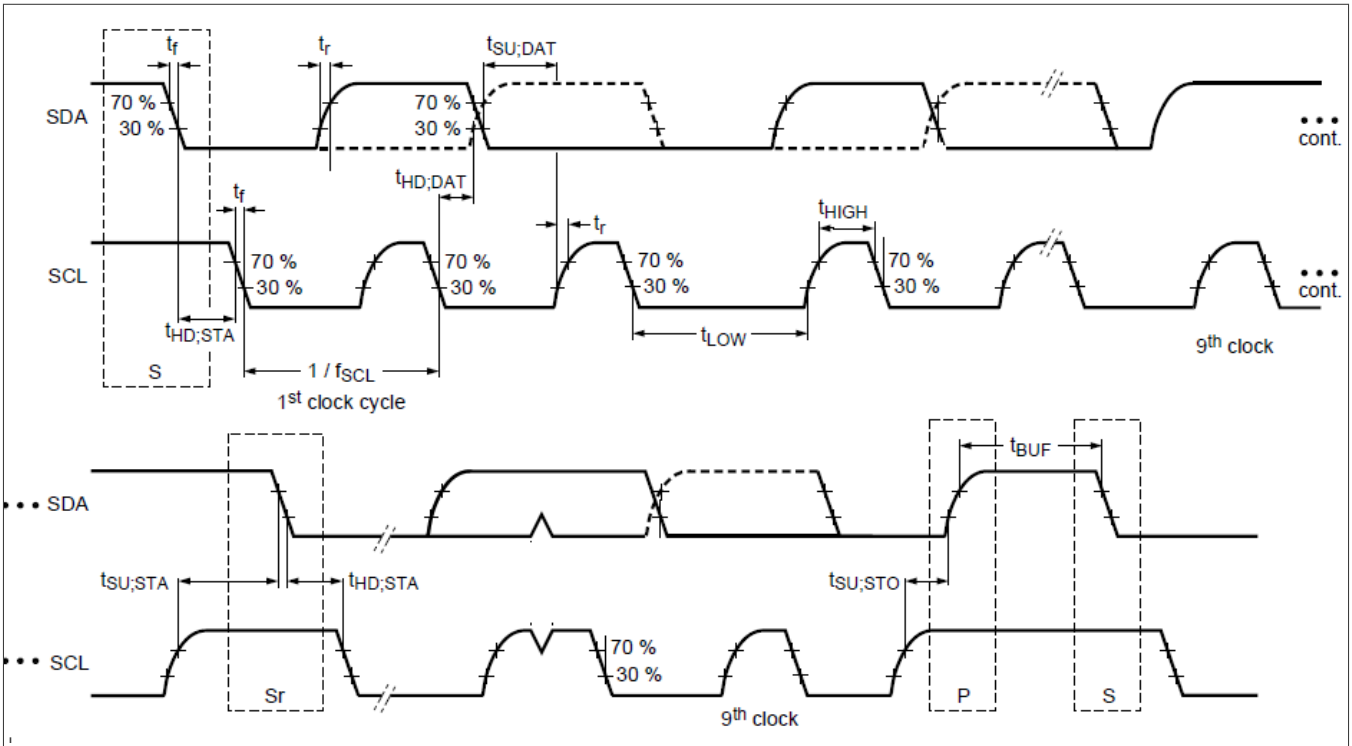


Figure 28. Definition of timing for F/S mode devices on the I2C bus

14.3.2 LPI2C

LPI2C is a low-power Inter-Integrated Circuit (I2C) module that supports an efficient interface to an I2C bus as a controller and/or as a target.

Table 36. LPI2C

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCL	SCL clock frequency: Standard mode (Sm) [1]	0	—	100	kHz	—	—

Table continues on the next page...

Table 36. LPI2C...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCL	SCL clock frequency: Fast mode (Fm) [1]	0	—	400	kHz	—	—
fSCL	SCL clock frequency: Fast mode Plus (Fm++) [1]	0	—	1000	kHz	—	—
fSCL	SCL clock frequency: Ultra Fast mode (Ufm) [1]	0	—	5000	kHz	—	—
tSU_STA	Setup time for repeated START	4.7	—	—	us	100kHz/SM	—
tSU_STA	Setup time for repeated START	600	—	—	ns	400kHz/FM	—
tSU_STA	Setup time for repeated START	260	—	—	ns	1MHz/FM+	—
tSU_STA	Setup time for repeated START	50	—	—	ns	5MHz/UFM	—
tHD_STA	Hold time for repeated START	400	—	—	ns	100kHz/SM	—
tHD_STA	Hold time for repeated START	600	—	—	ns	400kHz/FM	—
tHD_STA	Hold time for repeated START	260	—	—	ns	1MHz/FM+	—
tHD_STA	Hold time for repeated START	80	—	—	ns	5MHz/UFM	—
tLOW	SCL clock low period	4.7	—	—	us	100kHz/SM	—
tLOW	SCL clock low period	1300	—	—	ns	400kHz/FM	—
tLOW	SCL clock low period	500	—	—	ns	1MHz/FM+	—
tLOW	SCL clock low period	50	—	—	ns	5MHz/UFM	—
tDIG_L	SCL clock low period	tLOW+trCL	—	—	ns	100kHz/SM	—
tDIG_L	SCL clock low period	tLOW+trCL	—	—	ns	400kHz/FM	—
tDIG_L	SCL clock low period	tLOW+trCL	—	—	ns	1MHz/FM+	—
tDIG_L	SCL clock low period	tLOW+trCL	—	—	ns	5MHz/UFM	—

Table continues on the next page...

Table 36. LPI2C*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tHIGH	SCL clock high period	4	—	—	us	100kHz/SM	—
tHIGH	SCL clock high period	600	—	—	ns	400kHz/FM	—
tHIGH	SCL clock high period	260	—	—	ns	1MHz/FM+	—
tHIGH	SCL clock high period	50	—	—	ns	5MHz/UFM	—
tDIG_H	SCL clock high period	tHIGH+trCL	—	—	ns	100kHz/SM	—
tDIG_H	SCL clock high period	tHIGH+trCL	—	—	ns	400kHz/FM	—
tDIG_H	SCL clock high period	tHIGH+trCL	—	—	ns	1MHz/FM+	—
tDIG_H	SCL clock high period	tHIGH+trCL	—	—	ns	5MHz/UFM	—
tSU_DAT	Data setup time	250	—	—	ns	100kHz/SM	—
tSU_DAT	Data setup time	100	—	—	ns	400kHz/FM	—
tSU_DAT	Data setup time	50	—	—	ns	1MHz/FM+	—
tSU_DAT	Data setup time	30	—	—	ns	5MHz/UFM	—
tHD_DAT	Data hold time	0	—	—	us	100kHz/SM	—
tHD_DAT	Data hold time	0	—	—	ns	400kHz/FM	—
tHD_DAT	Data hold time	0	—	—	ns	1MHz/FM+	—
tHD_DAT	Data hold time	10	—	—	ns	5MHz/UFM	—
trCL	SCL signal rise time	—	—	1	us	100kHz/SM	—
trCL	SCL signal rise time [2]	—	—	300	ns	400kHz/FM	—
trCL	SCL signal rise time	—	—	120	ns	1MHz/FM+	—
trCL	SCL signal rise time	—	—	50	ns	5MHz/UFM	—
tfCL	SCL signal fall time	—	—	300	ns	100kHz/SM	—
tfCL	SCL signal fall time [2]	—	—	300	ns	400kHz/FM	—
tfCL	SCL signal fall time [2]	—	—	120	ns	1MHz/FM+	—
tfCL	SCL signal fall time	—	—	50	ns	5MHz/UFM	—
trDA	SDA signal rise time	—	—	1	us	100kHz/SM	—

Table continues on the next page...

Table 36. LPI2C...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
trDA	SDA signal rise time [2]	—	—	300	ns	400kHz/FM	—
trDA	SDA signal rise time	—	—	120	ns	1MHz/FM+	—
trDA	SDA signal rise time	—	—	50	ns	5MHz/UFM	—
tfDA	SDA signal fall time	—	—	300	ns	100kHz/SM	—
tfDA	SDA signal fall time [2]	—	—	300	ns	400kHz/FM	—
tfDA	SDA signal fall time [2]	—	—	120	ns	1MHz/FM+	—
tfDA	SDA signal fall time	—	—	50	ns	5MHz/UFM	—
tSU_STO	Setup time for STOP	4	—	—	us	100kHz/SM	—
tSU_STO	Setup time for STOP	600	—	—	ns	400kHz/FM	—
tSU_STO	Setup time for STOP	260	—	—	ns	1MHz/FM+	—
tSU_STO	Setup time for STOP	50	—	—	ns	5MHz/UFM	—
tBUF	Bus free time between a stop and a start	4.7	—	—	us	100kHz/SM	—
tBUF	Bus free time between a stop and a start	1.3	—	—	us	400kHz/FM	—
tBUF	Bus free time between a stop and a start	0.5	—	—	us	1MHz/FM+	—
tBUF	Bus free time between a stop and a start	80	—	—	ns	5MHz/UFM	—

1. For more details, see UM10204 I2C-bus specification and user manual.
2. Minimum time depends on bus loading. SRE of 111b should be used.

14.3.3 SPI

SRE[2:0]=101 is the required drive setting to meet the timing.

Table 37. SPI

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tSCK	SPI cycle time [1,2]	40	—	10000	ns	Master, MTFE=0	1
tSCK	SPI cycle time [2]	25	—	10000	ns	Master, MTFE=1	1
tSCK	SPI cycle time [2,3]	16.67	—	10000	ns	Slave Receive Mode	1

Table continues on the next page...

Table 37. SPI*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tSCK	SPI cycle time [2]	40	—	10000	ns	Slave Transmit Mode	1
tCSC	PCS to SCK delay [4]	20	—	10000	ns	—	2
tASC	After SCK delay [5]	20	—	10000	ns	—	3
tSDC	SCK duty cycle	40	—	60	%	—	4
tA	Slave access time	—	—	40	ns	SS active to SOUT valid	5
tDIS	Slave SOUT disable time	—	—	15	ns	SS inactive to SOUT hi-z or invalid	6
tPCSC	PCSx to PCSS time	13	—	—	ns	—	7
tPASC	PCSS to PCSx time	13	—	—	ns	—	8
tSUI	Input data setup time [6,7]	15	—	—	ns	Master, MTFE=0	9
tSUI	Input data setup time [7,8]	15 - N * ipg_clk_dspi_period	—	—	ns	Master, MTFE=1, CPHA=0, SMPL_PTR = 1	9
tSUI	Input data setup time [7]	15	—	—	ns	Master, MTFE=1, CPHA=1, SMPL_PTR = 1	9
tSUI	Input data setup time [7]	2	—	—	ns	Slave Receive Mode	9
tHI	Input data hold time [7]	0	—	—	ns	Master, MTFE=0	10
tHI	Input data hold time [7]	0 + N * ipg_clk_dspi_period	—	—	ns	Master, MTFE=1, CPHA=0, SMPL_PTR = 1	10
tHI	Input data hold time [7]	0	—	—	ns	Master, MTFE=1, CPHA=1, SMPL_PTR = 1	10
tHI	Input data hold time [7]	4	—	—	ns	Slave Receive Mode	10
tSUO	Output data valid time (after SCK edge) [9]	—	—	5	ns	Master, MTFE=0 max CLOAD=25pF, max pad drive setting	11
tSUO	Output data valid time (after SCK edge) [9]	—	—	5 + ipg_clk_dspi_period	ns	Master, MTFE=1, CPHA=0 max CLOAD=25pF, max pad drive setting	11

Table continues on the next page...

Table 37. SPI*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tSUO	Output data valid time (after SCK edge) [9]	—	—	5	ns	Master, MTFE=1, CPHA=1 max CLOAD=25pF, max pad drive setting	11
tSUO	Output data valid time (after SCK edge) [6,9]	—	—	16	ns	Slave Transmit Mode	11
tHO	Output data hold time [9]	-2	—	—	ns	Master, MTFE=0 max CLOAD=25pF, max pad drive setting	12
tHO	Output data hold time [9]	-2 + ipg_clk_dspi_period	—	—	ns	Master, MTFE=1, CPHA=0 max CLOAD=25pF, max pad drive setting	12
tHO	Output data hold time [9]	-2	—	—	ns	Master, MTFE=1, CPHA=1 max CLOAD=25pF, max pad drive setting	12
tHO	Output data hold time [9]	3	—	—	ns	Slave Transmit Mode	12

1. SMPL_PTR should be set to 1. For SPI_CTARn[BR] - 'Baud Rate Scaler' configuration is >= 3
2. The maximum SPI baud rate that is achievable in a dedicated master-slave connection depends on several parameters that are independent of the SPI module clocking capabilities (e.g. capacitive load of the signal lines, SPI slave clock-to-data delay, pad slew rate, etc.). The maximum achievable SPI baud rate needs to be evaluated in a corresponding SPI master-slave setup.
3. Slave Receive Mode can operate at a maximum frequency of 60 MHz. In this mode, the DSPI can receive data on SIN, but no valid data is transmitted on SOUT.
4. This value of 20 ns is with the configuration prescaler values: SPI_CTARn[PCSSCK] - "PCS to SCK Delay Prescaler" configuration is "3" (01h) and SPI_CTARn[CSSCK] - "PCS to SCK Delay Scaler" configuration is "2" (0000h)
5. This value of 20 ns is with the configuration prescaler values: SPI_CTARn[PASC] - "After SCK Delay Prescaler" configuration is "3" (01h) and SPI_CTARn[ASC] - "After SCK Delay Scaler" configuration is "2" (0000h)
6. For the case of both master and slave being NXP S32x devices, frequency of operation will be reduced to [1000 /2* {tSUI_master + tSUO_slave + PCB delay}] in ns.
7. Input timing assumes an input signal slew rate of 2ns (20%/80%).
8. N is number of protocol clock cycles where the master samples SIN in MTFE mode after SCK edge.
9. Output timing valid for maximum external load CL = 25 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).

Note that SPI operation should be done by selecting same pad type. A mix of 33 and 3318 pads for the same SPI is not supported.

Slave mode timing values given below are applicable when device is in MTFE=0.

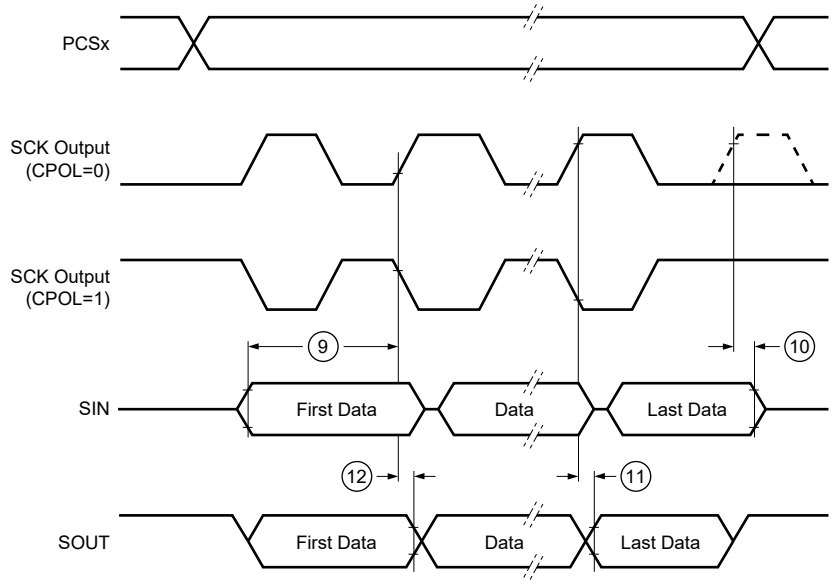


Figure 29. SPI Modified Transfer Format Timing - Master, CPHA = 1, MTFE=1

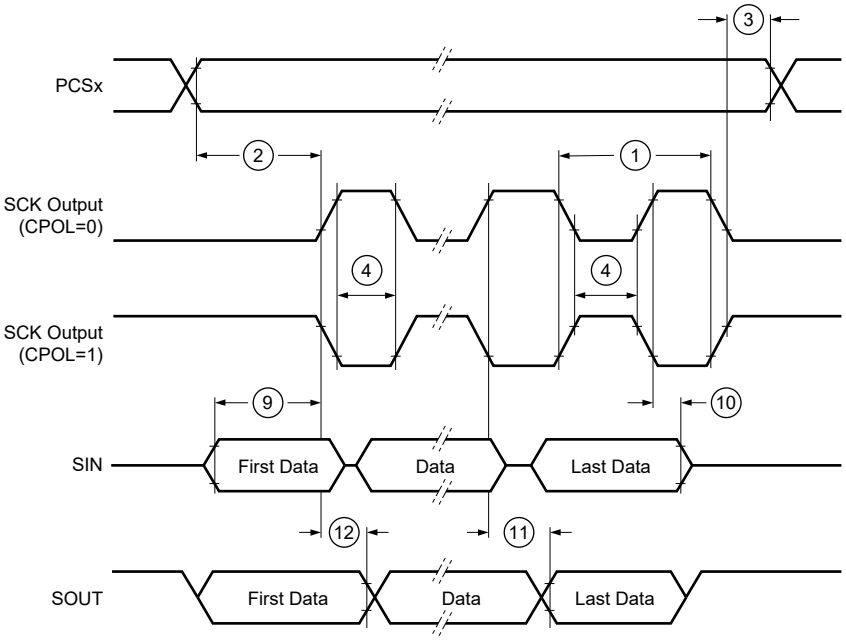


Figure 30. SPI Modified Transfer Format Timing - Master, CPHA = 0, MTFE=1

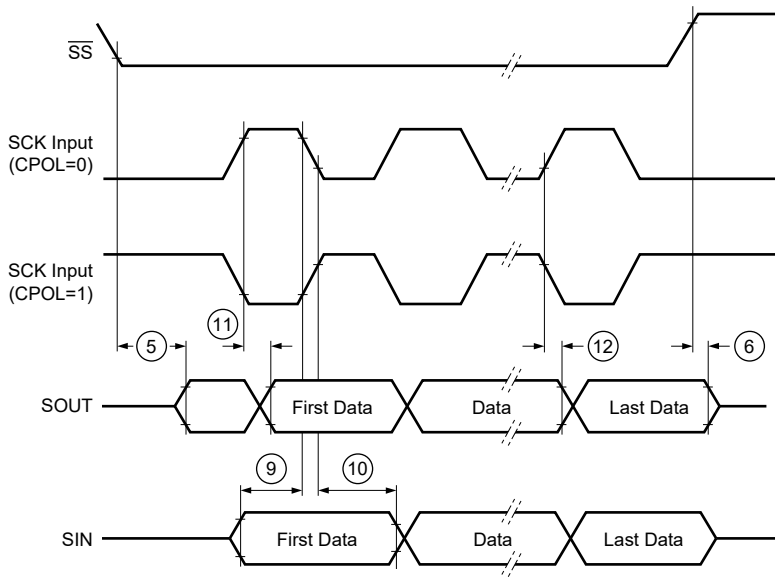


Figure 31. SPI Classic Timing - Slave CPHA = 1, MTFE=0

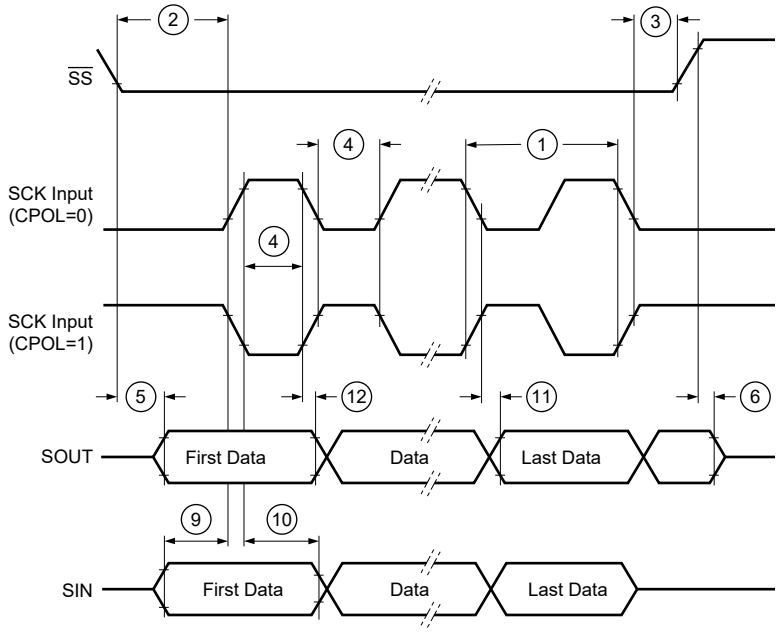


Figure 32. SPI Classic Timing - Slave CPHA = 0, MTFE=0

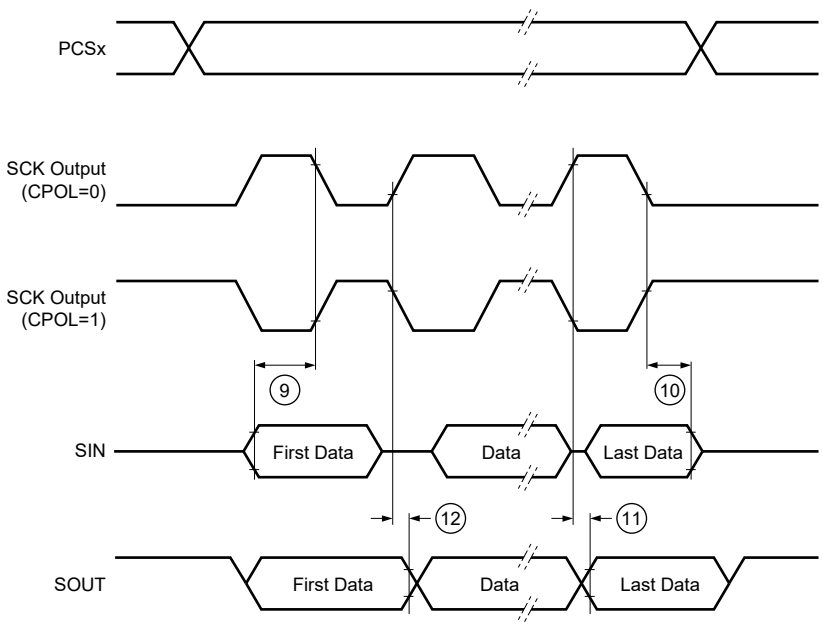


Figure 33. SPI Classic Timing - Master, CPHA = 1, MTFE=0

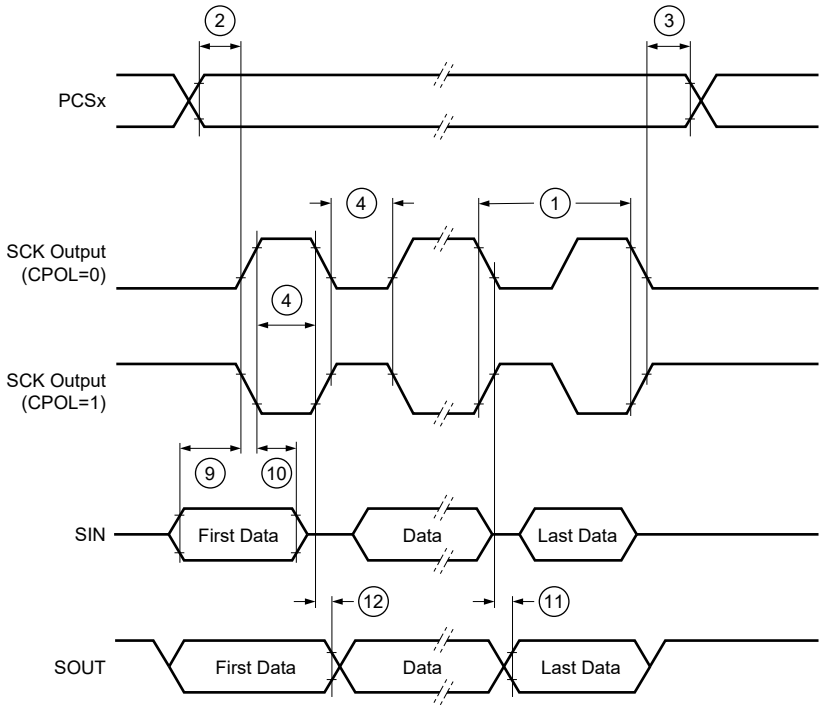


Figure 34. SPI Classic Timing - Master, CPHA = 0, MTFE=0

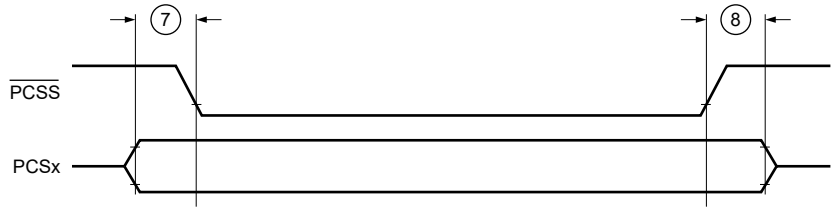


Figure 35. SPI PCS Strobe (PCSS) Timing

14.3.4 Microsecond channel (MSC)

Table 38. Microsecond channel (MSC)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tSCK	MSC cycle time	20	—	—	ns	—	—
tCSV	PCS valid after SCK [1]	—	—	5	ns	—	—
tCSH	PCS hold after SCK [1]	-4	—	—	ns	—	—
tSUO	Output data valid time (after SCK edge)	—	—	5	ns	—	—
tHO	Output data hold time	-4	—	—	ns	—	—
t1	SCK duty cycle deviation	-1	—	1	ns	—	—
t2	SOUT/SCK Rise time [2]	0.4	—	7	ns	ZL=100R, CL<50	—
t2	SOUT/SCK Rise time [2]	0.4	—	3.5	ns	ZL=100R, CL<25	—
t3	SOUT/SCK Fall time [2]	0.4	—	7	ns	ZL=100R, CL<50	—
t3	SOUT/SCK Fall time [2]	0.4	—	3.5	ns	ZL=100R, CL<25	—

1. With TSB mode or Continuous SCK clock mode selected, PCS and SCK are driven by the same edge of SPI_CLKn. This timing value is due to pad delays and signal propagation delays.
2. Measured at 20% to 80% of output voltage with tSCK=50Mhz.

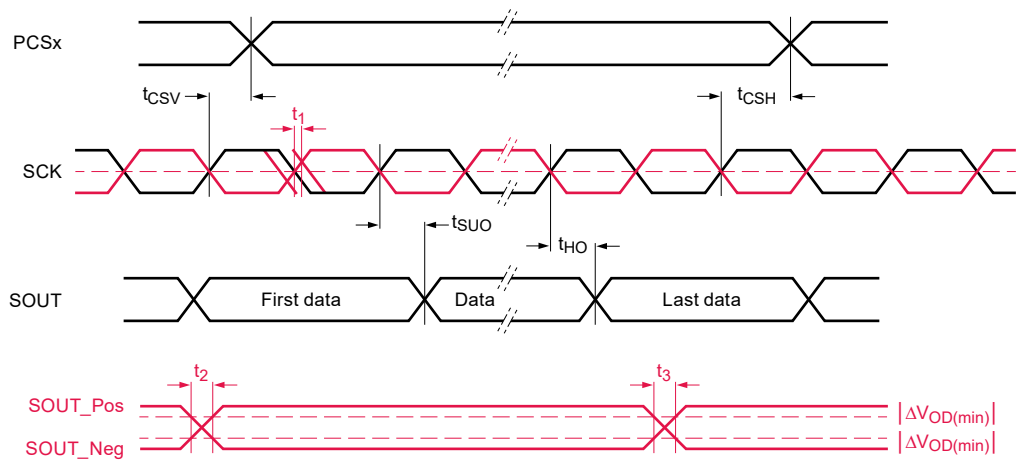


Figure 36. MSC master timing, output only

14.3.5 LIN

SRE[2:0]=110 is the required drive setting to meet the timing.

Table 39. LIN

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
RATE	Bit Rate	—	—	33	Mbps	UART mode	—
RATE	Bit Rate	4.8	—	20	Kbps	LIN mode	—

14.3.6 FlexRay

14.3.6.1 FlexRay - TxEN

Table 40. FlexRay - TxEN

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
dCCTxENRISE25	Rise time of TxEN signal at CC [1]	—	—	9	ns	TxEN load = 25pF max, SRE[2:0] = 100 (1.8V/3.3V GPIO), SRE[2:0] = 110 (3.3V GPIO)	—
dCCTxENFALL25	Fall time of TxEN signal at CC [1]	—	—	9	ns	TxEN load = 25pF max, SRE[2:0] = 100 (1.8V/3.3V GPIO), SRE[2:0] = 110 (3.3V GPIO)	—
dCCTxEN01	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge [1]	—	—	25	ns	TxEN load = 25pF max, SRE[2:0] = 100 (1.8V/3.3V GPIO), SRE[2:0] = 110 (3.3V GPIO)	—

Table continues on the next page...

Table 40. FlexRay - TxEN...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
dCCTxEN10	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge [1]	—	—	25	ns	TxEN load = 25pF max, SRE[2:0] = 100 (1.8V/3.3V GPIO), SRE[2:0] = 110 (3.3V GPIO)	—

1. Output timing valid for maximum external load CL = 25 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).

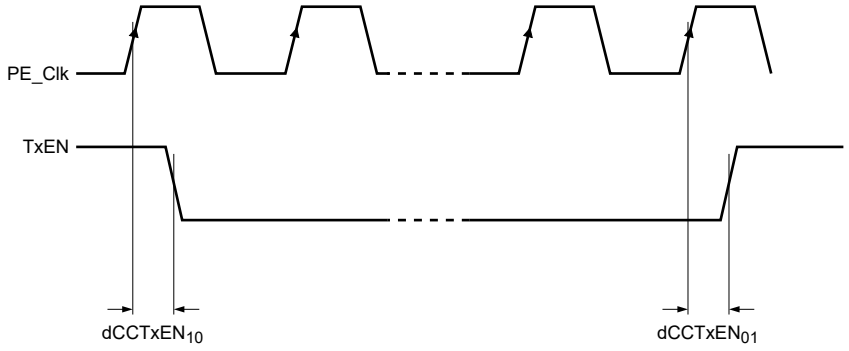


Figure 37. TxEN Signal Propagation Delay

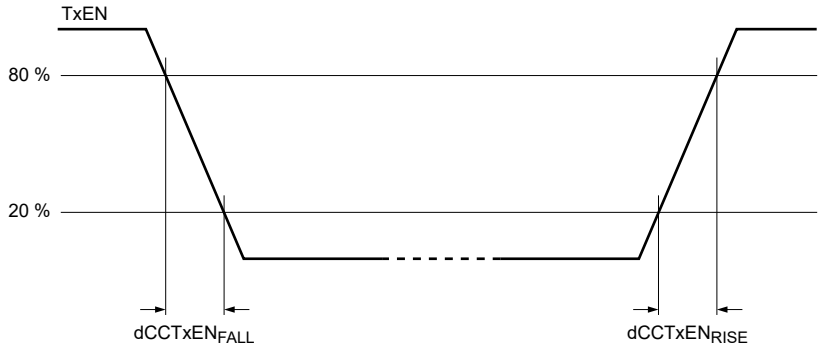


Figure 38. TxEN Signal

14.3.6.2 FlexRay - TxD

Table 41. FlexRay - TxD

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
dCCTxAsym	Asymmetry of sending CC, dCCTxD50% - N x gdBit [1]	-2.45	—	2.45	ns	N=1 gdBit = 100ns TxD load = 25pF max, SRE[2:0] = 100 (1.8V/3.3V GPIO), SRE[2:0] = 110 (3.3V GPIO)	—

Table continues on the next page...

Table 41. FlexRay - TxD*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
dCCTxDRISE25 + dCCTxDFALL25	Sum of rise and fall time of TxD signal at the output pin [1]	—	—	9	ns	TxD load = 25pF max Z = 50ohms delay = 0.6ns, SRE[2:0] = 100 (1.8V/3.3V GPIO), SRE[2:0] = 110 (3.3V GPIO)	—
dCCTxD01	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge [1]	—	—	25	ns	TxD load = 25pF max, SRE[2:0] = 100 (1.8V/ 3.3V GPIO), SRE[2:0] = 110 (3.3V GPIO)	—
dCCTxD10	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge [1]	—	—	25	ns	TxD load = 25pF max, SRE[2:0] = 100 (1.8V/ 3.3V GPIO), SRE[2:0] = 110 (3.3V GPIO)	—

1. Output timing valid for maximum external load CL = 25 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).

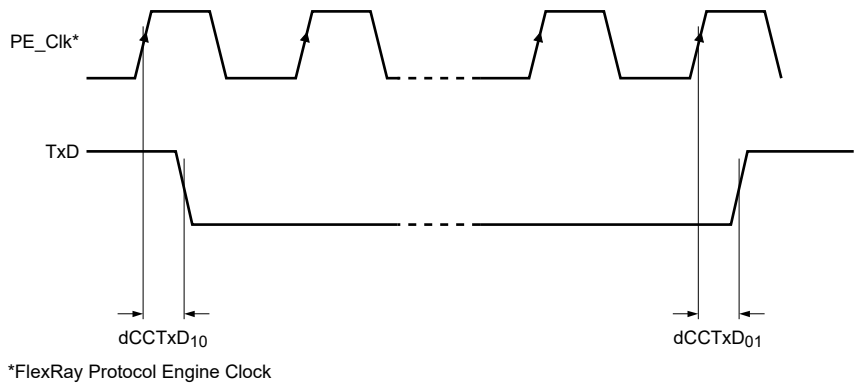


Figure 39. TxD Signal Propagation Delay

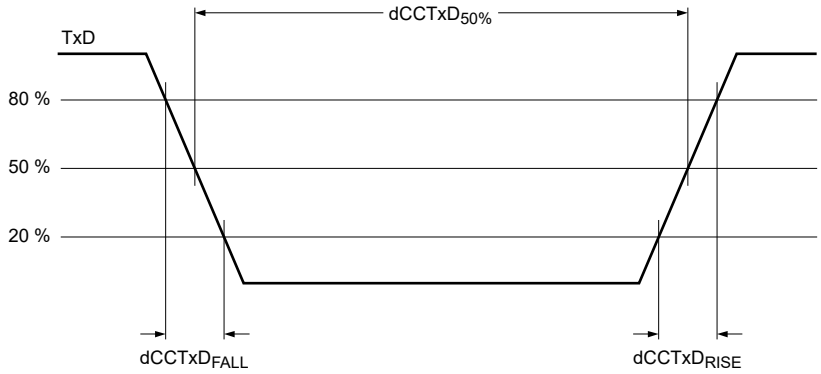


Figure 40. TxD Signal

14.3.6.3 FlexRay - RxD

Table 42. FlexRay - RxD

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
C_CCRxD	Input capacitance on RxD pin	—	—	8	pF	—	—
uCCLogic_1	Threshold for detecting logic high	35	—	70	%	—	—
uCCLogic_0	Threshold for detecting logic low	30	—	65	%	—	—
dCCRxD01	Sum of delay from actual input to the D input of the first FF, rising edge [1]	—	—	10	ns	—	—
dCCRxD10	Sum of delay from actual input to the D input of the first FF, falling edge [1]	—	—	10	ns	—	—
dCCRxAsymAccept15	Acceptance of asymmetry at receiving CC with 15pF load [1]	-31.5	—	44	ns	—	—
dCCRxAsymAccept25	Acceptance of asymmetry at receiving CC with 25pF load [1]	-30.5	—	43	ns	—	—

1. FlexRay RxD timing assumes an input signal slew rate of 2ns (20%/80%).

14.3.7 NETC

14.3.7.1 NETC MII

SRE[2:0]=100 is the required drive setting to meet the timing.

Table 43. NETC MII

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tCYC_RX	RX_CLK period	—	40 / 400	—	ns	10/100 Mbps	—
ΔtCYC_RX	RX_CLK duty cycle (tPWH / tCYC)	35	—	65	%	—	—
tS	Input setup time to RX_CLK [1]	5	—	—	ns	10/100 Mbps	—
tH	Input hold time to RX_CLK [1]	5	—	—	ns	10/100 Mbps	—
tCYC_TX	TX_CLK period [2]	—	40 / 400	—	ns	10/100 Mbps	—

Table continues on the next page...

Table 43. NETC MII*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
ΔtCYC_TX	TX_CLK duty cycle (tPWH / tCYC) [2]	35	—	65	%	—	—
tD	Output delay from TX_CLK [2]	2	—	25	ns	10/100 Mbps	—

1. Input timing assumes an input signal slew rate of 3ns (20%/80%).
2. Output timing valid for maximum external load CL = 25 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).

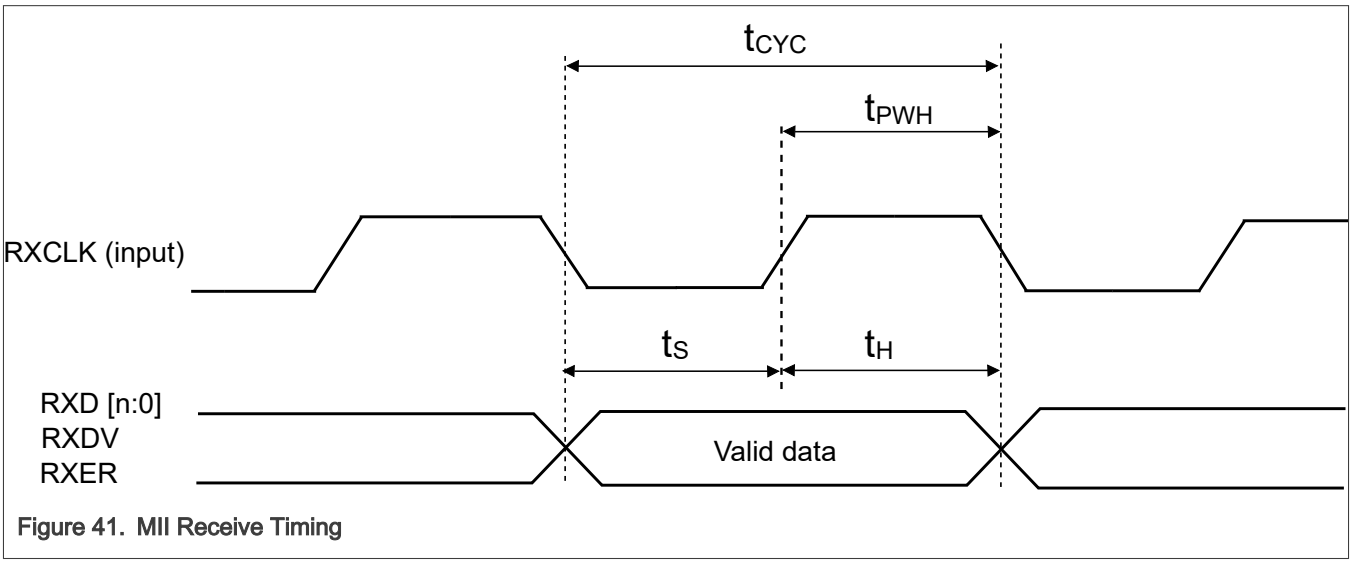


Figure 41. MII Receive Timing

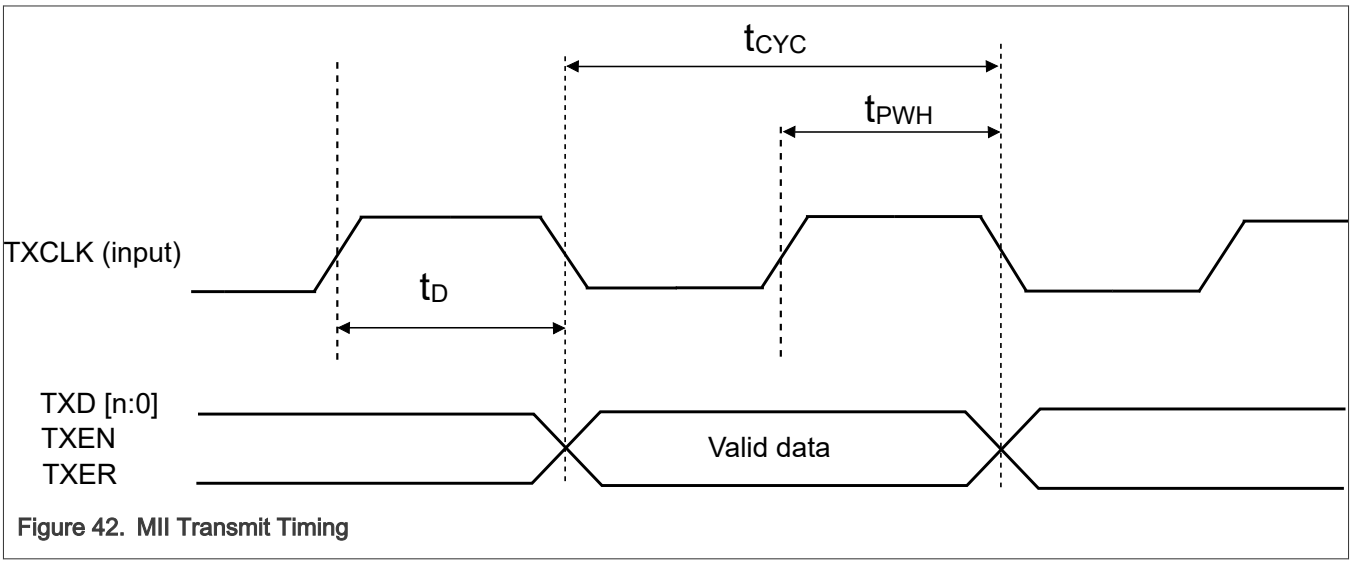


Figure 42. MII Transmit Timing

14.3.7.2 NETC RMII

SRE[2:0]=100 is the required drive setting to meet the timing.

Table 44. NETC RMII

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fRMII_CLK	RMII input clock frequency (RMII_CLK)	—	—	50	MHz	—	—
ΔtRMII_CLK	RMII_CLK duty cycle (tPWH / tCYC)	35	—	65	%	—	E3, E4, E7, E8
tS	RXD[1:0], CRS_DV, RXER to RMII_CLK setup time [1]	4	—	—	ns	—	E1
tH	RMII_CLK to RXD[1:0], CRS_DV, RXER hold time [1]	2	—	—	ns	—	E2
tDATA_VALID	RMII_CLK to TXD[1:0], TXEN data valid [2]	—	—	14	ns	CLOAD = 25pF	E6
tDATA_INVALID	RMII_CLK to TXD[1:0], TXEN data invalid [2]	2	—	—	ns	CLOAD = 25pF	E5

1. Input timing assumes an input signal slew rate of 3ns (20%/80%).
2. Output timing valid for maximum external load CL = 25 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).

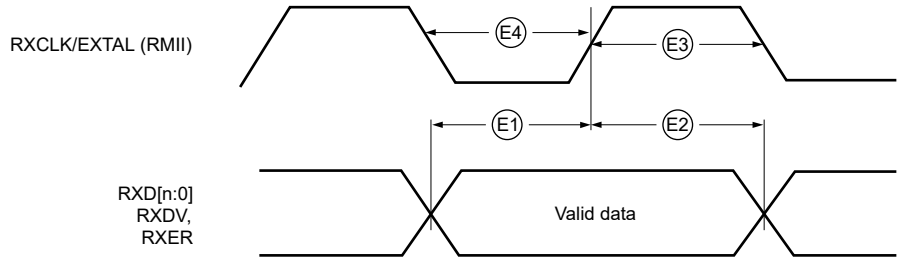


Figure 43. RMII Receive Timing

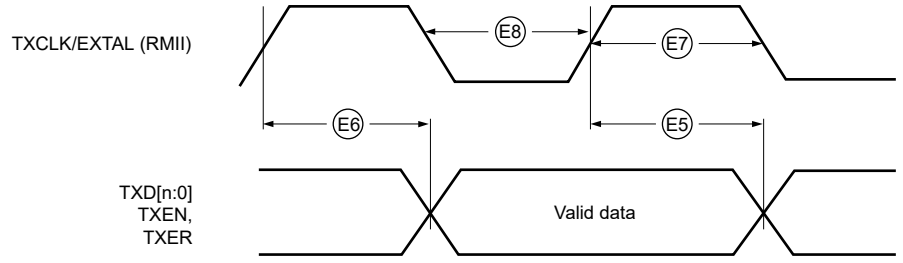


Figure 44. RMII Transmit Timing

14.3.7.3 NETC RGMII

SRE[2:0]=100 is the required drive setting to meet the timing.

Table 45. NETC RGMII

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Tcyc	Clock cycle duration [1,2,3,4]	7.2	—	8.8	ns	—	—
TskewT	Data to clock output skew (at transmitter) [1,2,3,5]	-500	—	500	ps	—	—
TskewR	Data to clock input skew (at receiver) [1,3,5]	1	—	2.6	ns	—	—
Duty_G	Clock duty cycle for Gigabit [1,3,6]	45	—	55	%	—	—
Duty_T	Clock duty cycle for 10/100T [1,3,6]	40	—	60	%	—	—

1. Measured as defined in EIA/JESD 8-6 1995 with a timing threshold voltage of VDDQ/2
2. Output timing valid for maximum external load CL = 15 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
3. RGMII timing specifications are valid for both 1.8V and 3.3V nominal I/O pad supply voltage.
4. For 10 Mbps and 100 Mbps, Tcyc will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.
5. For all versions prior to RGMII v2.0 specifications; This implies that PC board design will require clocks to be routed such that an additional delay of greater than 1.5 ns and less than 2 ns will be added to the associated clock signal. For 10/100, the max value is unspecified.
6. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

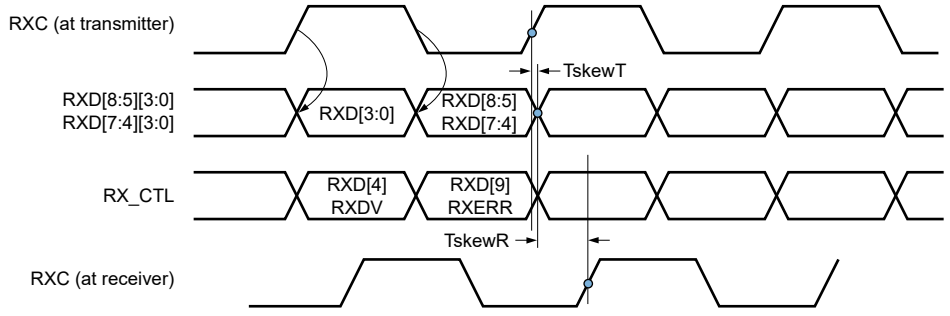


Figure 45. RGMII Receive Timing

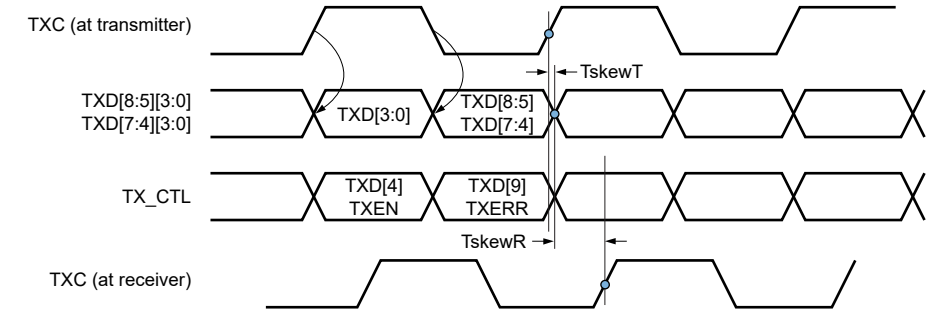


Figure 46. RGMII Transmit Timing

14.3.7.4 IEEE1588 interface

Table 46. IEEE1588 interface

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tT1588CLK	TMR_1588_CLK_IN clock period	5	—	—	ns	—	—
tT1588CLKH/ tT1588CLK	TMR_1588_CLK_IN duty cycle	40	50	60	%	—	—
tT1588CLKINJ	TMR_1588_CLK_IN peak-to-peak jitter	—	—	250	ps	—	—
tT1588CLKINR	Rise time TMR_1588_CLK_IN (20% to 80%)	1.0	—	2.0	ns	—	—
tT1588CLKINF	Fall time TMR_1588_CLK_IN (80% to 20%)	1.0	—	2.0	ns	—	—
tT1588CLKOUT	TMR_1588_CLK_OUT clock period	2 x t1588CLK	—	—	ns	—	—
tT1588CLKOTH/ tT1588CLKOUT	TMR_1588_CLK_OUT duty cycle	30.0	50.0	70.0	%	—	—
tT1588TRIGH	TMR_1588_TRIG_IN 1/2 pulse width	2 x t1588CLK	—	—	ns	—	—

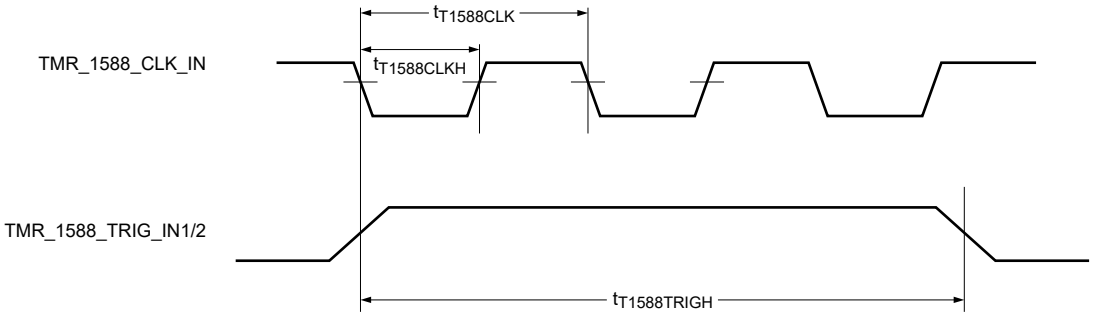
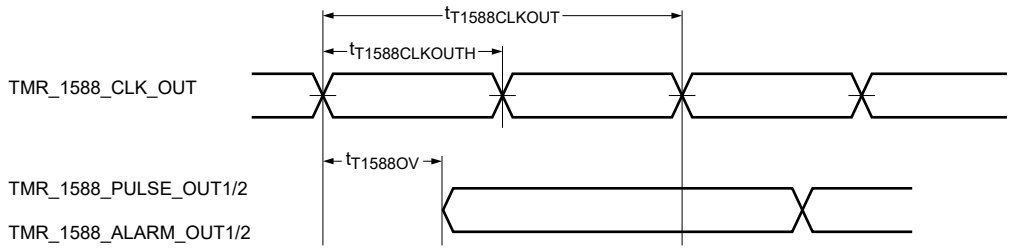


Figure 47. IEEE 1588 input AC timing



Note: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is counted starting at the falling edge.

Figure 48. IEEE 1588 output AC timing

14.3.7.5 NETC management interface

Table 47. NETC management interface

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fMDC	MDC clock frequency	—	—	5	MHz	—	—
MDIO_CH	MDC pulse width high time	40	—	60	%	—	MDC14
MDIO_CL	MDC pulse width low time	40	—	60	%	—	MDC15
tMDKHDX	MDC to MDIO delay [1]	((1+(2+6*EHOLD)*MDIO_HOLD) * tENET_CLK) – 3	—	((1+(2+6*EHOLD)*MDIO_HOLD) * tENET_CLK) + 8	ns	NEG=0	MDC10, MDC11
tMDKHDX	MDC to MDIO delay [1]	0.5*(MDC clock) – tENET_CLK	—	0.5*(MDC clock) + tENET_CLK	ns	NEG=1 and MDIO_CLK_DIV even	—
tMDKHDX	MDC to MDIO delay [1]	0.5*(MDC clock) – 2*tENET_CLK	—	0.5*(MDC clock) + 2*tENET_CLK	ns	NEG=1 and MDIO_CLK_DIV odd	—
MDIO_ISU	MDIO (input) to MDC rising edge setup time	8	—	—	ns	—	MDC12
MDIO_IH	MDIO (input) to MDC rising edge hold time	0	—	—	ns	—	MDC13

1. In the equations provided for Min and Max values, tENET_CLK is the NETC system clock period in nanoseconds, EHOLD and MDIO_HOLD are the actual values programmed into these register fields, and "MDC clock" is the MDC clock period in nanoseconds.

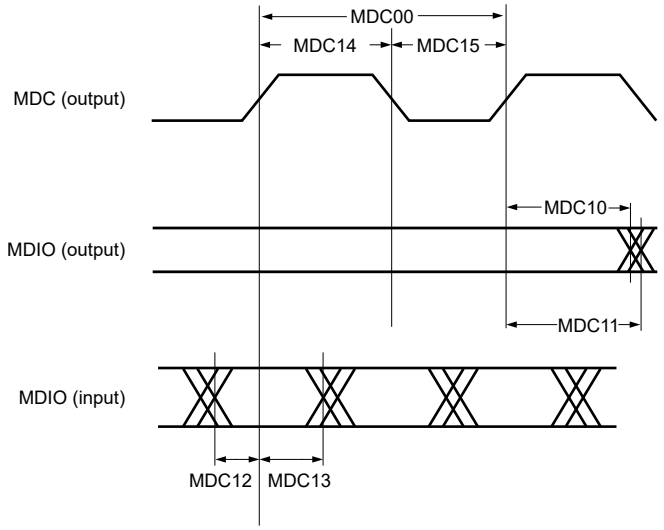


Figure 49. MDC / MDIO Timing

14.3.8 SENT Interface

Table 48. SENT Interface

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tFALL	Maximum SENT input signal fall time transition [1,2,3,4]	—	—	2.17	UI	SAE J2716 SENT standard complied with in the application, SAE J2716 recommended RC input filter used in the application	—

1. Input hysteresis enabled on I/O pads with selectable enable/disable (per the SAE 2716 SENT standard). Does not apply to pads without hysteresis control. In this case, the SENT module glitch filter should be used to reject false transitions. SRX programmable filter should be set to a value closest to 1/10th of a bit time where the max value of 128 is sufficient for long bit times.
2. By ensuring that the input fall transition is within the specification, SENT calibration and data bit errors are guaranteed not to occur as a result of variation in the input switching threshold level of the SENT input pin on the device. Switching threshold level variation is due to input signal noise, supply noise, and temperature drift.
3. This value is the ratio of the maximum 6.5uS fall time and minimum 3uS clock (UI), and assumes the transmit, clock, and measurement error tolerances as defined by the SAE 2716 SENT standard.
4. SENT inputs are supported at 3.3V on the device, with assumption that the input levels scale linearly for the recommended 3.3V circuit in the SAE 2716 SENT standard. The device does not support 1.8V or 5V SENT inputs.

14.3.9 CAN

See GPIO pads for CAN specifications.

14.3.10 CANXL

Table 49. CANXL

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tSymbolNom	CANXL PWM symbol length (PWMS + PWML)	62.5	—	200	ns	PWM Data rate= 5Mbps to 16Mbps	—
PWMS	PWM symbol period short phase [1]	5	—	0.5 *tSymbol Nom - 5	ns	50% VDD_IO, SRE[2:0]<111	—
PWML	PWM symbol period long phase	tSymbol Nom - max(PWMS)	—	tSymbol Nom - min(PWMS)	ns	50% VDD_IO, SRE[2:0]<111	—

1. To guarantee a minimum of 5ns decode time at the transceiver, the CANXL internal PWM must be programmed to ensure 10ns <= PWMS <= 0.5 * tSymbolNom – 10ns.

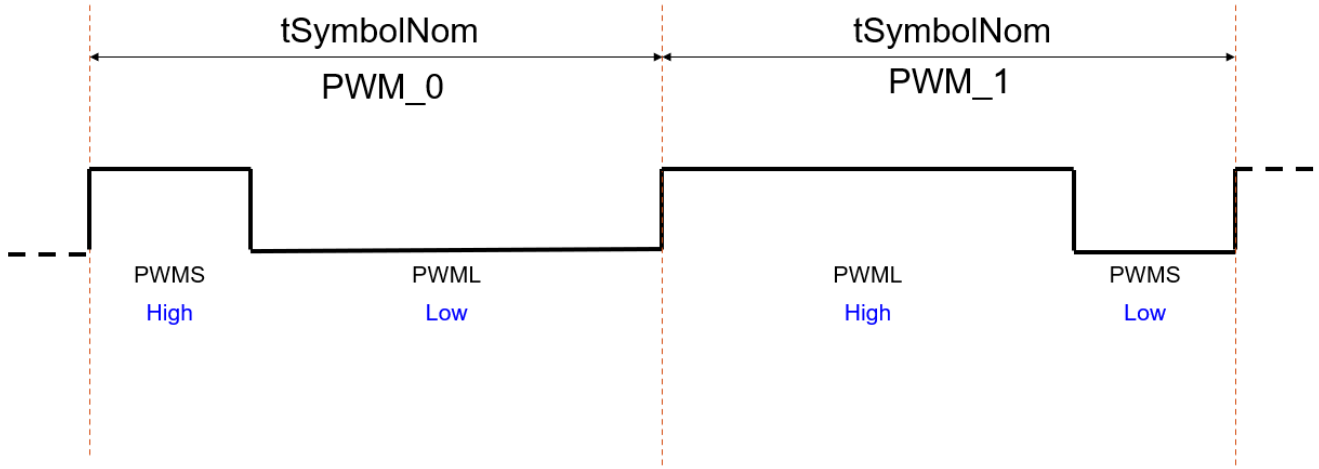


Figure 50. CANXL timing

14.3.11 PSI5

Table 50. PSI5

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	Delay from last bit of frame (CRC0) to assertion of new message received interrupt	—	—	3	us	—	—
—	Delay from internal sync pulse to sync	—	—	2	us	—	—

Table continues on the next page...

Table 50. PSI5...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	pulse trigger at the SDOUT_PSI5_n pin						
—	Delay jitter from last bit of frame (CRC0) to assertion of new message received interrupt [1]	—	—	1	cycles	—	—
—	Delay jitter from internal sync pulse to sync pulsetrigger at the SDOUT_PSI5_n pin. [2]	—	—	+/- (PSI5_1us_CLK + XBAR_DIV3_CLK)	cycles	—	—
DC	Duty Cycle [3]	35	—	65	%	—	—

1. Measured in PSI5 clock cycles. Minimum PSI5 clock period is 20ns.
2. Output timing valid for maximum external load CL = 25 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
3. PSI5 sensor input signals must meet the duty cycle requirement in order to be decoded properly.

14.4 Memories and Memory Interfaces

14.4.1 QuadSPI

14.4.1.1 QuadSPI interfaces

QuadSPI_0 supports interface (side) A. QuadSPI_1 supports two interfaces: A and B. These interfaces are not independent. See the QuadSPI chapter of the Reference Manual about their use. The following table summarizes the specifications that each interface supports.

Table 51. QuadSPI interfaces

QuadSPI instance and interface	1.8V Quad	1.8V Octal	1.8V HyperFlash	1.8V HyperRAM	3.3V Quad	3.3V Octal	3.3V HyperRAM
QuadSPI_0 side A	DDR 80 MHz SDR 133 MHz	DDR 166 MHz DDR 200 MHz SDR 133 MHz	DDR 133 and 166 MHz DDR 200 MHz	DDR 166 MHz	—	—	—
QuadSPI_1 side A	DDR 80 MHz SDR 133 MHz	DDR 166 MHz SDR 133 MHz	DDR 166 MHz	DDR 166 MHz	DDR 80 MHz SDR 133 MHz	DDR 100 MHz	DDR 100 MHz
QuadSPI_1 side B	—	—	—	—	SDR 50 MHz	—	—

14.4.1.2 QuadSPI Quad 1.8V DDR 80MHz

The SRE[2:0]=100 for 18FAST and 33GPIO pads and SRE[2:0]=101 for 3318 pads is the required drive setting to meet the timing.

FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 2.

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 52. QuadSPI Quad 1.8V DDR 80MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK	SCK clock frequency [1,2]	—	—	80	MHz	—	—
tCL_SCK	SCK clock low time [1,2]	5.625	—	—	ns	—	—
tCH_SCK	SCK clock high time [1,2]	5.625	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK) [1]	2.316	—	3.609	ns	—	—
tOD_CS	CS output delay (w.r.t. SCK) [1,3]	5.016 - n/fSCK	—	0.609 + m/fSCK	ns	—	—
tDVW	Input data valid window [2]	3.909	—	—	ns	—	—

1. Output timing valid for maximum external load CL = 20 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
2. Input timing assumes maximum input signal transition of 1ns (20%/80%).
3. Where m=TCSS and n=TCSH-1.

14.4.1.3 QuadSPI Quad 1.8V SDR 133MHz

The SRE[2:0]=100 for 33GPIO pads and SRE[2:0]=101 for 3318 pads is the required drive setting to meet the timing.

FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 2.

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 53. QuadSPI Quad 1.8V SDR 133MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK	SCK clock frequency [1,2,3]	—	—	133	MHz	DLL and Auto-Learning mode enabled	—
tCL_SCK	SCK low time [2,3]	3.383	—	—	ns	—	—
tCH_SCK	SCK high time [2,3]	3.383	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK) [3]	-0.594	—	1.594	ns	—	—
tOD_CS	CS output delay (w.r.t. SCK) [3,4]	4.016 - n/fSCK	—	4.204 + m/fSCK	ns	—	—
tDVW	Input data valid window [2,3]	4.624	—	—	ns	—	—

1. fSCK of 133.33MHz is also acceptable.
2. Input timing assumes maximum input signal transition of 1ns (20%/80%).

3. Output timing valid for maximum external load CL = 20 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
4. Where m=TCSS and n=TCSH-1.

14.4.1.4 QuadSPI Octal 1.8V SDR 133MHz

The SRE[2:0]=100 for 33GPIO pads and SRE[2:0]=101 for 3318 pads is the required drive setting to meet the timing.

FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 2.

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 54. QuadSPI Octal 1.8V SDR 133MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK	SCK clock frequency [1,2]	—	—	133	MHz	DLL and Auto-Learning mode enabled	—
tCL_SCK	SCK clock low time [1,2]	3.383	—	—	ns	—	—
tCH_SCK	SCK clock high time [1,2]	3.383	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK) [1]	-1.594	—	1.594	ns	—	—
tOD_CS	CS output delay (w.r.t. SCK) [1,3]	3.016 - n/fSCK	—	2.704 + m/fSCK	ns	—	—
tDVW	Input data valid window [2]	4.609	—	—	ns	—	—

1. Output timing valid for maximum external load CL = 20 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
2. Input timing assumes maximum input signal transition of 1ns (20%/80%).
3. Where m=TCSS and n=TCSH-1.

14.4.1.5 QuadSPI Octal 1.8V DDR 166MHz

The SRE[2:0]=000 for 18FAST, 33GPIO and 3318 pads is the required drive setting to meet the timing.

FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 2.

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 55. QuadSPI Octal 1.8V DDR 166MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK-DQS	SCK/DQS frequency [1,2]	—	—	166	MHz	fSCK duty cycle distortion is in the range of 45%-55%.	—
tCL_SCK	SCK low time [1,2]	2.711	—	—	ns	—	—
tCH_SCK	SCK high time [1,2]	2.711	—	—	ns	—	—

Table continues on the next page...

Table 55. QuadSPI Octal 1.8V DDR 166MHz...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tOD_DATA	Data output delay (w.r.t. SCK) [2]	0.616	—	2.095	ns	—	—
tOD_CS	CS output delay (w.r.t. SCK) [2,3]	3.016 - n/fSCK	—	-1.805 + m/fSCK	ns	—	—
tIH_DQS	Input hold time (w.r.t. DQS) [1]	2.105	—	—	ns	—	—
tISU_DQS	Input setup time (w.r.t. DQS) [1]	-0.616	—	—	ns	—	—

1. Input timing assumes maximum input signal transition of 1 ns (20%/80%). DQS denotes external strobe provided by the Flash.
2. Output timing valid for maximum external load CL = 20 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
3. Where m=TCSS and n=TCSH-1.

14.4.1.6 QuadSPI Octal 1.8V DDR 200MHz

The SRE[2:0]=000 for 18FAST, 33GPIO and 3318 pads is the required drive setting to meet the timing.

FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 2.

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 56. QuadSPI Octal 1.8V DDR 200MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK-DQS	SCK/DQS frequency [1,2]	—	—	200	MHz	fSCK duty cycle distortion is in the range of 45%-55%.	—
tCL_SCK	SCK low time [1,2]	2.25	—	—	ns	—	—
tCH_SCK	SCK high time [1,2]	2.25	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK) [2]	0.616	—	1.634	ns	—	—
tOD_CS	CS output delay (w.r.t. SCK) [2,3]	3.016 - n/fSCK	—	-2.266 + m/fSCK	ns	—	—
tIH_DQS	Input hold time (w.r.t. DQS) [1]	1.644	—	—	ns	—	—
tISU_DQS	Input setup time (w.r.t. DQS) [1]	-0.586	—	—	ns	—	—

1. Input timing assumes maximum input signal transition of 1 ns (20%/80%). DQS denotes external strobe provided by the Flash.
2. Output timing valid for maximum external load CL = 20 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
3. Where m=TCSS and n=TCSH-1.

14.4.1.7 QuadSPI Quad 3.3V DDR 80MHz

The SRE[2:0]=100 for 33GPIO pads and SRE[2:0]=101 for 3318 pads is the required drive setting to meet the timing.

FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 2.

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 57. QuadSPI Quad 3.3V DDR 80MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK	SCK clock frequency [1,2]	—	—	80	MHz	—	—
tCL_SCK	SCK clock low time [1,2]	5.625	—	—	ns	—	—
tCH_SCK	SCK clock high time [1,2]	5.625	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK) [1]	2.316	—	4.109	ns	—	—
tOD_CS	CS output delay (w.r.t. SCK) [1,3]	5.016 - n/fSCK	—	0.609 + m/fSCK	ns	—	—
tDVW	Input data valid window [2]	3.504	—	—	ns	—	—

1. Output timing valid for maximum external load CL = 20 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
2. Input timing assumes maximum input signal transition of 1ns (20%/80%).
3. Where m=TCSS and n=TCSH-1.

14.4.1.8 QuadSPI Quad 3.3V SDR 133MHz

The SRE[2:0]=100 for 33GPIO pads and SRE[2:0]=101 for 3318 pads is the required drive setting to meet the timing.

FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 2.

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 58. QuadSPI Quad 3.3V SDR 133MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK	SCK clock frequency [1,2,3]	—	—	133	MHz	DLL and Auto-Learning mode enabled	—
tCL_SCK	SCK clock low time [1]	3.383	—	—	ns	—	—
tCH_SCK	SCK clock high time [1,2]	3.383	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK) [2]	-1.294	—	1.844	ns	—	—

Table continues on the next page...

Table 58. QuadSPI Quad 3.3V SDR 133MHz...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tOD_CS	CS output delay (w.r.t. SCK) [2,4]	3.391 - n/fSCK	—	3.829 + m/fSCK	ns	—	—
tDVW	Input data valid window [1]	4.724	—	—	ns	—	—

1. Input timing assumes maximum input signal transition of 1ns (20%/80%).
2. Output timing valid for maximum external load CL = 20 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
3. fSCK of 133.33MHz is also acceptable.
4. Where m=TCSS and n=TCSH-1.

14.4.1.9 QuadSPI Quad 3.3V SDR 50MHz

These specs are preliminary.

The SRE[2:0]=100 for 33GPIO pads and SRE[2:0]=101 for 3318 pads is the required drive setting to meet the timing.

FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 2.

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 59. QuadSPI Quad 3.3V SDR 50MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK	SCK clock frequency	—	—	50	MHz	—	—
tCL_SCK	SCK clock low time	9	—	—	ns	—	—
tCH_SCK	SCK clock high time	9	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK)	-1.294	—	1.844	ns	—	—
tOD_CS	CS output delay (w.r.t. SCK) [1]	3.391 - n/fSCK	—	3.829 + m/fSCK	ns	—	—
tISU_SCK	Input setup time (w.r.t. SCK)	1.5	—	—	ns	—	—
tIH_SCK	Input hold time (w.r.t. SCK)	1	—	—	—	—	—

1. Where m=TCSS and n=TCSH-1.

14.4.1.10 QuadSPI Octal and HyperRAM 3.3V DDR 100MHz

The SRE[2:0]=100 for 33GPIO pads and SRE[2:0]=101 for 3318 pads is the required drive setting to meet the timing.

FLSHCR[TCSS] and FLSHCR[TCSH] should be set to 2.

Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 60. QuadSPI Octal and HyperRAM 3.3V DDR 100MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK_DQS	SCK / DQS frequency [1,2]	—	—	100	MHz	fSCK duty cycle distortion is in the range of 45%-55%.	—
tCL_SCK	SCK low time [1,2]	4.500	—	—	ns	—	—
tCH_SCK	SCK high time [1,2]	4.500	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK) [2]	1.016	—	3.484	ns	—	—
tOD_CS	CS output delay (w.r.t. SCK) [2,3]	3.016 - n/fSCK	—	-0.016 + m/fSCK	ns	—	—
tISU_DQS	Input setup time (w.r.t. DQS) [1]	-0.816	—	—	ns	—	—
tIH_DQS	Input hold time (w.r.t. DQS) [1]	3.684	—	—	ns	—	—

1. Input timing assumes maximum input signal transition of 1 ns (20%/80%). DQS denotes external strobe provided by the Flash.
2. Output timing valid for maximum external load CL = 20 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
3. Where m=TCSS and n=TCSH-1.

14.4.1.11 QuadSPI configurations

The following table shows a subset of the QuadSPI module configurations for different speeds and data rates.

NOTE

In Table 61:

- DLLCR represents DLLCRA or DLLCRB, as applicable.
- SMPR[DLLFSMPF] represents SMPR[DLLFSMPFA] or SMPR[DLLFSMPFB], as applicable.

Table 61. QuadSPI configurations

Characteristic	QuadSPI_0 side A	QuadSPI_0 side A and QuadSPI_1 side A				QuadSPI_1 side A	QuadSPI_1 side B
	1.8V Octal	1.8V Quad	1.8V Quad	1.8V Octal	1.8V HyperFlash or HyperRAM	1.8V Octal	3.3V Quad
	DDR 200 MHz	DDR 80 MHz	SDR 100 MHz	SDR 133 MHz	DDR 166 MHz	DDR 166 MHz	SDR 50 MHz
DQS mode	External DQS Edge-aligned	Internal pad loopback	Internal pad loopback	Internal pad loopback	External DQS Edge-aligned	External DQS Edge-aligned	Internal pad loopback
FLSHCR[TDH]	1	1	0	0	1	1	0

Table continues on the next page...

Table 61. QuadSPI configurations...*continued*

Characteristic	QuadSPI_0 side A	QuadSPI_0 side A and QuadSPI_1 side A				QuadSPI_1 side A	QuadSPI_1 side B
	1.8V Octal	1.8V Quad	1.8V Quad	1.8V Octal	1.8V HyperFlash or HyperRAM	1.8V Octal	3.3V Quad
	DDR 200 MHz	DDR 80 MHz	SDR 100 MHz	SDR 133 MHz	DDR 166 MHz	DDR 166 MHz	SDR 50 MHz
FLSHCR[TCSH]	2	2	2	2	2	2	2
FLSHCR[TCSS]	2	2	2	2	2	2	2
MCR[DLPEN][1]	0	1	1	1	0	0	0
DLLCR[DLLEN]	1	1	1	1	1	1	0
DLLCR[FREQEN]	1	0	0	0	1	1	NA
DLLCR[DLL_REFCNTR]	2	2	2	2	2	2	NA
DLLCR[DLLRES]	8	8	8	8	8	8	NA
DLLCR[SLV_FINE_OFFSET]	0	0	0	0	0	0	0
DLLCR[SLV_DLY_OFFSET]	0	3	3	3	0	0	0
DLLCR[SLV_DLY_COARSE]	NA	NA	NA	NA	NA	NA	0
DLLCR[SLAVE_AUTO_UPDT]	1	1	1	1	1	1	NA
DLLCR[SLV_EN]	1	1	1	1	1	1	1
DLLCR[SLV_DLL_BYPASS]	0	0	0	0	0	0	1
DLLCR[SLV_UPD]	1	1	1	1	1	1	1
SMPR[DLLFSMPF]	4	NA	NA	NA	4	4	0
SMPR[FSDLY]	NA	1	1	1	NA	NA	0
SMPR[FSPHS]	NA	NA	0	0	NA	NA	1

1. The settings for MCR[DLPEN], which disable or enable the data learning pattern mechanism, derive from simulations and testing. Users might need to alter these settings depending on delays or other behavior on their board.

14.4.1.12 QuadSPI timing diagrams

This section shows the QuadSPI timing diagrams for all modes supported by the chip. All data is based on a negative-edge data launch from the chip.

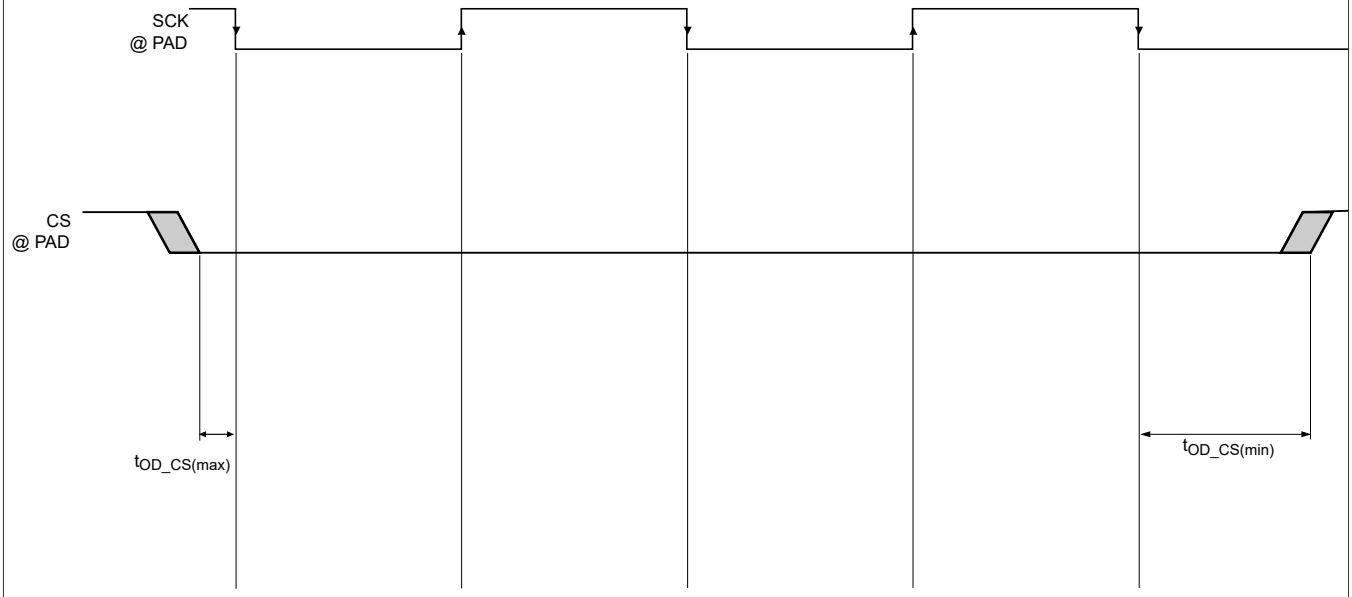


Figure 51. CS output timing

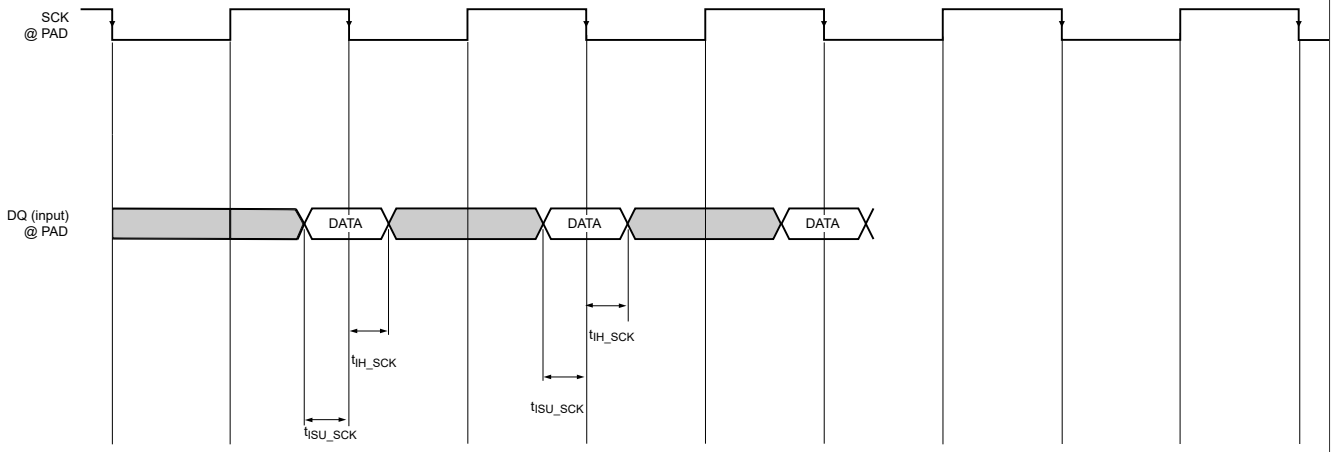


Figure 52. SDR input timing

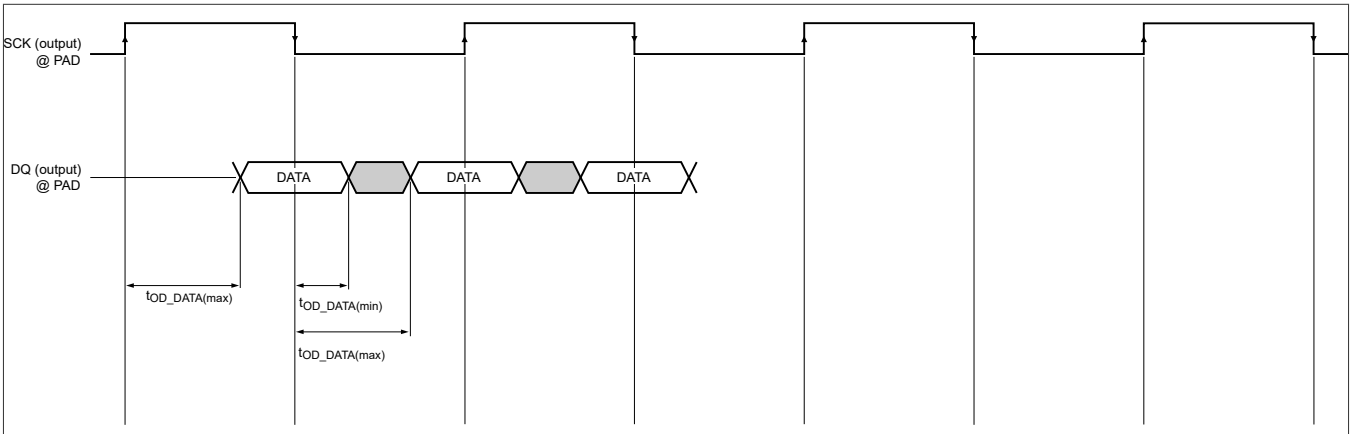


Figure 53. DDR output timing

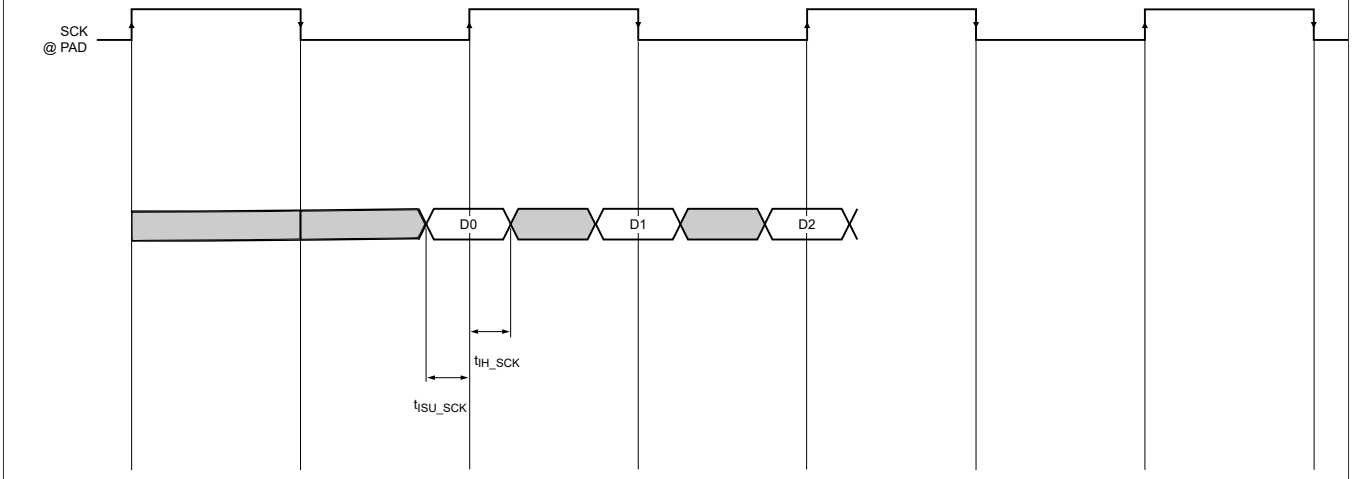
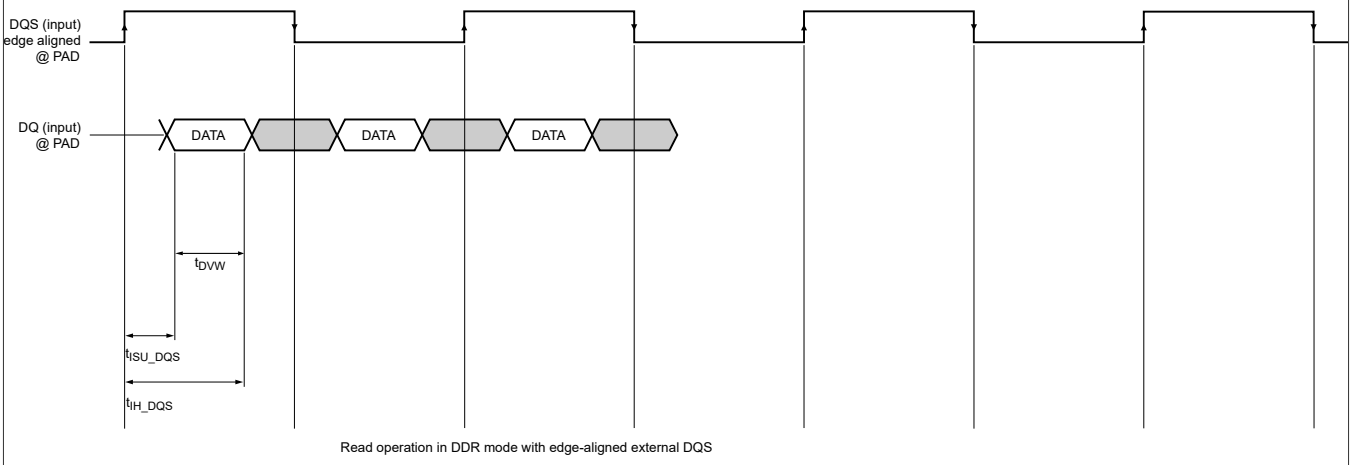


Figure 54. DDR with internal pad loopback input timing



Read operation in DDR mode with edge-aligned external DQS

Figure 55. DDR edge-aligned DQS input timing

14.4.2 uSDHC

14.4.2.1 uSDHC SD3.0/eMMC5.1 DDR

The SRE[2:0]=101 is required drive setting to meet the timing.

Data transitions measured at 35%/65% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 62. uSDHC SD3.0/eMMC5.1 DDR

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fpp	Clock frequency (eMMC high speed DDR) [1]	—	—	52	MHz	3.3V/1.8V	SD1
fpp	Clock frequency (SD/SDIO DDR50) [1]	—	—	50	MHz	1.8V	SD1
tWL	Clock low time	8.8	—	—	ns	—	—
tWH	Clock high time	8.8	—	—	ns	—	—
tTLH	Clock rise time [1,2]	—	—	0.8	ns	—	SD9
tTHL	Clock fall time [2]	—	—	0.8	ns	—	SD10
tOD	SDHC output delay (output valid)	2.7	—	5.6	ns	SDHC_CLK to SDHC_DAT	SD2
tOD	SDHC output delay (output valid)	-5.6	—	2.6	ns	SDHC_CLK to SDHC_CMD	SD6 (See SD3.0/ SDIO3.0/ eMMC5.1 SDR Mode Interface Timing figure)
tISU	SDHC Input setup time [3]	1.6	—	—	ns	SDHC_DAT to SDHC_CLK	SD3
tISU	SDHC Input setup time [3]	4.8	—	—	ns	SDHC_CMD to SDHC_CLK	SD7 (See SD3.0/ SDIO3.0/ eMMC5.1 SDR Mode Interface Timing figure)
tIH	SDHC Input hold time [3]	1.5	—	—	ns	SDHC_CLK to SDHC_DAT	SD4

Table continues on the next page...

Table 62. uSDHC SD3.0/eMMC5.1 DDR...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tIH	SDHC Input hold time [3]	1.5	—	—	ns	SDHC_CLK to SDHC_CMD	SD8 (See SD3.0/SDIO3.0/eMMC5.1 SDR Mode Interface Timing figure)

1. Output timing valid for maximum external load CL = 25 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
2. The SDHC_CLK rise/fall time specification applies to the input clock transition required in order to meet the output delay specifications. SDHC_CLK output transition time is dependent on output load and GPIO pad drive strength. See the GPIO pad specifications for detail.
3. Input signal timing assumes an input signal slew rate of 3ns (20%/80%).

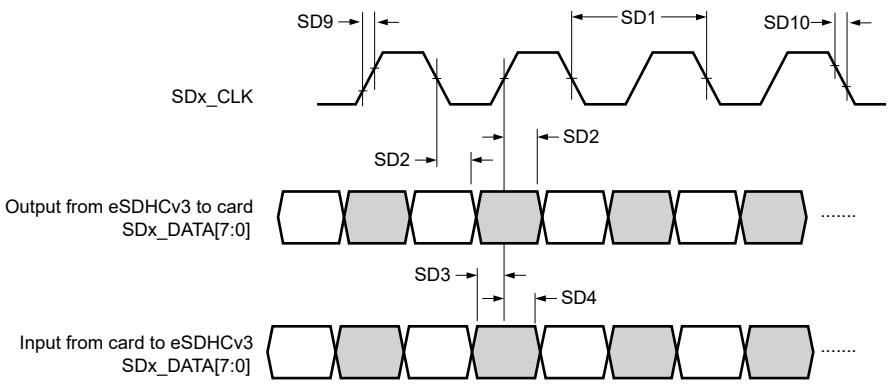


Figure 56. SD3.0/eMMC5.1 DDR Mode Interface Timing

14.4.2.2 uSDHC DDR-HS400

The SRE[2:0]=000 is required drive setting to meet the timing.

Data transitions measured at 35%/65% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 63. uSDHC DDR-HS400

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fPP	Clock frequency [1]	—	—	200	MHz	1.8V	SD1
tCL	Clock low time	2.2	—	—	ns	—	SD2
tCH	Clock high time	2.2	—	—	ns	—	SD3
tTLH	Clock rise time [1,2]	—	—	0.8	ns	—	SD8

Table continues on the next page...

Table 63. uSDHC DDR-HS400*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tTHL	Clock fall time [1,2]	—	—	0.8	ns	—	SD9
tOD1	Output skew from Edge of Data to SCK [1,3]	0.65	—	—	ns	—	SD4
tOD2	Output skew from Edge of SCK to Data [1,3]	0.65	—	—	ns	—	SD5
tRQ	Input skew (data) [4]	—	—	0.45	ns	—	SD6
tRQ	Input skew (CMD) [4,5]	—	—	0.45	ns	—	SD8
tRQH	Hold skew (data) [4]	—	—	0.45	ns	—	SD7
tRQH	Hold skew (CMD) [4,5]	—	—	0.45	ns	—	SD9
tOD	uSDHC Output delay [1]	-1.2	—	0.6	ns	SDHC_CLK to SDHC_CMD	—

1. Output timing valid for maximum external load CL = 15 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
2. The SDHC_CLK rise/fall time specification applies to the input clock transition required in order to meet the output delay specifications. SDHC_CLK output transition time is dependent on output load and GPIO pad drive strength. See the GPIO pad specifications for detail.
3. Board skew margin between CLK and DATA/CMD is considered as +/-50 ps in calculations
4. Input signal timing assumes an input signal slew rate of 1ns (20%/80%).
5. Spec numbers SD6 and SD7 are also applicable for the CMD input timing for HS400 mode in enhanced strobe mode. For HS400 mode without enhanced strobe, CMD input timing is the same as for HS200 mode.

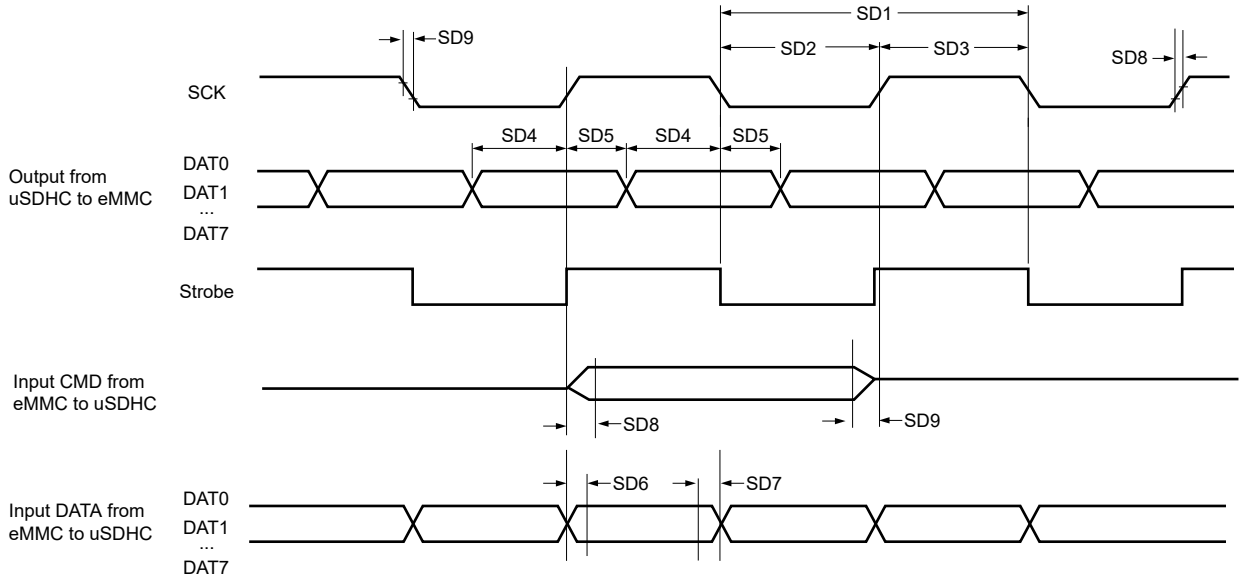


Figure 57. HS400 Mode Interface Timing

14.4.2.3 uSDHC SD3.0/SDIO3.0/eMMC5.1 SDR

The SRE[2:0]=101 is required drive setting to meet the timing.

Data transitions measured at 35%/65% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 64. uSDHC SD3.0/SDIO3.0/eMMC5.1 SDR

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fpp	Clock frequency (SD/SDIO default speed /high speed) [1,2]	—	—	25/50	MHz	3.3V	SD1
fpp	Clock frequency (eMMC legacy SDR /high speed DDR) [2,3]	—	—	26/52	MHz	1.8V/3.3V	SD1
fpp	Clock frequency (SD/SDIO SDR12/ SDR25) [1,2]	—	—	25/50	MHz	1.8V	SD1
fOD	Clock frequency (SD/SDIO identification mode) [2,4]	100	—	400	kHz	3.3V	SD1
fOD	Clock frequency (eMMC identification mode) [2]	—	—	400	kHz	1.8V/3.3V	SD1
tWL	Clock low time	8.8	—	—	ns	—	SD2
tWH	Clock high time	8.8	—	—	ns	—	SD3
tTLH	Clock rise time [2,5]	—	—	0.8	ns	—	SD4
tTHL	Clock fall time [2,5]	—	—	0.8	ns	—	SD5
tOD	SDHC output delay (output valid) [2]	-5.6	—	2.6	ns	SDHC_CLK to SDHC_ CMD / SDHC_DAT	SD6
tISU	SDHC Input setup time [6]	4.8	—	—	ns	SDHC_CMD / SDHC_ DAT to SDHC_CLK	SD7
tIH	SDHC Input hold time [6]	1.5	—	—	ns	SDHC_CLK to SDHC_ CMD / SDHC_DAT	SD8

1. In default speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.
2. Output timing valid for maximum external load CL = 25 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
3. In Legacy speed mode for MMC card, clock frequency can be any value between 0–26 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.
4. In SD/SDIO identification mode, card clock must be lower than 400 kHz, voltage ranges from 2.7V to 3.6V.
5. The SDHC_CLK rise/fall time specification applies to the input clock transition required in order to meet the output delay specifications. SDHC_CLK output transition time is dependent on output load and GPIO pad drive strength. See the GPIO pad specifications for detail.
6. Input signal timing assumes an input signal slew rate of 3ns (20%/80%).

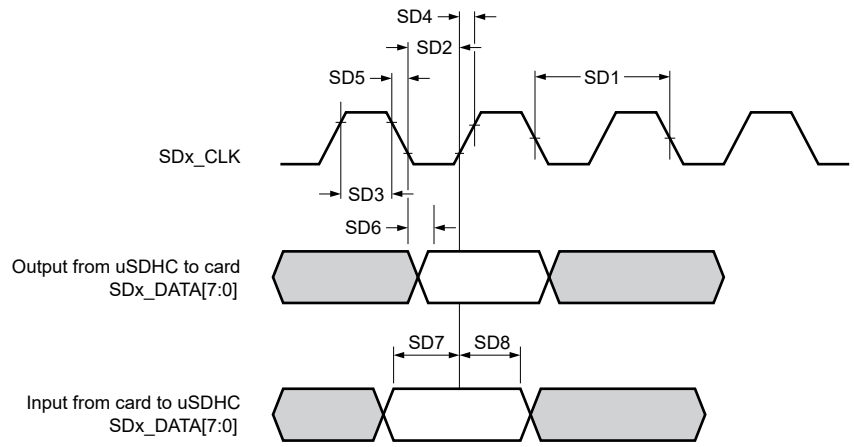


Figure 58. SD3.0/SDIO3.0/eMMC5.1 SDR Mode Interface Timing

14.4.2.4 uSDHC SDR-HS200

The SRE[2:0]=000 is required drive setting to meet the timing.

Data transitions measured at 35%/65% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply.

Table 65. uSDHC SDR-HS200

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tCLK	Clock frequency [1]	—	—	200	MHz	1.8V	SD1
tCL	Clock low time	2.2	—	—	ns	—	SD2
tCH	Clock high time	2.2	—	—	ns	—	SD3
tTLH	Clock rise time [1,2]	—	—	0.8	ns	—	SD5
tTHL	Clock fall time [1,2]	—	—	0.8	ns	—	SD6
tOD	uSDHC output delay [1]	-1.2	—	0.6	ns	SDHC_CLK to SDHC_CMD / SDHC_DAT	SD4
tODW	Input data window [3]	2.6	—	—	ns	SDHC_DAT / SDHC_CMD	SD8

1. Output timing valid for maximum external load CL = 15 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
2. The SDHC_CLK rise/fall time specification applies to the input clock transition required in order to meet the output delay specifications. SDHC_CLK output transition time is dependent on output load and GPIO pad drive strength. See the GPIO pad specifications for detail.
3. Input signal timing assumes an input signal slew rate of 1ns (20%/80%).

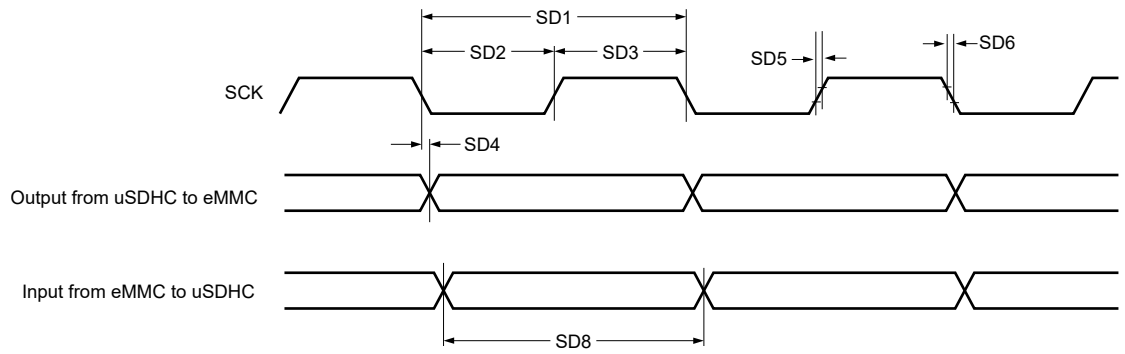


Figure 59. HS200 Mode Interface Timing

14.4.3 DDR

The chip supports the following memory types:

1. LPDDR4 SDRAM compliant to JEDEC209-4B LPDDR4 JEDEC standard release.

14.4.3.1 DDR Common DC Input

The specifications given in the table below represent the common DC input conditions for all DDR interface modes. Unless otherwise specified, all input specifications (both common and DDR standard specific) are measured at the host PHY input pins. Subsequent sections list input parameters for the specific memory interface standards.

Table 66. DDR Common DC Input

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IIZ-BP	Input leakage current [1]	-50	—	50	uA	—	—
VIH-DC_BPDAT	Input high voltage threshold	VREF+0.085	—	—	V	—	—
VIL-DC_BPDAT	Input low voltage threshold	—	—	vref - 0.085	V	—	—

1. Leakage current is measured when the pin is configured to a high-impedance state with all on-die termination disabled. Leakage is valid for any input except for Vref over the range:0 <= VIN <= VDD_IO_DDR0. All pins not under test = VSS or VDD_IO_DDR0.

14.4.3.2 DDR Common DC Output

Table 67. DDR Common DC Output

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
ROnPu	Output driver pull-up impedance: DQ, DQS outputs [1]	—	120,60,40	—	Ohm	—	—
ROnPd	Output driver pull-down impedance: DQ, DQS outputs [1]	—	120,60,40	—	Ohm	—	—

Table continues on the next page...

Table 67. DDR Common DC Output...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
ROnPu	Output driver pull-up impedance: address, command [1]	—	120,60,40	—	Ohm	—	—
ROnPd	Output driver pull-down impedance: address, command [1]	—	120,60,40	—	Ohm	—	—
ROnPu	Output driver pull-up impedance: DDR0_RESET_B, CKE outputs [2]	—	18-28	—	Ohm	—	—
ROnPd	Output driver pull-down impedance: DDR0_RESET_B, CKE outputs [2]	—	18-28	—	Ohm	—	—
ZN	Driver impedance calibration resistor	118.8	120	121.2	Ohm	—	—

1. Calibrated at VDD_IO_DDR0 / 2.
2. For the DDR0_RESET_B pin and CKE pin, the driver is in maximum strength and impedance value is process dependent.

NOTE: Refer to IBIS model for the complete IV curve characteristics.

14.4.3.3 LPDDR4 Output Timing

Table 68. LPDDR4 Output Timing

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tCK(avg)	Average clock period [1]	—	1.25	—	ns	—	—
tDOeye	Output data eye [1,2,3]	0.45	—	—	UI	—	—
tCAOeye	CA output data eye [1,4]	0.55	—	—	UI	UI=1250ps, LPDDR4	—
tCAOeye-flash	CA output data eye in flash memory mode	0.45	—	—	UI	UI=1250pcs, Flash memory mode	—

1. Measurements were done with signals terminated with a 50ohm resistor terminated to VSS, Phy output is calibrated to a drive strength of 40ohms. Slew rate AtxSlewRate was set to 0x1FF (PreDrvMode=1, PreN=F,PreP=F); TxSlewRate was set 0x1FF (PreDrvMode=1, PreN=F, PreP=F).
2. Tx DQS to MCLK edges are trained to be aligned.
3. tDOeye is trained to be shifted min 200 ps from DQS edge (tDQS2DQ learning).
4. Addr/Cmd is centered aligned by training.

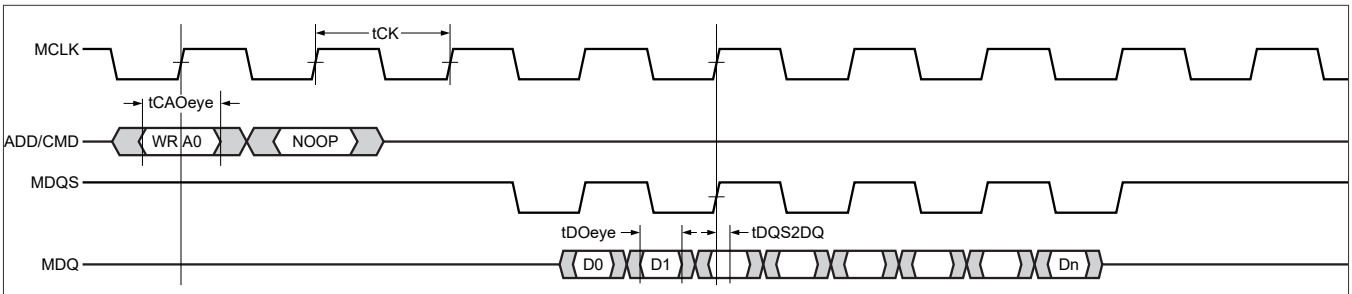


Figure 60. LPDDR4 Output Timing

14.4.4 Flash KGD

Table 69. Flash KGD

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
T_Flash_On	Flash lifetime power-on duration	40	200	—	hours	—	—
Flash Reads	Lifetime reads	1M	—	—	array reads	Refers to the read of 16MB	—
DR_100	Data retention (between 0 and 100 program/ erase cycles) [1]	20	—	—	years	—	—
DR_1000	Data retention (between 100 and 1000 program/erase cycles) [1]	5	—	—	years	—	—
E	Endurance [1]	100	1000	—	Program/ erase cycles	—	—

1. You can use only block erase or chip erase (sector erase is not allowed). It does not support EEPROM emulation as well.

14.4.5 AE Flash Memory Specifications

14.4.5.1 AE Flash Program Erase

Table 70. AE Flash Program Erase

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tdwpgm	Doubleword (64 bits) program time [1,2]	—	43	—	us	25C	—
tdwpgm	Doubleword (64 bits) program time [2,3]	—	—	100	us	Initial Max, 20C <= Ta <= 30C	—
tdwpgm	Doubleword (64 bits) program time [2,3]	—	—	150	us	Initial Max, Full Temp, -40C <= Tj <= 150C	—

Table continues on the next page...

Table 70. AE Flash Program Erase...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tdwpgm	Doubleword (64 bits) program time [2,4]	—	55	—	us	Typical End of Life, -40C <= Tj <= 150C	—
tdwpgm	Doubleword (64 bits) program time [2,5]	—	—	500	us	Lifetime Max, <= 250,000 cycles	—
tppgm	Page (256 bits) program time [2,5]	—	73	—	us	25C	—
tppgm	Page (256 bits) program time [2,3]	—	—	200	us	Initial Max, 20C <= Ta <= 30C	—
tppgm	Page (256 bits) program time [2,3]	—	—	300	us	Initial Max, Full Temp, -40C <= Tj <= 150C	—
tppgm	Page (256 bits) program time [2,4]	—	108	—	us	Typical End of Life, -40C <= Tj <= 150C	—
tppgm	Page (256 bits) program time [2,5]	—	—	500	us	Lifetime Max, <= 250,000 cycles	—
tqppgm	Quad-page (1024 bits) program time [2,5]	—	268	—	us	25C	—
tqppgm	Quad-page (1024 bits) program time [2,3]	—	—	800	us	Initial Max, 20C <= Ta <= 30C	—
tqppgm	Quad-page (1024 bits) program time [2,3]	—	—	1200	us	Initial Max, Full Temp, -40C <= Tj <= 150C	—
tqppgm	Quad-page (1024 bits) program time [2,4]	—	396	—	us	Typical End of Life, -40C <= Tj <= 150C	—
tqppgm	Quad-page (1024 bits) program time [2,5]	—	—	2000	us	Lifetime Max, <= 250,000 cycles	—
t16kpgm	16KB Block program time [2,5]	—	34	—	ms	25C	—
t16kpgm	16KB Block program time [2,3]	—	—	45	ms	Initial Max, 20C <= Ta <= 30C	—
t16kpgm	16KB Block program time [2,3]	—	—	50	ms	Initial Max, Full Temp, -40C <= Tj <= 150C	—
t16kpgm	16KB Block program time [2,4]	—	40	—	ms	Typical End of Life, -40C <= Tj <= 150C	—
t16kpgm	16KB Block program time [2,5]	—	—	1000	ms	Lifetime Max, <= 250,000 cycles	—

Table continues on the next page...

Table 70. AE Flash Program Erase...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
t64kpgm	64KB Block program time [2,5]	—	138	—	ms	25C	—
t64kpgm	64KB Block program time [2,3]	—	—	180	ms	Initial Max, 20C <= Ta <= 30C	—
t64kpgm	64KB Block program time [2,3]	—	—	210	ms	Initial Max, Full Temp, -40C <= Tj <= 150C	—
t64kpgm	64KB Block program time [2,4]	—	170	—	ms	Typical End of Life, -40C <= Tj <= 150C	—
t64kpgm	64KB Block program time [2,5]	—	—	1600	ms	Lifetime Max, <= 250,000 cycles	—
t16kers	16KB Block erase time [2,5]	—	168	—	ms	25C	—
t16kers	16KB Block erase time [2,3]	—	—	290	ms	Initial Max, 20C <= Ta <= 30C	—
t16kers	16KB Block erase time [2,3]	—	—	320	ms	Initial Max, Full Temp, -40C <= Tj <= 150C	—
t16kers	16KB Block erase time [2,4]	—	250	—	ms	Typical End of Life, -40C <= Tj <= 150C	—
t16kers	16KB Block erase time [2,5]	—	—	1000	ms	Lifetime Max, <= 250,000 cycles	—
t64kers	64KB Block erase time [2,5]	—	315	—	ms	25C	—
t64kers	64KB Block erase time [2,3]	—	—	490	ms	Initial Max, 20C <= Ta <= 30C	—
t64kers	64KB Block erase time [2,3]	—	—	590	ms	Initial Max, Full Temp, -40C <= Tj <= 150C	—
t64kers	64KB Block erase time [2,4]	—	420	—	ms	Typical End of Life, -40C <= Tj <= 150C	—
t64kers	64KB Block erase time [2,5]	—	—	1600	ms	Lifetime Max, <= 250,000 cycles	—

1. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
2. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming. Factory fast block program times assume factory fast quad-page programming.
3. Plant Programing times provide guidance for timeout limits used in the factory.
4. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
5. Conditions: -40°C ≤ Tj ≤ 150°C, full spec voltage.

14.4.5.2 AE Flash Array

Table 71. AE Flash Array

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tai16kseq	Array integrity time for sequential sequence on 16KB block [1,2]	—	—	512 x Tperiod x Nread	—	—	—
tai64kseq	Array integrity time for sequential sequence on 64KB block [1,2]	—	—	2048 x Tperiod x Nread	—	—	—
tmr16kseq	Margin Read time for sequential sequence on 16KB block [1,2]	73.81	—	110.7	us	—	—
tmr64kseq	Margin Read time for sequential sequence on 64KB block [1,2]	237.65	—	356.5	us	—	—

1. The units for array integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.
2. Array integrity times must be calculated and depend on system frequency and number of clocks per read. The equation presented requires Tperiod (which is the unit accurate period--thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution--thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read and has the address pipeline set to 2, Nread would equal 6-2, or 4).

14.4.5.3 AE Flash Module Life

Table 72. AE Flash Module Life

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
P/E Cycles	Number program/ erase cycles per block (16KB, 32KB, 64KB blocks)	250000	—	—	P/E Cycles	-40C < Tj < 150C	—
P/E Cycles	Number program/ erase cycles per block (256KB blocks)	1000	250000	—	P/E Cycles	-40C < Tj < 150C	—
Data Retention	Minimum data retention	50	—	—	Years	Blocks with 0 - 1000 P/E cycles, -40C < Tj < 150C	—
Data Retention	Minimum data retention	20	—	—	Years	Blocks with 0 - 100,000 P/E cycles, -40C < Tj < 150C	—
Data Retention	Minimum data retention	10	—	—	Years	Blocks with 0 - 250,000 P/E cycles, -40C < Tj < 150C	—

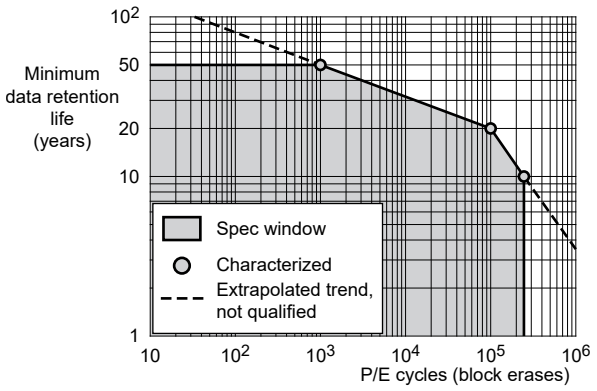


Figure 61. Flash Module Life

14.4.5.4 AE Flash AC Timing

Table 73. AE Flash AC Timing

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tpsus	Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1	—	9.5 + 4 sys clock periods	11.5 + 4 sys clock periods	us	—	—
tesus	Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1	—	16 + 4 sys clock periods	20.8 + 4 sys clock periods	us	—	—
tres	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low	—	—	100	ns	—	—
tdone	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/ erase until the MCR-DONE bit is cleared	—	—	5	ns	—	—
tdones	Time from 1 to 0 transition on the MCR-EHV bit aborting a program/ erase until the MCR-DONE bit is set to a 1	—	16 + 4 sys clock periods	20.8 + 4 sys clock periods	us	—	—
tdrcv	Time to recover once exiting low power mode	16 + 7 sys clock periods	—	45 + 7 sys clock periods	us	—	—

Table continues on the next page...

Table 73. AE Flash AC Timing...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
taistart	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns	—	—
taistop	Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 + 16 sys clock periods	ns	—	—
tmrstop	Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 + 4 sys clock periods	—	20.42 + 4 sys clock periods	us	—	—

14.4.5.5 AE Flash Read Latency

Table 74. AE Flash Read Latency

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	Flash read latency on line buffer miss (initial beat) [1]	—	—	8.5/9	cycles	RWSC = 4, APC = 1, fSYS_AE = 160MHz	—

Table continues on the next page...

Table 74. AE Flash Read Latency...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	Flash read latency on line buffer hit (initial beat) [1]	—	—	3.5/4	cycles	RWSC = 4, APC = 1, fSYS_AE = 160MHz	—
—	Flash read latency for subsequent beats of a cache line fill [1]	—	—	1	cycles	RWSC = 4, APC = 1, fSYS_AE = 160MHz	—

1. Cycle is defined as one cycle of the f SYS_AE clock.

14.5 Analog Modules

14.5.1 Temperature Monitoring Unit (TMU)

The table below gives the specification for the Temperature Monitoring Unit (TMU). Specifications apply to all remote temperature sensors connected to the TMU on the device.

Table 75. Temperature Monitoring Unit (TMU)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TRANGE	Temperature monitoring range [1]	-45	—	155	C	—	—
TERR	Temperature sensor error	-8	—	8	C	TRANGE = -40C to 99C	—
TERR	Temperature sensor error	-5	—	5	C	TRANGE = 100C to 144C	—
TERR	Temperature sensor error	-3	—	3	C	TRANGE = 145C to 150C	—

1. Accuracy outside of operating range (-40 to 150) is not guaranteed.

14.5.2 SAR ADC

ADC performance specifications are only guaranteed when the injection current limits in the operating conditions table of this electrical specification are met.

Although functionally supported on devices with 2 ADCs, ADC performance specifications are not guaranteed for shared channels between the 2 ADCs if the input channel is sampled or converted simultaneously by both ADCs. For best performance in this case, the external capacitance at the input pin and reference pin should be maximized.

Table 76. SAR ADC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VAD_INPUT	ADC Input Voltage [1]	VSS_ADC	—	VDD_ANA	V	on or off channels	—
fAD_CK	ADC Clock Frequency	20	—	80	MHz	—	—

Table continues on the next page...

Table 76. SAR ADC...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tSAMPLE	ADC Input Sampling Time [2]	275	—	—	ns	—	—
tCONV	ADC Total Conversion Time [3]	1	—	—	us	—	—
tRECOVERY	ADC Initialization Time from power-down	—	—	1	us	—	—
CAD_INPUT	ADC Input Capacitance	—	—	6.5	pF	ADC component plus pad capacitance (~2pF)	—
RAD_INPUT	ADC Input Series Resistance	—	—	1.25	kΩ	—	—
OFS	ADC Offset Error [4]	-6	—	6	LSB	after calibration	—
GNE	ADC Gain Error (full scale) [4]	-6	—	6	LSB	after calibration	—
DNL	ADC Differential Non-linearity [4,5,6]	-1	—	2	LSB	after calibration	—
INL	ADC Integral Non-linearity [4,6]	-3	—	3	LSB	after calibration	—
TUE	ADC Total Unadjusted Error [4,6]	-8	—	8	LSB	after calibration	—
SNR	Signal-to-Noise Ratio [4]	—	65	—	dBFS	input signal frequency <= 50KHz	—
THD	Total Harmonic Distortion [4]	—	72	—	dBFS	Input signal frequency <= 50KHz.	—
IAD_LKG	ADC Input Leakage Current [7]	-1	—	1	uA	TJ = 150C, Dedicated input channel, channel selection switch open	—
IAD_LKG	ADC Input Leakage Current [7]	-2	—	2	uA	TJ = 150C, Shared channel, channel selection switch open	—
CP1	ADC input pin capacitance 1	—	—	2	pF	—	—
CP2	ADC input pin capacitance 2	—	—	0.5	pF	—	—
CS	ADC input sampling capacitance	—	—	4	pF	—	—
RSW1	Internal resistance of analog source	—	—	600	ohm	—	—

Table continues on the next page...

Table 76. SAR ADC*...continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
RAD	Internal resistance of analog source	—	—	150	ohm	—	—

1. The reduced limits for VAD_INPUT in this table are recommended for normal operation.
2. During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within tsample. After the end of the sample time tsample, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock tsample depend on programming.
3. 1Msps is the ADC output rate and includes both sampling and analog to digital conversion.
4. ADC performance specifications are guaranteed when calibration uses maximum averaging i.e. when AVGEN = 1 and NRSMPL = 3.
5. During calibration, the ADC determines its (positive or negative) offset value and stores the result in an internal register. During each conversion, the offset value is subtracted from the raw result to compensate the individual ADC offset.Since the ADC cannot generate negative numbers, a negative calibration offset results in a minimum output code between 0 and 6. A positive calibration offset does not impact the max. code output of 4095. Calibration fails if it determines an offset larger than +/- 6 LSB.
6. This specification is taken with averaging through post process ADC data.
7. The maximum and minimum leakage current values are reached when Vin=VREF and Vin=0, respectively.

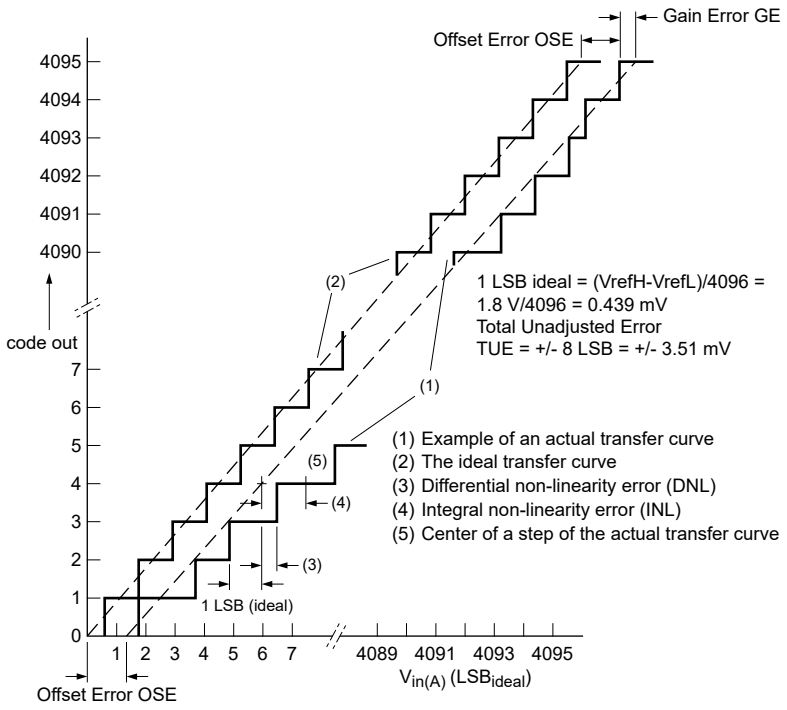


Figure 62. SAR ADC Specification Characteristics

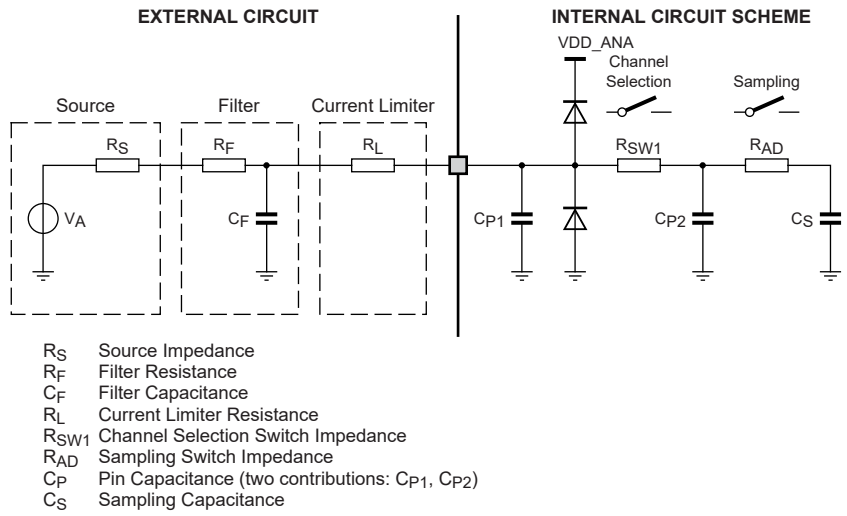


Figure 63. SAR ADC Input Circuit

14.5.3 AE SAR ADC

Table 77. AE SAR ADC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VAD_INPUT	ADC Input Voltage [1,2]	SAR*_VRL	—	SAR*_VRH	V	on or off channels	—
fAD_CK	ADC Clock Frequency [2]	20	—	80	MHz	—	—
fSAMPLE	ADC Input Sampling Frequency [2,3]	—	—	993	KHz	—	—
tSAMPLE	ADC Sample Time [2]	275	—	—	ns	12-bit resolution	—
tCONV	ADC Conversion Time [2,4]	662.5	—	—	ns	—	—
Cs	ADC Input Sampling Capacitance [2]	—	3.8	6.5	pF	ADC component only.	—
Cp1	ADC Input Pad 1 Capacitance [2]	—	—	2	pF	—	—
Cp2	ADC Input Pad 2 Capacitance [2]	—	—	0.6	pF	—	—
RAD_INPUT	ADC Input Internal Series Resistance (RSW1 + RAD) [2]	—	—	1350	Ω	4.5V <= VRH <= 5.5V	—
RAD_INPUT	ADC Input Internal Series Resistance (RSW1 + RAD) [2]	—	—	1850	Ω	3.0V <= VRH <= 3.6V	—
OFS	ADC Offset Error [2]	-4	—	4	LSB	after calibration	—

Table continues on the next page...

Table 77. AE SAR ADC...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
GNE	ADC Gain Error (full scale) [2]	-4	—	4	LSB	after calibration	—
DNL	ADC Differential Non-linearity [2,5]	-1	—	2	LSB	after calibration	—
INL	ADC Integral Non-linearity [2]	-2	—	2	LSB	after calibration	—
TUE	ADC Total Unadjusted Error [2]	-6	—	6	LSB	after calibration, no current injection on an adjacent pin	—
SNR	Signal-to-Noise Ratio [2,6]	67	—	—	dBFS	Input signal frequency <= 125KHz, VRH = 5.0V	—
THD	Total Harmonic Distortion [2,6]	—	—	-65	dBFS	Input signal frequency <= 125KHz, VRH >= 4.5V	—
THD	Total Harmonic Distortion [2,6]	—	—	-63	dBFS	50KHz < Input signal frequency < 125KHz, VRH <= 4.5V	—
SINAD	Signal-to-Noise and Distortion [2,6]	65	—	—	dBFS	Input signal frequency <= 125KHz, VRH >= 4.5V	—
SINAD	Signal-to-Noise and Distortion [2,6]	62.5	—	—	dBFS	50KHz < Input signal frequency < 125KHz, VRH <= 4.5V	—
IAD_LKG	ADC Input Leakage Current [2]	—	—	100	nA	VAD_INPUT <= VREFH - 150mV TJ = 150C Dedicated input channel, channel OFF	—
IAD_LKG	ADC Input Leakage Current [2]	—	—	250	nA	VAD_INPUT <= VREFH - 150mV TJ = 150C Shared channel, channel OFF	—

1. The ADC is fully functional with Vin from VREFL to VREFH, but performance specifications are only guaranteed within 150mV of each rail.
2. ADC performance specifications are guaranteed without injection current on the input pin. Injection current limits and lifetime durations are given in the Absolute Maximum Ratings section.
3. During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within tsample. After the end of the sample time tsample, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock tsample depend on programming.
4. Total conversion time is the sum of the sample time tSAMPLE and the conversion time tCONV.
5. No missing codes. During calibration, the ADC will determine the its offset value and store the result in an internal OCV register as a signed value in 15bit resolution notation. During each conversion, the OCV value will be subtracted from the raw result to compensate the individual ADC offset. Since the ADC analog module cannot generate negative numbers, a negative OCV value of 0xFFF8 or greater will cause that code 0 will never be the final ADC result.

6. If multiple ADCs are running in parallel, the same frequency must be used for f AD_CK for all ADCs. If the clocks are not synchronized, then a 12dB degradation in performance may be observed.

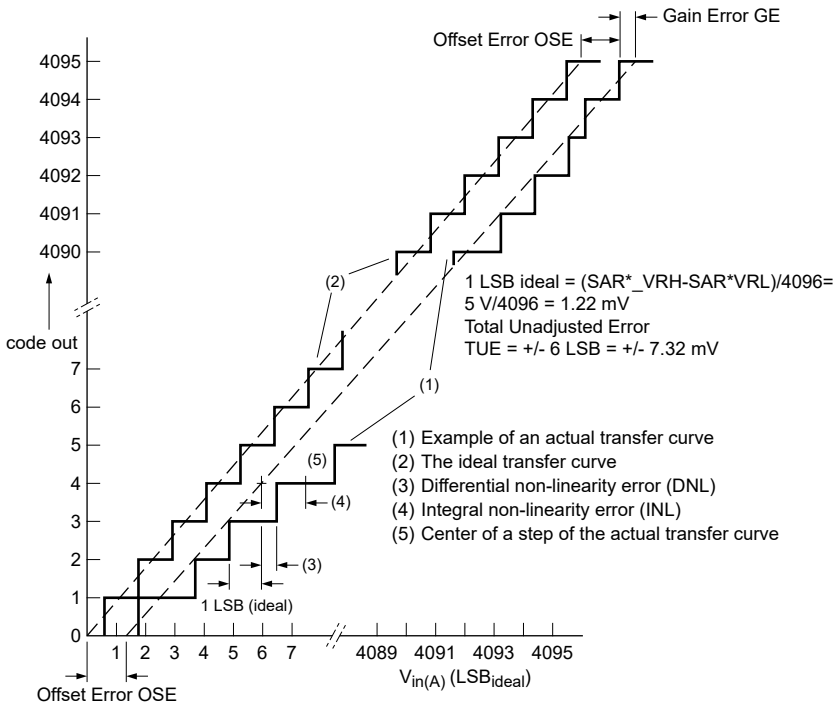
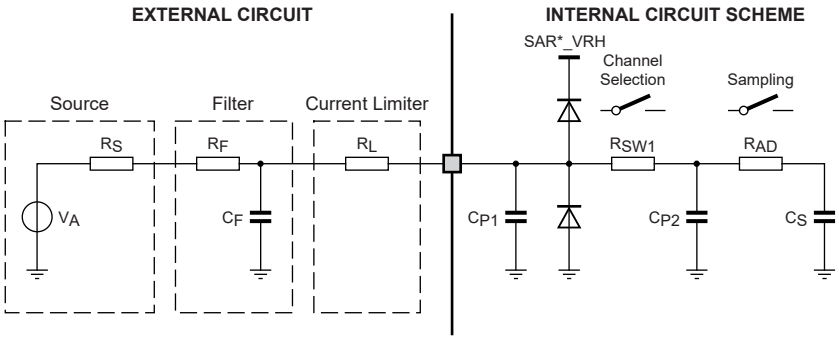


Figure 64.



R_S Source Impedance
R_F Filter Resistance
C_F Filter Capacitance
R_L Current Limiter Resistance
R_{SW1} Channel Selection Switch Impedance
R_{AD} Sampling Switch Impedance
C_P Pin Capacitance (two contributions: C_{P1}, C_{P2})
C_S Sampling Capacitance

Figure 65.

14.6 Motor Control

14.6.1 LCU

Table 78. LCU

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tMIPW	LCU input pulse width [1]	4	—	—	tPER_CLK	—	—
tMOPW	LCU output pulse width [1,2]	1	—	—	tPER_CLK	—	—

1. tPER_CLK is the period of the peripheral clock (PER_CLK) on the device.
2. Actual output pulse may be larger when considering a slow transitioning output.

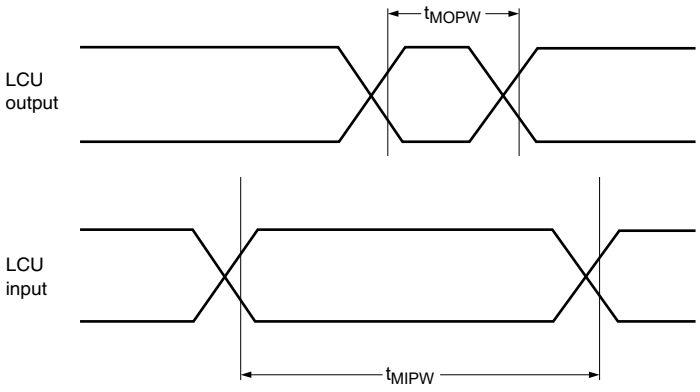


Figure 66. LCU timing

14.6.2 SINC timing

Table 79. SINC timing

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
MCLK	External modulator clock frequenc	0.02	—	33	MHz	—	—
MMCLK	Manchester Modulator clock frequenc	—	—	22	MHz	Clock recovered internally using External Modulator bit	—
TS1	Setup time from data valid to clock high	2	—	—	ns	—	—
TH1	Hold time from clock high to data valid	2	—	—	ns	—	—
TS2	Setup time from data valid to clock low	2	—	—	ns	—	—
TH2	Hold time from clock low to data valid	2	—	—	ns	—	—

Table continues on the next page...

Table 79. SINC timing...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TS3	Setup time from data valid to clock high	2	—	—	ns	—	—
TH3	Hold time from clock high to data valid	2	—	—	ns	—	—
TS4	Setup time from data valid to clock low	2	—	—	ns	—	—
TH4	Hold time from clock low to data valid	2	—	—	ns	—	—

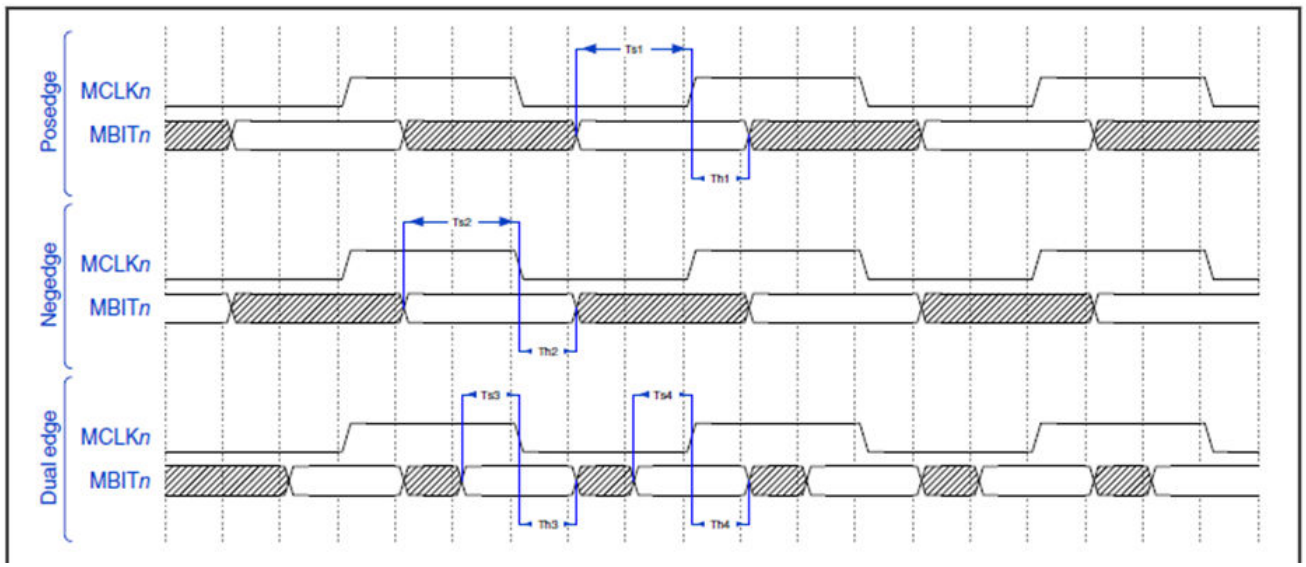


Figure 67. SINC timing

14.7 Digital NanoEdge timing

Table 80. Digital NanoEdge timing

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tHRESPWM_CHOFFS	Relative output delay between any channel [1]	—	—	10	ns	—	—
tHRESPWM_PAIROFFS	Relative output delay within channel pairs [1]	—	—	2	ns	—	—
tHRESPWM_RES	PWM delay resolution	617	1/fHRESPWM	—	ps	—	—

1. Corresponding pad configurations must be identical (e.g. slew rate, load, ...)

14.8 Glitch Filter

Table 81. Glitch Filter

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TFILT	Glitch filter max filtered pulse width [1,2,3,4]	—	—	17	ns	—	—
TUNFILT	Glitch filter min unfiltered pulse width [1,3,4,5]	400	—	—	ns	—	—

1. An input signal pulse is defined by the duration between the input signal's crossing of a Vil/Vih threshold voltage level, and the next crossing of the opposite level.
2. Pulses shorter than defined by the maximum value are guaranteed to be filtered (not passed).
3. Pulses in between the max filtered and min unfiltered may or may not be passed through.
4. See the device reference manual for which package pins include glitch filters on the pin input.
5. Pulses larger than defined by the minimum value are guaranteed to not be filtered (passed).

14.9 IRQ

The following table gives the input specifications for the external interrupt pins.

tCYC refers to FIRC_CLK.

For the AE subsystem, tCYC refers to FIRC_AE_CLK.

Table 82. IRQ

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tIPWL	IRQ pulse width low	4	—	—	tCYC	MAXCNT = 3	1
tIPWH	IRQ pulse width high	4	—	—	tCYC	MAXCNT = 3	2

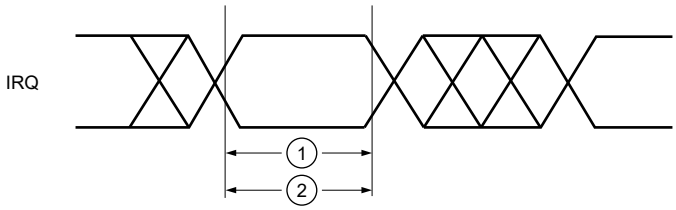


Figure 68. External Interrupt Timing (IRQ)

14.10 Debug

14.10.1 JTAG Boundary Scan

The following table gives the JTAG specifications in boundary scan mode.

The SRE[2:0]=100 is required drive setting to meet the timing.

Table 83. JTAG Boundary Scan

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tJCYC	TCK cycle time [1,2,3]	100	—	—	ns	—	1
tJDC	TCK clock pulse width [1,2]	45	—	55	%	—	2
tTCKRISE	TCK rise/fall time [1,4]	—	—	3	ns	—	3
tTMSS, tTDIS	TMS, TDI data setup time [1,5]	5	—	—	ns	—	4
tTMSH, tTDIH	TMS, TDI data hold time [1,5]	5	—	—	ns	—	5
tTDOV	TCK low to TDO data valid [1,6,7]	—	—	17.5	ns	—	6
tTDOI	TCK low to TDO data invalid [1,6]	0	—	—	ns	—	7
tTDOHZ	TCK low to TDO high impedance [1,6]	—	—	17.5	ns	—	8
tJCMPPW	JCOMP assertion time [1]	100	—	—	ns	—	9
tJCMPS	JCOMP setup time to TCK high [1]	40	—	—	ns	—	10
tBSDV	TCK falling edge to output valid [1,6,8]	—	—	600	ns	—	11
tBSDVZ	TCK falling edge to output valid out of high impedance [1,6]	—	—	600	ns	—	12
tBSDVHZ	TCK falling edge to output high impedance [1,6]	—	—	600	ns	—	13
tBSDST	Boundary scan input valid to TCK rising edge [1]	15	—	—	ns	—	14
tBSDHT	TCK rising edge to boundary scan input invalid [1]	15	—	—	ns	—	15

1. These specifications apply to JTAG boundary scan mode only.
2. TCK pin must have external pull down.
3. JTAG port interface speed only. Does not apply to boundary scan timing.
4. The TCK rise/fall time specification applies to the input clock transition required in order to meet the TDO output specifications that are relative to TCK.
5. Input timing assumes an input signal slew rate of 3ns (20%/80%).
6. Output timing valid for maximum external load CL = 25 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).
7. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
8. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

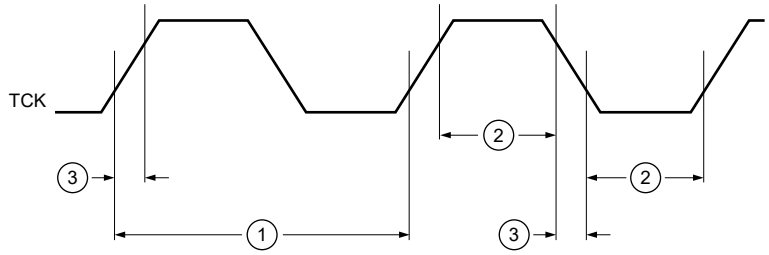


Figure 69. JTAG TCK Input Timing

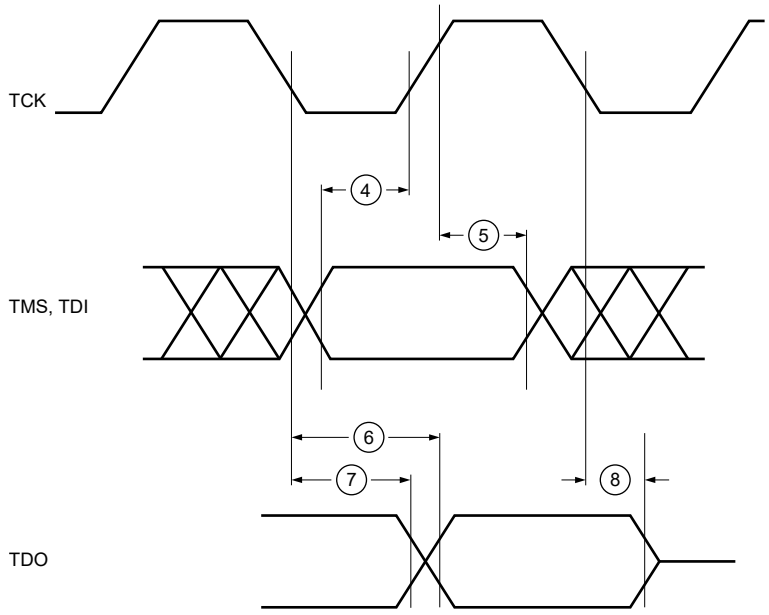


Figure 70. JTAG Test Access Port Timing

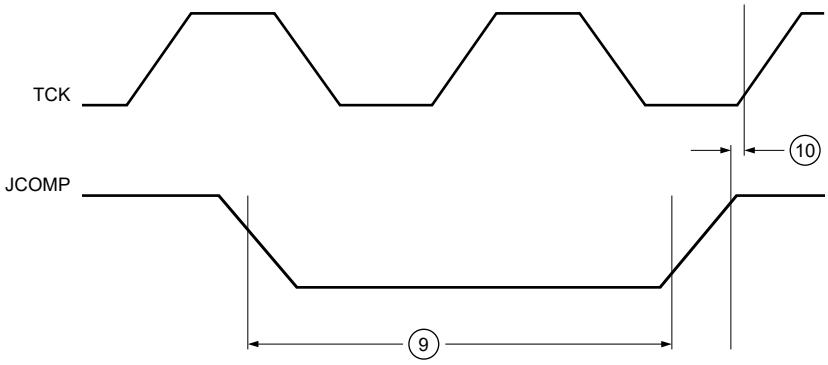


Figure 71. JCOMP Timing

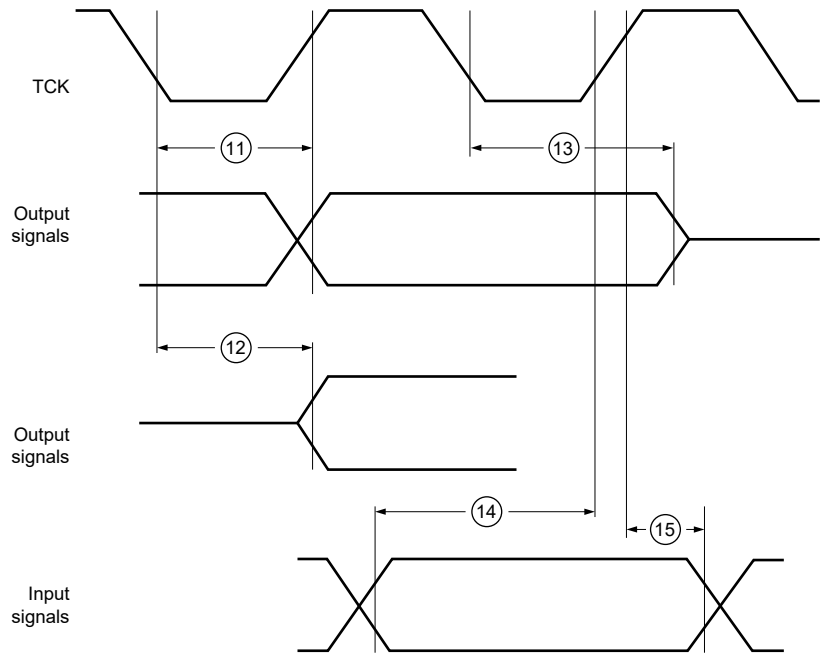


Figure 72. Boundary Scan Timing

14.10.2 AE JTAG boundary scan

The following table gives the JTAG specifications in boundary scan mode for AE subsystem.

The SRE[2:0]=100 is required drive setting to meet the timing.

Table 84. AE JTAG boundary scan

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tJCYC	TCK cycle time [1,2,3]	100	—	—	ns	—	—
tJDC	TCK clock pulse width [1,3]	45	—	55	%	—	—
tTCKRISE	TCK rise/fall time [3,4]	—	—	3	ns	—	—
tTMSS, tTDIS	TMS, TDI data setup time [3,5]	5	—	—	ns	—	—
tTMSH, tTDIH	TMS, TDI data hold time [3,5]	5	—	—	ns	—	—
tTDOV	TCK low to TDO data valid [3,6,7]	—	—	41.5	ns	—	—
tTDOI	TCK low to TDO data invalid [3,6]	0	—	—	ns	—	—
tTDOHZ	TCK low to TDO high impedance [3,6]	—	—	41.5	ns	—	—
tJCMPPW	JCOMP assertion time [3]	100	—	—	ns	—	—

Table continues on the next page...

Table 84. AE JTAG boundary scan...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tJCMPS	JCOMP setup time to TCK high [3]	40	—	—	ns	—	—
tBSDV	TCK falling edge to output valid [3,6,8]	—	—	600	ns	—	—
tBSDVZ	TCK falling edge to output valid out of high impedance [3,6]	—	—	600	ns	—	—
tBSDVHZ	TCK falling edge to output high impedance [3,6]	—	—	600	ns	—	—
tBSDST	Boundary scan input valid to TCK rising edge [3]	15	—	—	ns	—	—
tBSDHT	TCK rising edge to boundary scan input invalid [3]	15	—	—	ns	—	—

1. TCK pin must have external pull down.
2. JTAG port interface speed only. Does not apply to boundary scan timing.
3. These specifications apply to JTAG boundary scan mode only.
4. The TCK rise/fall time specification applies to the input clock transition required in order to meet the TDO output specifications that are relative to TCK.
5. Input timing assumes an input signal slew rate of 3ns (20%/80%).
6. Output timing valid for maximum external load CL = 25pF, which is assumed to be a 10pF load at the end of a 50Ohm, un-terminated, 5 inch microstrip trace on standard FR4 (1.5pF/inch), (25pF total with margin). For best signal integrity, the series resistance of the transmission line should be matched closely to the selected RDSON of the I/O pad output driver.
7. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
8. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

For respective timing diagrams, see section "JTAG Boundary Scan".

14.10.3 JTAG Debug Interface Timing

The following table gives the JTAG specifications in debug interface mode.

Table 85. JTAG Debug Interface Timing

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tTCYC	Absolute minimum TCK cycle time (TDO sampled on posedge of TCK) [1,2]	50	—	—	ns	—	—
tTCYC	Absolute minimum TCK cycle time (TDO sampled on negedge of TCK) [1,2]	25	—	—	ns	—	—

Table continues on the next page...

Table 85. JTAG Debug Interface Timing...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tJDC	TCK clock pulse width	45	—	55	%	—	—
tNTDIS	TDI data setup time [3]	5	—	—	ns	—	11
tNTDIH	TDI data hold time [3]	5	—	—	ns	—	12
tNTMSS	TMS data setup time	5	—	—	ns	—	13
tNTMSH	TMS data hold time	5	—	—	ns	—	14
tNTDOD	TDO propagation delay from falling edge of TCK [4,5]	—	—	17.5	ns	—	15
tNTDOH	TDO hold time with respect to falling edge of TCK [5]	1	—	—	ns	—	16
tTDOHZ	TCK low to TDO high impedance [5]	—	—	17.5	ns	—	—

1. Maximum frequency for TCK is limited to 6MHz during BOOTROM startup of the device, when the system clock is the trimmed 48MHz FIRC.
2. TCK pin must have external pull down.
3. Input timing assumes an input signal slew rate of 3ns (20%/80%).
4. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
5. Output timing valid for maximum external load CL = 25 pF (includes PCB trace, package trace (around 1-2pF) and flash input load).

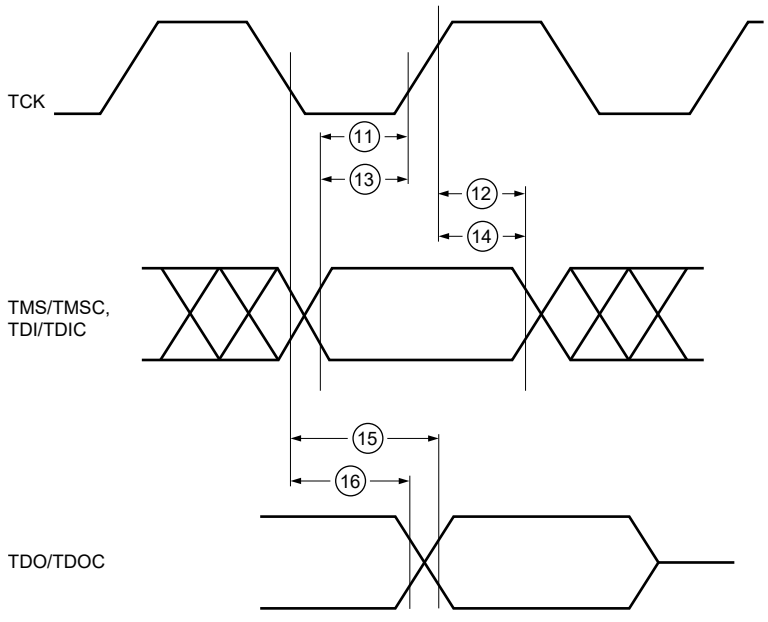


Figure 73. JTAG debug Interface Timing

14.10.4 SWD electrical specifications

The following table gives the Serial Wire Debug specifications for the device.

The following table describes the SWD electrical characteristics. Measurements are with maximum output load of 30pF, input transition of 1ns and pad configured SRE[2:0] =100.

Table 86. SWD electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S1	SWD_CLK frequency	—	—	33	MHz	—	S1
S2	SWD_CLK cycle period	1 / S1	—	—	ns	—	S2
S3	SWD_CLK pulse width	40	—	60	%	—	S3
S4	SWD_CLK rise and fall times	—	—	1	ns	—	S4
S9	SWD_DIO input data setup time to SWD_CLK rise	5	—	—	ns	—	S9
S10	SWD_DIO input data hold time after SWD_CLK rising edge	5	—	—	ns	—	S10
S11	SWD_CLK high to SWD_DIO output data valid	—	—	22	ns	—	S11
S12	SWD_CLK high to SWD_DIO output data hi-Z	—	—	22	ns	—	S12
S13	SWD_CLK high to SWD_DIO output data invalid	0	—	—	ns	—	S13

Timing valid for maximum external load CL = 25pF, which is assumed to be a 10pF load at the end of a 50ohm, un-terminated, 5 inch microstrip trace on standard FR4 (1.5pF/inch), (25pF total with margin). For best signal integrity, the series resistance in the transmission line should be matched closely to the selected RDSON of the I/O pad output.

The SWD_CLK rise/fall time specification applies to the input clock transition required in order to meet the DIO output specifications that are relative to SWD_CLK.

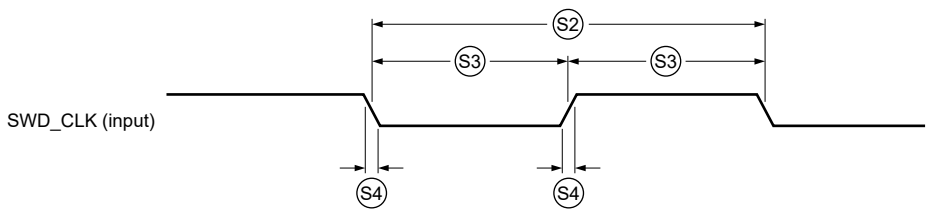


Figure 74. SWD Input Clock Timing

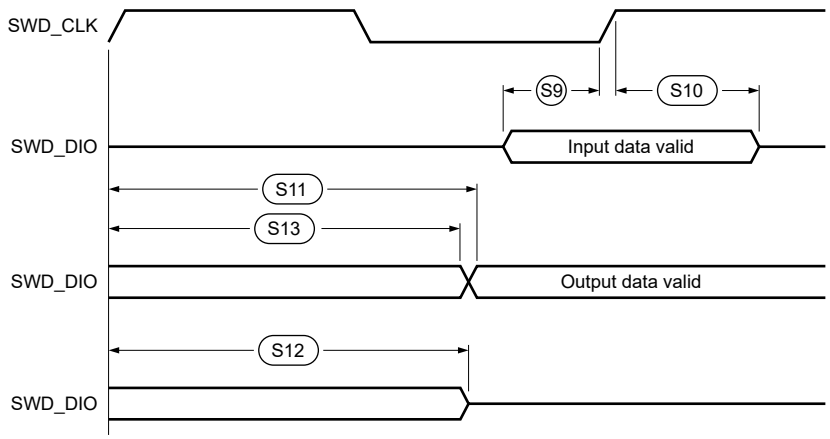


Figure 75. SWD Output Data Timing

15 Ballmaps

For package ballmaps and signal descriptions, see the Reference Manual.

16 Packaging

The following table provides the document number for each package drawing.

If you want the drawing for this package	Then use this document number
27 mm x 27 mm 975-ball MAPBGA	98ASA01799D

NOTE

To find a package drawing, go to http://www.nxp.com and perform a keyword search for the drawing's document number.

17 Revision history

The following tables summarize changes to this document since the release of Rev. 1.

Rev. 5, 3 December 2024
• Changed Max from 160 MHz to 162 MHz for: — fSYS_AE and fSYS_MC in AE Operating Conditions — fP5_AE_CLK in Clock frequency ranges • In Static power specifications for I/O Domains — For both 1.8V and 3.3V Conditions: divided VDD_IO_ETH specifications into separate VDD_IO_ETH_0 and VDD_IO_ETH_1 specifications — For 3.3V Condition: divided VDD_HV_IO_D specifications into separate VDD_HV_IO_D0 and VDD_HV_IO_D1 specifications, and changed Max from 0.3 mA to 0.5 mA

Table continues on the next page...

Rev. 5, 3 December 2024

- Added VDD_HV_IO_D0 and VDD_HV_IO_D1 specifications for 5.0V Condition

- In Power-up, added step "Ramp up all 1.1V supplies."
- In Aurora PLL, for PER_jitter, in Condition text changed "fPLL_CLKIN = 100MHz" to "fPLL_CLKIN = 40MHz | 100MHz"
- Removed section heading for GTM under "Timer Modules"
- In uSDHC SD3.0/eMMC5.1 DDR
  - For first fpp specification
    - In Description, changed "eMMC5.1" to "eMMC high speed"
    - In Condition, added "3.3V/1.8V"
  - For second fpp specification
    - In Description, changed "SD3.0 DDR" to "SD/SDIO DDR50"
    - In Condition, added "1.8V"
- In uSDHC DDR-HS400
  - For fPP: in Condition, added "1.8V"
  - Moved footnote about SD6 and SD7 from tRQ and tRQH specifications for skew (data) to tRQ and tRQH specifications for skew (CMD)
- In uSDHC SD3.0/SDIO3.0/eMMC5.1 SDR
  - For fpp specification with Max value 25/50 MHz and former Description "SD/SDIO full speed/ high speed," divided into two fpp specifications with:
    - Description "SD/SDIO default speed /high speed" and Condition 3.3V
    - Description "SD/SDIO SDR12/ SDR25" and Condition 1.8V

    In shared footnote, changed "normal (full) speed" to "default speed"
  - For fpp specification with former Max value 20/52 MHz
    - In Description, changed "eMMC full speed/ high speed" to "eMMC legacy SDR /high speed DDR"
    - Changed Max to 26/52 MHz
    - In Condition, added "1.8V/3.3V"
    - In second footnote, changed "normal (full) speed" to "Legacy speed" and changed "0–20MHz" to "0–26MHz"
  - For fOD specification with Min value 100 kHz and Max value 400 kHz
    - In Description, changed "identification mode" to "SD/SDIO identification mode" and added footnote about SD/SDIO identification mode
    - In Condition, added "3.3V"
  - For specification with no Min value and Max value 400 kHz
    - Changed symbol from fpp to fOD
    - In Description, changed "low speed" to "eMMC identification mode" and removed footnote about low speed mode

Table continues on the next page...

Rev. 5, 3 December 2024
◦ In Condition, added "1.8V/3.3V" • In uSDHC SDR-HS200, for tCLK, added Condition "1.8V" • In AE SAR ADC — Added second THD specification with Max value -63 dBFS — Added second SINAD specification with Min value 62.5 dBFS

Rev. 4, 22 October 2024
• In Device Power and Operating Current Specifications, replaced IVREFH_ADC with IDD_VREF_DYN and IDD_VREF_LKG • In I3C timing when communicating with Legacy I2C devices and LPI2C — For tfCL and tfDA for FM+, changed Min from 20 * (VDD/5.5V) ns to — — For tfCL and tfDA for FM+, added footnote • In NETC management interface, for tMDKHDX specifications with Condition NEG=0, at end of Max value, changed +3 to +8

Rev. 4 Draft A, 5 October 2024
• In Ordering information, in description of 7th character for Flash memory size, added text: "All S32Z2 devices have 0 MB." • In Absolute Max Ratings — For VAD_INPUT, revised footnote 6 — For V_OS_US_1p6, added footnotes 1 and 4 • In Operating Conditions, for IINJ_LVDS, removed Condition text "LVDS enabled" • In Device Power and Operating Current Specifications, for IDD_HV_LFASTPLL, added Condition text "per PLL" • Added Static power specifications for I/O Domains • In LVDS Pads — For RTERM_LVDS, added Condition text "transmitter and receiver" — For TEYE_LVDS, added Condition text "transmitter" • In Aurora PLL, for fPLL_CLKIN — Changed Min from — to 40 MHz — Changed Typ from 100 MHz to — — Changed Max from — to 100 MHz • In PLL, in introductory text, changed "applies to instances" to "applies to all instances" • In FXOSC, added ΔfXTAL_CLK • In I3C timing when communicating with Legacy I2C devices and LPI2C

Table continues on the next page...

Rev. 4 Draft A, 5 October 2024

- For trCL and trDA for FM, changed Min from 20 ns to —
- For tfCL and tfDA for FM, changed Min from 20 * (VDD/5.5V) ns to —
- For trCL, tfCL, trDA, and tfDA for FM, added footnote

- In Microsecond channel (MSC)
  - For t2 and t3 in table:
    - In Description, changed "SOUT" to "SOUT/SCK"
    - In Condition, removed references to frequency values
    - Added footnote
  - Modified figure "MSC master timing, output only"
- In following sections, in "Output timing valid" footnote, changed "input load" to "flash input load"
  - FlexRay - TxEN
  - FlexRay - TxD
  - NETC MII
  - NETC RMII
  - NETC RGMII
  - PSI5
  - All sections of QuadSPI and uSDHC timing specifications
  - JTAG Boundary Scan
  - JTAG Debug Interface Timing
- In IEEE1588 interface, changed "NETC" to "IEEE" in section and table headings
- In NETC management interface, for tMDKHDX specifications with Condition NEG=1, removed content of Spec Number column
- In SENT Interface, in "Input hysteresis" footnote, changed "set to 1/10th of clock tick to avoid failures" to "set to a value closest to 1/10th of a bit time where the max value of 128 is sufficient for long bit times"
- Removed section heading for PSI5_S under "Communication Modules"
- In following sections, for fSCK, added footnote "fSCK of 133.33MHz is also acceptable"
  - QuadSPI Quad 1.8V SDR 133MHz
  - QuadSPI Quad 3.3V SDR 133MHz
- In QuadSPI Octal 1.8V DDR 200MHz
  - For tOD_DATA, removed Condition text
  - Removed separate tOD_DATA specification for single SRE configuration
- In QuadSPI Quad 3.3V SDR 50MHz, removed "and Octal" from section and table headings
- In uSDHC SD3.0/eMMC5.1 DDR
  - For tTLH and tTHL, added Spec Number

Table continues on the next page...

Rev. 4 Draft A, 5 October 2024
— For tOD, tISU, and tIH, expanded Spec Number information — In footnote 3, changed "Input timing" to "Input signal timing" • In uSDHC DDR-HS400 — Changed introductory text from "In Split SRE configuration SRE[2:0]=000 for Data/CMD and SRE[2:0]=111 for CLK are the required drive settings" to "The SRE[2:0]=000 is required drive setting" — In table: ◦ For tTLH and tTHL, added Spec Number ◦ Added tRQ and tRQH specifications for skew (CMD) ◦ In footnote 5, changed "Input timing" to "Input signal timing" — Modified figure "HS400 Mode Interface Timing" • In uSDHC SD3.0/SDIO3.0/eMMC5.1 SDR, in footnote 6, changed "Input timing" to "Input signal timing" • In uSDHC SDR-HS200 — In table: ◦ For tTLH and tTHL, added Spec Number ◦ In footnote 3, changed "Input timing" to "Input signal timing" — Modified figure "HS200 Mode Interface Timing" • In Flash KGD — For Flash Reads, moved value of 1M array reads from Max to Min — For DR_100 ◦ In Description, changed "after 100" to "between 0 and 100" ◦ Moved value of 20 years from Typ to Min — For DR_1000 ◦ In Description, changed "after 1000" to "between 100 and 1000" ◦ Moved value of 5 years from Typ to Min — For E ◦ Moved value of 100 cycles from Typ to Min ◦ Moved value of 1000 cycles from Max to Typ • In SAR ADC, for IAD_LKG, changed TJ value in Condition text from 125C to 150C • In AE JTAG boundary scan, revised "Output timing valid" footnote • In SWD electrical specifications, revised first paragraph after table

Rev. 3, 04/2024
• In Absolute Max Ratings

Table continues on the next page...

Rev. 3, 04/2024
— For VAD_INPUT, expanded footnote 7 — Added specification: VIN_LVDS — For IINJ_LVDS, revised and expanded footnote 14 • In Operating Conditions — Added specifications: VIN_LVDS and IINJ_LVDS — For ΔVDD_HV_18_IO, added footnotes 15 and 16 — For ΔVDD_HV_18_ANA, added footnote 15 • In AE Operating Conditions, for VIN, changed Max from 3.465V to VDD_HV_IO_D* • In Device Power and Operating Current Specifications, for IVREFH_ADC — Changed Typ from 100 uA to 50 uA — Changed Max from — uA to 115 uA — In Condition text, added "Typ at 25C and Max at 150C" and "1Msps conversion rate" • In GPIO Pads — In footnote 6, changed "1.5pF/inch" to "3.3pF/inch" — In footnote 7, added: "Actual application rise fall times extracted from simulation must meet TR_TF specification." • In LVDS Pads — Removed TSTARTUP_LVDS_REF — For VCM_LVDS_TX that applies to SPI/MSC, changed Min from 1.03 V to 1.05 V — For TSTARTUP_LVDS_TX ◦ In Description, changed "Sleep to normal mode" to "transmitter ready after enabling" ◦ Changed Max from 500 ns to 1.5 us ◦ In Condition, added "Includes reference startup time" — For VCM_LVDS_RX ◦ Added footnote ◦ Changed Min from 0.2 V to 0.225 V ◦ Changed Max from (VDD_HV_IO_LFAST - 0.2) V to (VDD_HV_IO_LFAST - 0.225) V — For VDIFF_LVDS_RX, added footnote: "The LVDS input pin maximum voltage given in the operating conditions section of the datasheet must be obeyed when setting the common-mode and differential swing voltages seen by the LVDS receiver." — For TSTARTUP_LVDS_RX ◦ In Description, changed "Power down to Normal mode" to "receiver ready after enabling" ◦ In Condition, changed "bandgap" to "reference startup" — Added figure "VDIFF_LVDS_TX pk-pk in single ended and differential mode" • In LPI2C, added specifications: tSU_STA, tHD_STA, tLOW, tDIG_L, tHIGH, tDIG_H, tSU_DAT, tHD_DAT, trCL, tfCL, trDA, tfDA, tSU_STO, and tBUF

Table continues on the next page...

Rev. 3, 04/2024

- In SPI, revised footnote 9
- In Microsecond channel (MSC), revised Descriptions
  - For t1, changed "Duty cycle deviation" to "SCK duty cycle deviation"
  - For t2, changed "Rise time" to "SOUT rise time"
  - For t3, changed "Fall time" to "SOUT fall time"
- In FlexRay - TxEN and FlexRay - TxD, revised footnote 1
- In NETC MII and NETC RMII, revised footnote 2
- In NETC RGMII, revised footnote 3
- In NETC management interface, modified tMDKHDX specifications
- Added CANXL
- In PSI5, revised footnote 2
- Revised "Output timing valid" footnote in
  - QuadSPI Quad 1.8V DDR 80MHz (footnote 2)
  - QuadSPI Quad 1.8V SDR 133MHz (footnote 1)
  - QuadSPI Octal 1.8V SDR 133MHz (footnote 2)
  - QuadSPI Octal 1.8V DDR 166MHz (footnote 1)
  - QuadSPI Octal 1.8V DDR 200MHz (footnote 1)
  - QuadSPI Quad 3.3V DDR 80MHz (footnote 2)
  - QuadSPI Quad 3.3V SDR 133MHz (footnote 1)
  - QuadSPI Octal and HyperRAM 3.3V DDR 100MHz (footnote 1)
- In QuadSPI configurations, removed table columns with DQS mode defined as "Internal pad loopback (data + DQS)" and "Edge-aligned" for:
  - QuadSPI_0 side A: 1.8V Octal, DDR 200 MHz
  - QuadSPI_1 side A: 1.8V HyperFlash or HyperRAM, DDR 166 MHz
- In uSDHC SD3.0/eMMC5.1 DDR, revised footnote 1
- In uSDHC DDR-HS400
  - Revised footnote 1
  - For tCL and tCH, changed Min from 2.35 ns to 2.2 ns
  - For tOD, changed Max from 0.9 ns to 0.6 ns
- In uSDHC SD3.0/SDIO3.0/eMMC5.1 SDR, revised footnote 2
- In uSDHC SDR-HS200, revised footnote 1
- In JTAG Boundary Scan, revised footnote 6
- In AE JTAG boundary scan, revised footnote 7
- In JTAG Debug Interface Timing, revised footnote 4
- In SWD electrical specifications, revised first paragraph after table

Rev. 3 Drafts A and B, 10/2023

- Changed I3C protocol to I2C protocol, changed number of I3C instances from 3 to 1, and added LPI2C instances in:
  - Block diagram
  - Table 1 in Feature summary
- In Ordering information, changed production part number and redefined 11th and 12th characters
- In Device Power and Operating Current Specifications, changed Typ for IVREFH_ADC from 0.65 mA to 100 uA
- In Total power specifications, changed Symbol for both total dynamic power specifications from PVDD_DOMAIN1 to PDYN_DOMAIN1
- In GPIO Pads, removed IOH_33 specification with Condition of SRE[2:0]=000
- In LVDS Pads
  - Added IDD_HV_LVDS_REF
  - For VCM_LVDS_TX with Condition for SPI/MSC, changed Min from 1.075 V to 1.03 V and Max from 1.325 V to 1.37 V
  - For TSTARTUP_LVDS_TX, changed Description text from "assertion of ipp_obe to common mode settling time" to "Sleep to normal mode"
  - For TEYE_LVDS, added to Condition text: "includes PLL jitter"
  - For TSTARTUP_LVDS_RX, added Description text "Power down to normal mode" and added Condition text "Includes bandgap time"
  - Added CIN
  - Added "LFAST timing definition" figure
- In LFAST PLL, added new footnote for tLOCK
- Added introductory text in I3C
- In I3C timing when communicating with Legacy I2C devices
  - Added Min and Max values for both tHD_DAT specifications
  - Removed "I3C START timing" figure
  - Added "Definition of timing for F/S mode devices on the I2C bus" figure
- Added LPI2C
- In SPI, moved SRE[2:0] = 101 from Condition for all tSUO and tHO specifications to initial paragraph
- In Microsecond channel (MSC), added t1, t2, and t3 specifications
- In LIN
  - For RATE with Condition of UART mode, changed Max from 2 Mbps to 33 Mbps
  - Moved SRE[2:0] = 110 from Condition for RATE specifications to initial paragraph
- In NETC MII, moved SRE[2:0] = 100 from Condition for final three specifications to initial paragraph
- In NETC RMII, moved SRE[2:0] = 100 from Condition for final two specifications to initial paragraph
- In NETC RGMII, moved SRE[2:0] = 100 from Condition for all specifications to initial paragraph
- In NETC management interface

Table continues on the next page...

Rev. 3 Drafts A and B, 10/2023
— For existing tMDKHDX, removed footnote, redefined Min and Max, and added Condition text NEG=1 — Added two more tMDKHDX specifications • In QuadSPI interfaces, added hyperlinks to applicable sections of specifications • In QuadSPI Octal 1.8V SDR 133MHz, removed tISU_SCK and tIH_SCK • In QuadSPI Octal 1.8V DDR 166MHz, QuadSPI Octal 1.8V DDR 200MHz, and QuadSPI Octal and HyperRAM 3.3V DDR 100MHz, removed tDVW • Added QuadSPI configurations

Rev. 2, 06/2023
• In AE Operating Conditions, for VDD_HV_REG — Changed Min from 1.62 V to 1.68 V — Changed Max from 1.98 V to 1.92 V • In Device Power and Operating Current Specifications — Removed PVDD_SOC_BASE_TYP — Added PLKG_SOC_TYP and PDYN_SOC_BASE_TYP — For PDYN_R52_TYP at 800 MHz, changed Typ from 1.95 W to 0.8 W — Added PDYN_R52_TYP at 900 MHz and 1 GHz — For PDYN_DDR_TYP, changed Typ from TBD to 0.1 W and, in Condition, changed VDD_DDR from 0.77 V to 0.825 V and 32-bit to 16-bit — For PDYN_LLCE_TYP, changed Typ from TBD to 0.2 W and, in Condition, changed 200 MHz to 400 MHz — In Condition for IVDD_IO_ETH_0 and IVDD_IO_ETH_1 at both 3.3 V and 1.8 V, removed SRE=4 and VDD=3.3 V and added Tj=150C and RGMII 125 MHz — Removed pre-existing IVDD_IO_QSPI_0 and IVDD_IO_QSPI_1 specifications — Changed PVDD_IO_QSPI_0 and PVDD_IO_QSPI_1 to IVDD_IO_ETH_0 and IVDD_IO_ETH_1, respectively — For new IVDD_IO_QSPI_0, changed Max from TBD to 35 mA and, in Condition, changed max drive to Octal mode, DDR — For new IVDD_IO_QSPI_1 at 1.8 V, changed Max from TBD to 80 mA and, in Condition, changed max drive to Octal mode, DDR — For new IVDD_IO_QSPI_1 for QuadSPI_1 A at 3.3 V, changed Max from TBD to 130 mA and, in Condition, changed 133 MHz / max drive to 100 MHz Octal mode, DDR — For new IVDD_IO_QSPI_1 for QuadSPI_1 B at 3.3 V, changed Max from TBD to 75 mA and, in Condition, changed max drive to Quad mode, SDR — Changed footnote 1

Table continues on the next page...

Rev. 2, 06/2023

- from: "SoC logic power consumption includes total SoC leakage power plus the dynamic power for basic configuration blocks like clocking and other infrastructure blocks. Please contact NXP Semiconductor for leakage power and temperature values for the device."
- to: "Base dynamic power includes SMU, HSE, DMA, peripherals, and clocks. It excludes RTU and FlexLLCE clocks and domains."

— In footnote 2, changed "four Cortex-R52 cores" to "eight Cortex-R52 cores" and added: "RTU0 and RTU1 each account for half the spec value."

— Added new footnote 3: "Power includes MC_CGM_6 clocking current at 400MHz plus DDR access current and excludes IO_DDR."

— In footnote 4, changed "based on simulation of the expected average logic activity within the FlexLLCE" to "includes FlexLLCE subsystem clocks and peripherals plus all cores running Dhrystone."

- In Total power specifications, reversed the positions of footnotes 1 and 3
- In AE Device Power and Operating Current Specifications, for PVDD12, changed Max from 100 mW to 200 mW
- In Power-down, added table
- In LVDS Pads
  - — In introductory paragraph, added "MSC, SPI and Zipwire"
  - — For pre-existing VCM_LVDS_TX, added Condition: "Applies to Aurora, CLKOUT LVDS TX and Zipwire"
  - — Added second VCM_LVDS_TX with Condition: "Applies to SPI/MSC"
  - — For VDIFF_LVDS_RX, changed Max from 400 mW to 450 mW
  - — Removed footnote: "When measuring leakage with Rx enabled, when we drive both pad_p and pad_n high, an internal pull down resistor is enabled to ground and will show upto 100uA leakage on each pin"
- In PLL changed "System PLL" to "PLL" for tLOCK, PER_jitter, LT_jitter, and footnote 3
- In FXOSC, for TCST, added to Condition: "time to stable duty cycle when EOCV is set to 1 ms period"
- In NETC MII, for ΔtCYC_TX
  - — Changed Min from 45% to 35%
  - — Changed Max from 55% to 65%
- In NETC management interface
  - — For tMDKHDX, in Spec Number, added MDC10, MDC11
  - — For MDIO_ISU, in Spec Number, added MDC12
  - — In footnote 1, added: "If NEG=1, then MDIO is driven with the negedge of MDC, and the other fields don't affect the timing. If NEG=0 and EHOLD=0, then the delay from MDC to MDIO is 2*MDIO_HOLD+1 NETC cycles. If NEG=1 and EHOLD=1, then the delay from MDC to MDIO is 8*MDIO_HOLD+1 NETC cycles."
- In all sections of QuadSPI specifications, in introductory text, changed paragraph beginning "Clock measurements..." to: "Data transitions measured at 30%/70% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply."
- In QuadSPI Octal 1.8V DDR 166MHz
  - — For tIH_DQS, changed Min from 2.145 ns to 2.105 ns

Table continues on the next page...

Rev. 2, 06/2023
— For tISU_DQS, changed Min from -0.496 ns to -0.616 ns • In QuadSPI Octal 1.8V DDR 200MHz — For pre-existing tOD_DATA, added to Condition: "Split SRE configuration, SRE[2:0]=000 for Data and SRE[2:0]=110 for CLK" — Added second tOD_DATA — For tIH_DQS, changed Min from 1.684 ns to 1.644 ns — For tISU_DQS, changed Min from -0.466 ns to -0.586 ns • Added QuadSPI timing diagrams • In all sections of uSDHC specifications, in introductory text, changed paragraph beginning "All uSDHC parameters..." to: "Data transitions measured at 35%/65% supply for the write path. Data transitions measured at mid-supply for the read path. Clock transitions measured at mid-supply." • In uSDHC DDR-HS400 — In introductory text, changed paragraph beginning "The SRE[2:0]..." to: "In Split SRE configuration SRE[2:0]=000 for Data/CMD and SRE[2:0]=111 for CLK are the required drive settings to meet the timing." — For tCL and tCH, changed Min from 2.2 ns to 2.35 ns — For tOD1 and tOD2, changed Min from 0.45 ns to 0.65 ns — Added tOD — Removed footnote: "The CMD output timing for HS400 mode is the same as CMD output timing for HS200 mode."

Rev. 2 Draft C, 02/2023
• In Ordering information, for 12th character, changed "0 = Initial version" to "A = Initial production version" • In Total power specifications — Changed introductory text to: "The part is designed with a power distribution network that has two specifications: dynamic power and total supply rail power (dynamic power plus leakage power). At higher temperatures, the leakage is higher and the user must manage the dynamic power to compensate. The user must ensure the total supply rail power is below the total power distribution network capacity. At lower temperatures, the leakage is reduced and the part can utilize the full dynamic power capacity. Exceeding either power specifications will result in IR drop issues and unpredictable operation of the device." — Replaced two footnotes in table with three new footnotes — For specification with Max value 5.2, removed from Condition text: "temperature range classification M" — For specification with Max value 4.8 (formerly 3.9), removed from Condition text: "temperature range classification V" — Added specification with Max value 2.0 — For specification with Max value 2.8: in Condition text, changed "temperature independent" to "Tj=125C" • In GPIO Pads — For TR_TF_33 with Condition text SRE[2:0] = 100, changed Min from 1.75 to 1.9

Table continues on the next page...

Rev. 2 Draft C, 02/2023

- For TR_TF_33 with Condition text SRE[2:0] = 101, changed Min from 0.05 to 1.00 and Max from 8.25 to 8.50
- For TR_TF_33 with Condition text SRE[2:0] = 110, changed Min from 0.01 to 0.50 and Max from 7.0 to 7.30
- For TR_TF_33 with Condition text SRE[2:0] = 111, changed Min from 0.005 to 0.40 and Max from 5.5 to 6.0

- Added I3C timing when communicating with Legacy I2C devices and Flash KGD
- In SENT Interface, added new final sentence to footnote 4: "SRX programmable filter should be set to 1/10th of clock tick to avoid failures."
- In QuadSPI Quad 3.3V SDR 50MHz, added tISU_SCK and tIH_SCK specifications
- In Temperature Monitoring Unit (TMU) for TRANGE
  - Changed Min from -40°C to -45°C
  - Changed Max from 150°C to 155°C
  - Added footnote: "Accuracy outside of operating range (-40 to 150) is not guaranteed."
- In second paragraph of SAR ADC, changed "the external capacitance at the input pin should be maximized" to "the external capacitance at the input pin and reference pin should be maximized"

Rev. 2 Draft B, 12/2022

- In Overview, changed "microcontrollers (MCUs)" to "real-time processors"
- In Absolute Max Ratings
  - For VIN, added footnote about DC case limit
  - For existing V_OS_US_* specifications, added "3.3V" to Condition text
  - Added new V_OS_US_10 specification for 1.8V
- In Operating Conditions
  - For fSYS_R52, changed Max from 800 MHz to 1 GHz and added Condition text and related footnote
  - For both VDD_IO_ETH_n specifications, added Condition text
  - For VIN_33 and VIN_18, added footnote about DC case limit
  - For ΔVDD_HV_18_ANA, added footnote about VREFH_ADCn
  - Added "ADC supply sequencing" diagram
- In Device Power and Operating Current Specifications, added PVDD_IO_QSPI_0 and PVDD_IO_QSPI_1 specifications
- Moved content of "Power Sequencing" section into Power-up subsection, added table in Power-up subsection, and added Power-down subsection
- In Reset related pad electrical characteristics, after "RESET_B pad detailed behavior" diagram, added text: "The RESET_B pad behavior described in the diagram and the related VRSE_RESET_B parameter spec also apply to the case of core VDD droop after power-up."
- In Reset Duration, added diagrams:
  - Reset_b pad detailed behavior during core supply brownout

Table continues on the next page...

Rev. 2 Draft B, 12/2022

- Reset_b pad detailed behavior during pad HV supply brownout
- Reset_b pad detailed behavior during power down

- In Clock frequency ranges
  - For fP0_PSI5_189K_CLK. changed Max from 6.048 MHz to 6.0606 MHz
  - For fRTU0_CORE_CLK and fRTU1_CORE_CLK, changed Max from 900 MHz to 1 GHz, expanded Condition text, and added related footnote
  - For fRTU0_CORE_DIV2_CLK and fRTU1_CORE_DIV2_CLK, changed Max from 450 MHz to 500 MHz, expanded Condition text, and added related footnote
- In PLL
  - For fPLL_CORE_PHI0, changed Max from 900 MHz to 1000 MHz, expanded Condition text, and added footnote
  - For fPLL_DDR_PHI0
    - Removed single specification with Min of 800 MHz and Max of 1620 MHz
    - Added four specifications with varying Condition text and footnotes, each with a single value for both Min and Max: 266 MHz, 333 MHz, 400 MHz, and 405 MHz
- In DFS
  - For fDFS_CORE_CLK0, changed Max from 900 MHz to 1000 MHz, expanded Condition text, and added footnote
  - For fDFS_PER_CLK5, changed Max from 333 MHz to 330 MHz
- In Microsecond channel (MSC)
  - Removed Note and tCSC and tASC specifications
  - Added tCSV and tCSH specifications as well as diagram
  - For tSUO, changed 6 ns value from Min to Max
- Removed "I3C Push-Pull Timing Parameters for SDR Mode" section
- Added CAN
- In IEEE1588 interface, removed tT1588OV specification
- For QuadSPI, removed tISU_SCK and tIH_SCK specifications from
  - QuadSPI Quad 1.8V DDR 80MHz
  - QuadSPI Quad 1.8V SDR 133MHz
  - QuadSPI Octal 1.8V SDR 133MHz
  - QuadSPI Quad 3.3V SDR 133MHz
- In uSDHC SD3.0/eMMC5.1 DDR, renamed section (was "uSDHC DDR-52MHz") and figure, and added text preceding table: "All uSDHC parameters are measured at mid-supply (VDD_IO_SDHC/2)."
- In uSDHC DDR-HS400, removed "HS400 mode uSDHC output timing" and "HS400 mode uSDHC input timing" diagrams, and added text preceding table: "All uSDHC parameters are measured at mid-supply (VDD_IO_SDHC/2)."
- In uSDHC SD3.0/SDIO3.0/eMMC5.1 SDR, renamed section (was "uSDHC SDR-52MHz") and figure, and added text preceding table: "All uSDHC parameters are measured at mid-supply (VDD_IO_SDHC/2)."
- In uSDHC SDR-HS200, added text preceding table: "All uSDHC parameters are measured at mid-supply (VDD_IO_SDHC/2)."

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- Throughout: Changed S32E27 to S32E2, changed S32Z27 to S32Z2, and removed references to S32S27
- In "Block diagram" section figure, in "Math/ML acceleration" block: Removed "CEVA_SPF2" and changed "Vector DSP" to "FP Vector DSP"
- In "Feature summary" section text: For GTM list item, changed "on S32E27 and optional for S32Z27" to "optional for both S32E2 and S32Z2"
- Modified table in "Feature summary" section
- Modified figure in "Ordering information" section
- In "Absolute Max Ratings" section:
  - For VAD_INPUT: Changed VREFL_ADC to VSS_ADC and VREFH_ADC to VDD_ANA
  - Added IINJ_LVDS
  - For final four parameters, added symbol names: V_OS_US_10, V_OS_US_7p5, V_OS_US_2p5, and V_OS_US_1p6
  - In footnote 8: Added "For powered devices when VIN ≥ VDD_IO*, VIN must simultaneously follow the constraint that VIN-VDD_IO* ≤ 0.3V."
  - In footnote 9: Added "Unpowered devices must simultaneously follow IINJ_D unpowered current injection constraints."
  - Added new footnotes 12 and 15
- In "Operating Conditions" section:
  - For VAD_INPUT: Changed VREFL_ADC to VSS_ADC and VREFH_ADC to VDD_ANA
  - For existing IINJ_D parameter: Added condition "Unpowered"
  - Added IINJ_D parameter with condition "Powered"
  - In footnote 2: Changed "the modulation depth (max 1.5%)" to "half the modulation depth"
  - In footnote 8: Added "See device hardware design guidelines document for more details."
  - Changed footnote 9 from "Additional +0.3V are supported for DC signal" to "For AC signals, allowed max VIN ≤ VDD_IO* for lifetime operation. If AC overshoot beyond VDD_IO* occurs, then refer to the Abs Max duration constraints as a function of the amount of overshoot. For DC signals ≥ VDD_IO, VIN-VDD_IO* ≤ 0.3V is allowed for lifetime operation."
  - Changed footnote 10 from "Absolute minimum level for VIN signal is -0.3V" to "The min DC VIN level for a powered device is -0.3V. If AC undershoot below -0.3V occurs, then refer to the Abs Max duration constraints as a function of the amount of undershoot."
  - Added new footnote 15
- In "Thermal Design, Characteristics, and Ratings" section: Expanded text and, in table, revised descriptions and footnotes
- In "Device Power and Operating Current Specifications" section: Added footnotes and, for IVREFH_ADC, changed unit from uA to mA
- In "GPIO Pads" section:
  - Added VOL and VOH and new footnote 1

Table continues on the next page...

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— Removed Note: "VOH/VOL values should be calculated based on the provided RDSON, IOH/IOL values and IBIS models."

— In "1.8V/3.3V GPIO pad detailed behavior during power up" figure: Changed "weak pull-down" to "weak pull-down as per ILKG_3318 specification"

— Removed text: "The weak pull-down is 100 Kohm and is separate from the usual selectable 12Kohm internal pull resistor. If the pad is in 3.3V mode and the IOMUX sheet defines the 'Pad State During POR reset sequence' as 'Hi-Z', the 100Kohm pull-down remains engaged until RESET_B is released."

- In "Clock frequency ranges" section, added text after table: "The stated maximum operating frequency must be observed when using the PLL with frequency modulation enabled. Center-spread modulation is supported in cases where the nominal operating frequency plus half the modulation depth is less than the stated maximum frequency."
- In "PLL" section:
  — Moved text from after table to before table: "Spread spectrum clock modulation is only available on the Core PLL and DDR reference PLLs."
  — In table: Changed Min to 40 MHz for fPLL_CORE_PHI0, fPLL_PER_PHI0, fPLL_PER_PHI1, fPLL_PER_PHI2, fPLL_PER_PHI3, fPLL_PER_PHI4, fPLL_PER_PHI5, and fPLL_PER_PHI6
- In "DFS" section:
  — In table: Changed Min to 40 MHz for fDFS_CORE_CLK0, fDFS_CORE_CLK1, fDFS_CORE_CLK2, fDFS_CORE_CLK3, fDFS_CORE_CLK4, fDFS_CORE_CLK5, fDFS_PER_CLK0, fDFS_PER_CLK1, fDFS_PER_CLK2, fDFS_PER_CLK3, fDFS_PER_CLK4, and fDFS_PER_CLK5
  — Added PER_Jitter with condition fDFS_CLKIN = 2400 MHz, Odd MFN
- In "SIRC" section:
  — For PTA: Changed description from "Post Trim Accuracy" to "Trimming Resolution"
  — For ðfVAR: Changed condition from "Trimmed" to "Frequency variation across voltage and temperature range after trimming"
- In "uSDHC DDR-HS400" section:
  — For "Clock frequency" parameter: Changed symbol from tPP to fPP
  — Changed tOD parameter to tOD1 and modified characteristics
  — Removed tISU and tIH parameters and added tOD2, tRQ, and tRQH parameters
- In "SAR ADC" section: For VAD_INPUT, changed VREFL_ADC to VSS_ADC and VREFH_ADC to VDD_ANA
- Added "Microsecond channel (MSC)" section
- Added "QuadSPI Octal 3.3V SDR 50MHz" section
- In "DDR" section: Added "This chip supports the following memory types..."

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