



MC33FS5502Y3KS

Configuration report for FS5502 OTP program ID: Y3

Rev 1.0 — 16 August 2024

Report

1 General description

The FS5502 is an automotive high voltage multi-output power supply integrated circuit, with focus on Radio, Radar, V2X and Infotainment applications. It includes multiple switch mode and linear voltage regulators. It offers external frequency synchronization input and output, for optimized system EMC performance.

Several device versions are available, offering choice in number of output rails, output voltage setting, operating frequency and power up sequencing, to address multiple applications.

Note: All parametric information is maintained in FS5502 datasheet

2 Features and benefits

- 60 V DC maximum input voltage for 12 V and 24 V applications
- VPRE synchronous buck controller with external MOSFETs. Configurable output voltage, switching frequency, and current capability up to 10 A peak.
- Low voltage integrated synchronous BUCK1 converter, dedicated to MCU core supply with SVS capability. Configurable output voltage and current capability up to 3.6 A peak.
- Low voltage integrated synchronous BUCK3 converter. Configurable output voltage and current capability up to 3.6 A peak.
- EMC optimization techniques including SMPS frequency synchronization, spread spectrum, slew rate control, manual frequency tuning
- One linear voltage regulator for MCU IOs and ADC supply, external physical layer. Configurable output voltage and current capability up to 400 mA DC.
- OFF mode with very low sleep current (10 μ A typ)
- 2x input pins for wake-up detection and battery voltage sensing
- Device control via I2C interface with CRC
- Three voltage monitoring circuits, dedicated interface for MCU monitoring, power good, reset and interrupt outputs
- Configuration by OTP programming. Prototype enablement to support custom setting during project development in engineering mode.



3 Applications

- Radio
- Radar
- V2x
- Infotainment

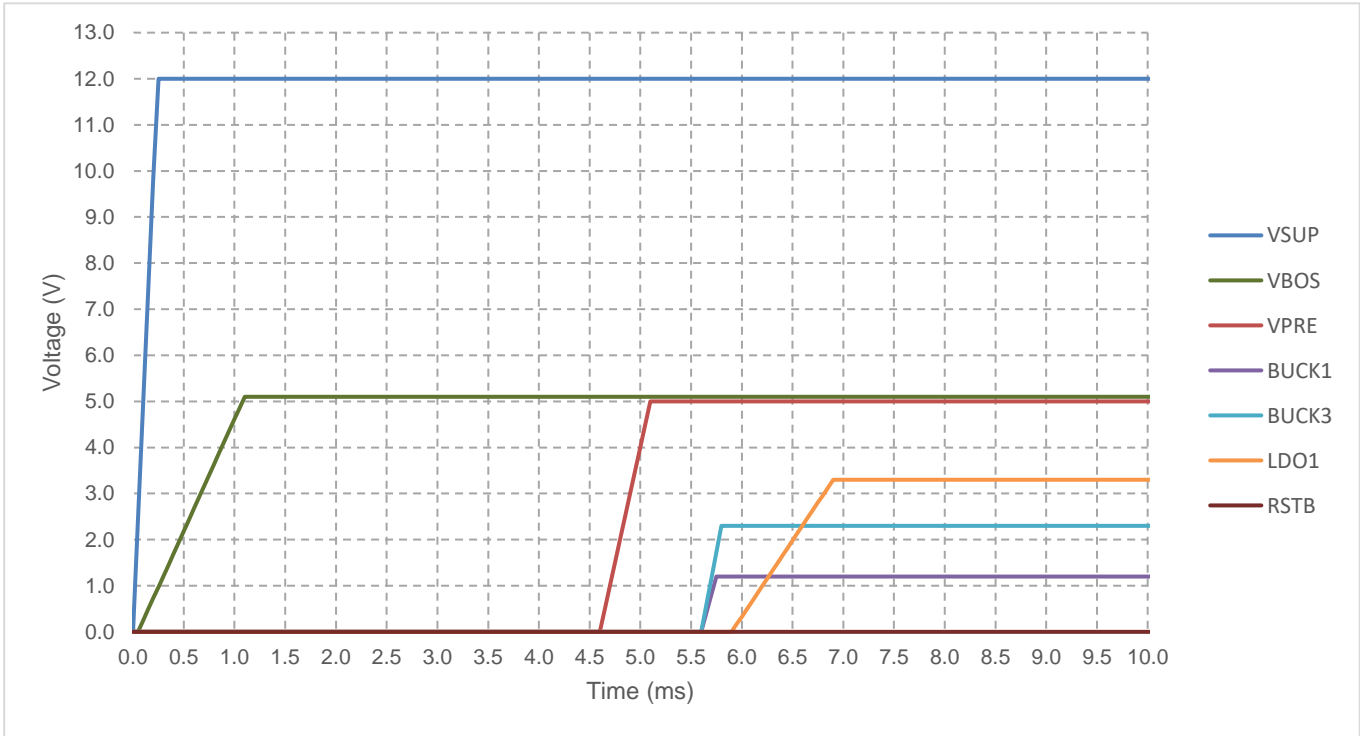
4 Ordering information

Table 1. Ordering Information

Type number ^[1]	Package		
	Name	Description	Version
MC33FS5502Y3ES	HVQFN56	HVQFN56, plastic, thermally enhanced very thin quad; flat non-leaded package, wettable flanks; 56 terminals; 0.5 mm pitch; 8 mm x 8 mm x 0.85 mm body	SOT684-23

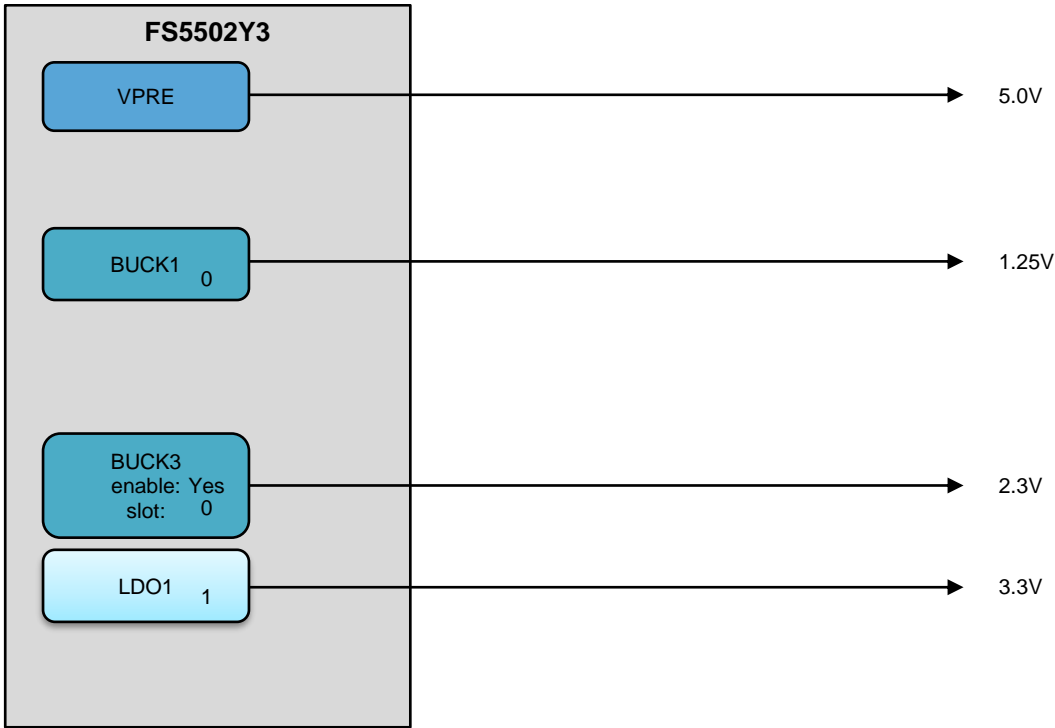
[1] To order parts in tape and reel, add the R2 suffix to the part number.

5 Power up sequence summary



Note: VBOS is set at 5.1 V and RSTB at 3.2 V or 4.9 V to differentiate from regulators on the graph

6 Hardware configuration diagram



7 OTP configuration

Table 2. Main OTP configuration

Functional block	Feature	OTP selection
VPRE	Output voltage	5.0V
	Slope compensation	70mV/μs
	Current limitation	80mV
	High Side slew rate	PU/PD/900mA
	Low Side slew rate	PU/PD/900mA
	Switching frequency	455KHz
	Phase shifting	delay 0
	Turn OFF delay	250μs
	VPRE mode	Force PWM

Table 2. Main OTP configuration (continued)

Functional block	Feature	OTP selection
BUCK1	Output voltage	1.25V
	Inductor	1μH
	Current limitation	2.6A
	Compensation network	65 GM

	Switching frequency	2.22MHz
	Phase shifting	delay 4
	Behavior in case of TSD	BUCK1 Shutdown
	Power sequencing slot	Regulator Start and Stop in Slot 0
	Soft start ramp	7.81mV/μs
BUCK3	Enabled	Yes
	Output voltage	2.3V
	Inductor	1μH
	Current limitation	4.5A
	Compensation resistor	Default
	Gain control	Default
	Switching frequency	2.22MHz
	Phase shifting	delay 0
	Behavior in case of TSD	BUCK3 Shutdown
	Power sequencing slot	Regulator Start and Stop in Slot
	Soft start ramp	10.41mV/μs
LDO1	Output voltage	3.3V
	Current limitation	400mA
	Behavior in case of TSD	LDO1 Shutdown
	Power sequencing slot	Regulator Start and Stop in Slot
Miscellaneous	Power up/down slot duration	250μs
	PSYNC	Disabled
	PLL enabled	Yes
	Deep Fail Safe (autoretry)	Infinite
	VSUP power-up threshold	4.9V for Vpre < 4.5V
	Regulator assigned to VDDIO	LDO1
	I2C address	0x20
	Device ID	00000001

Table 3. Fail-safe OTP configuration

Functional block	Feature	OTP selection
VCOREMON	Monitoring Voltage	1.25V
	OVTH	112%
	UVTH	88%
	OV_DGLT	45μs
	UV_DGLT	25μs
	SVS_CLAMP	No SVS
VDDIOMON	Monitoring Voltage	3.3V
	OVTH	112%
	UVTH	88%

	OV_DGLT	45µs
	UV_DGLT	25µs
VMON1	OVTH	112%
	UVTH	88%
	OV_DGLT	45µs
	UV_DGLT	25µs
PGOOD	VCOREMON	Yes
	VDDIOMON	Yes
	VMON1	No
	RSTB	Yes
VMON1 Enable	VMON1	No
I2C	I2C address	0x21

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Date of release: 16 August 2024
Document identifier: R_FS5502Y3