PF9453

Power management IC for i.MX 91

Rev. 1.1 — 23 April 2025 Objective short data sheet

1 General description

The PF9453 is a single chip power management IC (PMIC) designed for the i.MX 91 processor. It provides power supply solutions for IoT, smart appliance, and portable applications where size and efficiency are critical.

The device provides four high-efficiency step-down regulators, three LDOs, one 400 mA load switch, and a 32.768 kHz crystal oscillator driver. One buck regulator supports dynamic voltage scaling (DVS) along with programmable ramping up and down time. This device, is characterized across -40 °C to 105 °C ambient temperature range for the HVQFN40 package, making it a option for the industrial, extended industrial, and consumer markets. In the case of WLCSP36, the package is characterized as -40 °C to 85 °C. The four step-down regulators are designed to provide power for the i.MX 91 processor and the associated dynamic random access memory (DRAM). One always-on LDO is for the secure nonvolatile storage (SNVS) core power supply, and two LDOs are supposed to supply power to processor and peripheral devices. One 400 mA load switch supplies 3.3 V power to an SD card. The SD card has an internal discharge resistor used to discharge the electric charge stored in the output when the equipment is turned off, for safety reasons.

The PF9453 is offered in two packages: 40-pin HVQFN package, 5 mm x 5 mm, 0.4 mm pitch, and 36-bump wafer-level CSP package, 2.48 mm x 2.48 mm, 0.4 mm pitch.

2 Features and benefits

- Four buck regulators
  - BUCK1: 0.6 V to 3.775 V, 25 mV step, 2000 mA[1]
  - BUCK2: 0.6 V to 2.1875 V, 12.5 mV step, 2700 mA[1]
  - BUCK3: 0.6 V to 3.775 V, 25 mV step, 2000 mA[1]
  - BUCK4: 0.6 V to 3.775 V, 25 mV step, 2500 mA[1]
  - Dynamic voltage scaling on BUCK2
  - Monitor fault condition
- Three linear regulators
  - LDO_SNVS, always-on, 1.2 V to 3.4 V with 25 mV step, 10 mA
  - LDO1 with 25 mV step, 250 mA, voltage selection through SD_VSEL Pin
  - LDO2, 0.5 V to 1.95 V with 25 mV step, 200 mA (only available in QFN Package)
  - Built-in active discharge resistor
- One 400 mA load switch with a built-in active discharge resistor and GPIO/I^{2}C control, multiplexed with a DBUS debounce filter
- 32.768 kHz crystal oscillator driver and buffer output
- Power control I/O
  - Power ON/OFF control
  - Standby/Run mode control
  - Watchdog reset input
- Flexible power ON/OFF sequence, one time programmable (OTP) device configuration
- Built-in active discharge resistor

1 Output current of PF9453 regulators changes depending on the part number; please refer to Table 1

- Fm+ 1 MHz I^2C Interface
- ESD protection
  - Human body model (HBM) : ±2000 V
  - Charged device model (CDM) : ±500 V
- Available in:
  - WLCSP36 (36 bumps in 6x6 array, 2.48 mm x 2.48 mm, 0.4 mm pitch)
  - HVQFN40 (40-pins, 5 mm x 5 mm, 0.4 mm pitch)

3 Applications

- IoT devices
- White goods appliances
- Industrial applications
- Portable devices

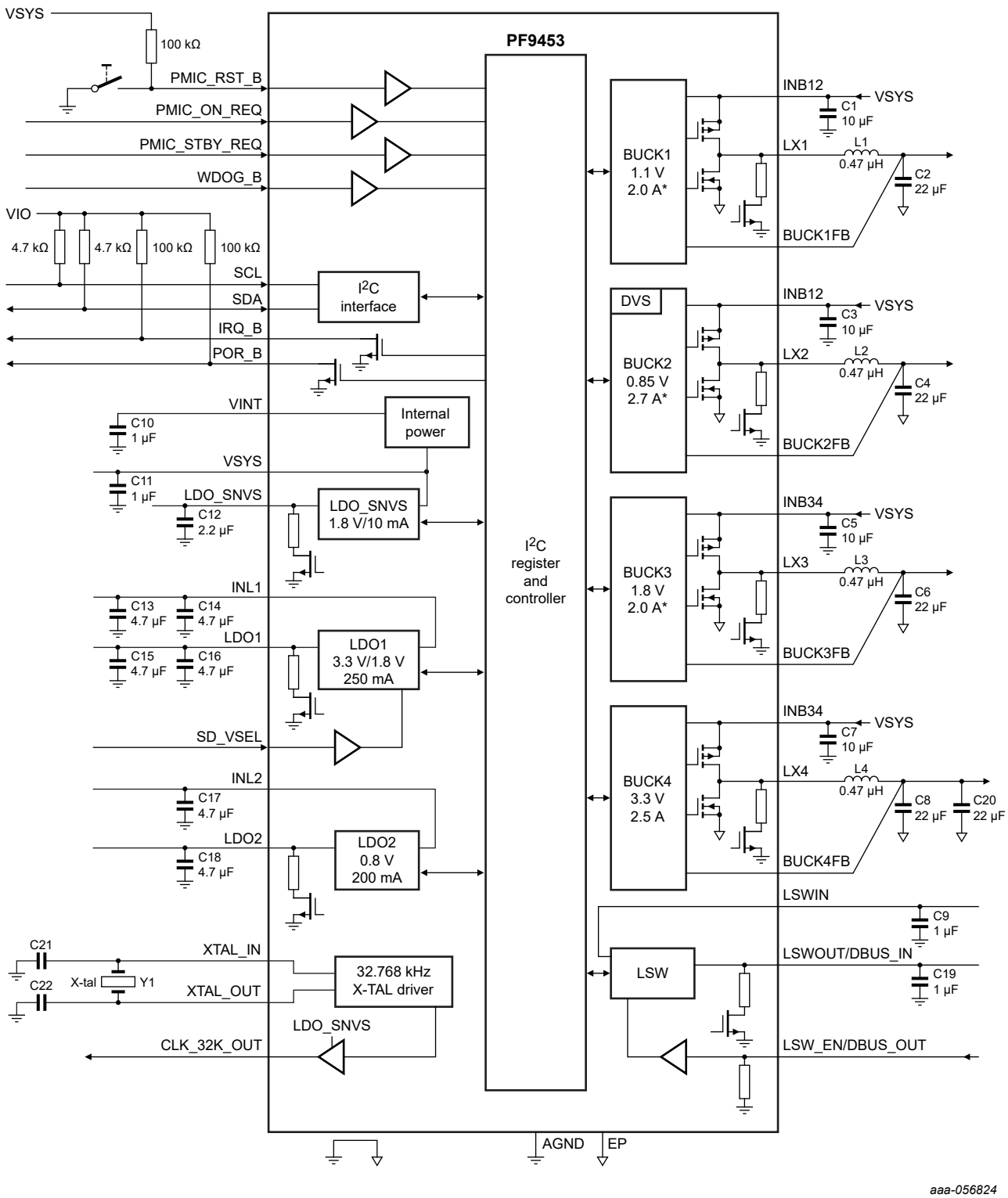
4 Ordering information

Table 1. Ordering information

Part number	Topside marking	Ambient temperature	Package			OTP configuration	Processor
			Name	Description	Version		
MPF9453AVMA1HN	-	-40 °C to +105 °C (for use in industrial applications)	HVQFN40	40-pin QFN, 5.0 mm x 5.0 mm with exposed pad, 0.4 mm pitch	SOT2231-1	A1[1]	i.MX 9131, 9111
MPF9453AVMA2HN	-					A2[2]	i.MX 93
MPF9453AVMB1HN	-					B1[3]	i.MX9121, 9101
MPF9453ACMA1HN	-	-40 °C to +85 °C (for use in consumer applications)				A1[1]	i.MX 9131, 9111
MPF9453ACMA2HN	-					A2[2]	i.MX 93
MPF9453ACMB1HN	-					B1[3]	i.MX9121, 9101
PPF9453ACMA1UK	-	-40 °C to +85 °C (for use in consumer applications)	WLCSP36	Wafer-level chip scale package; 36 bumps; 2.46 mm x 2.46 mm x 0.525 mm body (backside coating included), 0.4 mm pitch	SOT1780-14	A1[1]	i.MX 91
PPF9453ACMB1UK	-					B1[3]	i.MX 9121, 9101
Note: *P = Pre-release part number; M = Production part number*							

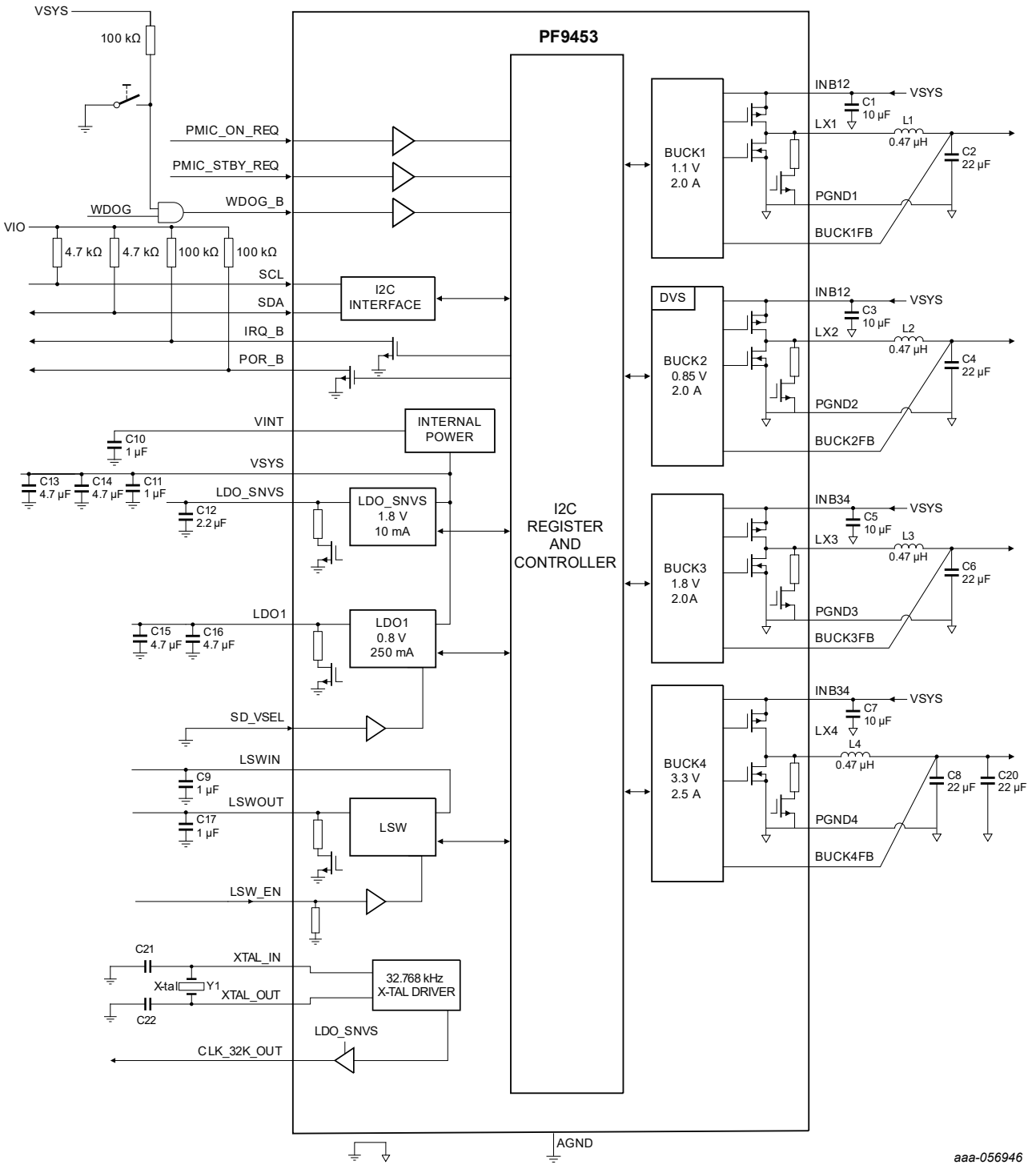
[1] For A1 OTP configuration, BUCK1 and BUCK3 are 1000 mA, BUCK2 is 1500 mA, BUCK4 is 2500 mA
[2] For A2 OTP configuration, BUCK1, BUCK3 are 2000 mA, BUCK2 is 2700 mA and BUCK4 is 2500 mA
[3] For B1 OTP configuration, BUCK1, BUCK2, BUCK3 are 1000 mA and BUCK4 is 1500 mA

5 Block diagram



For A1 and B1 OTP configuration, current output is different. See Table 1

Figure 1. PF9453 block diagram - HVQFN40 package



For A1 and B1 OTP configuration, current output is different. See Table 1

Figure 2. PF9453 block diagram - WLCSP36 package

6 Pinning information

6.1 Pinning

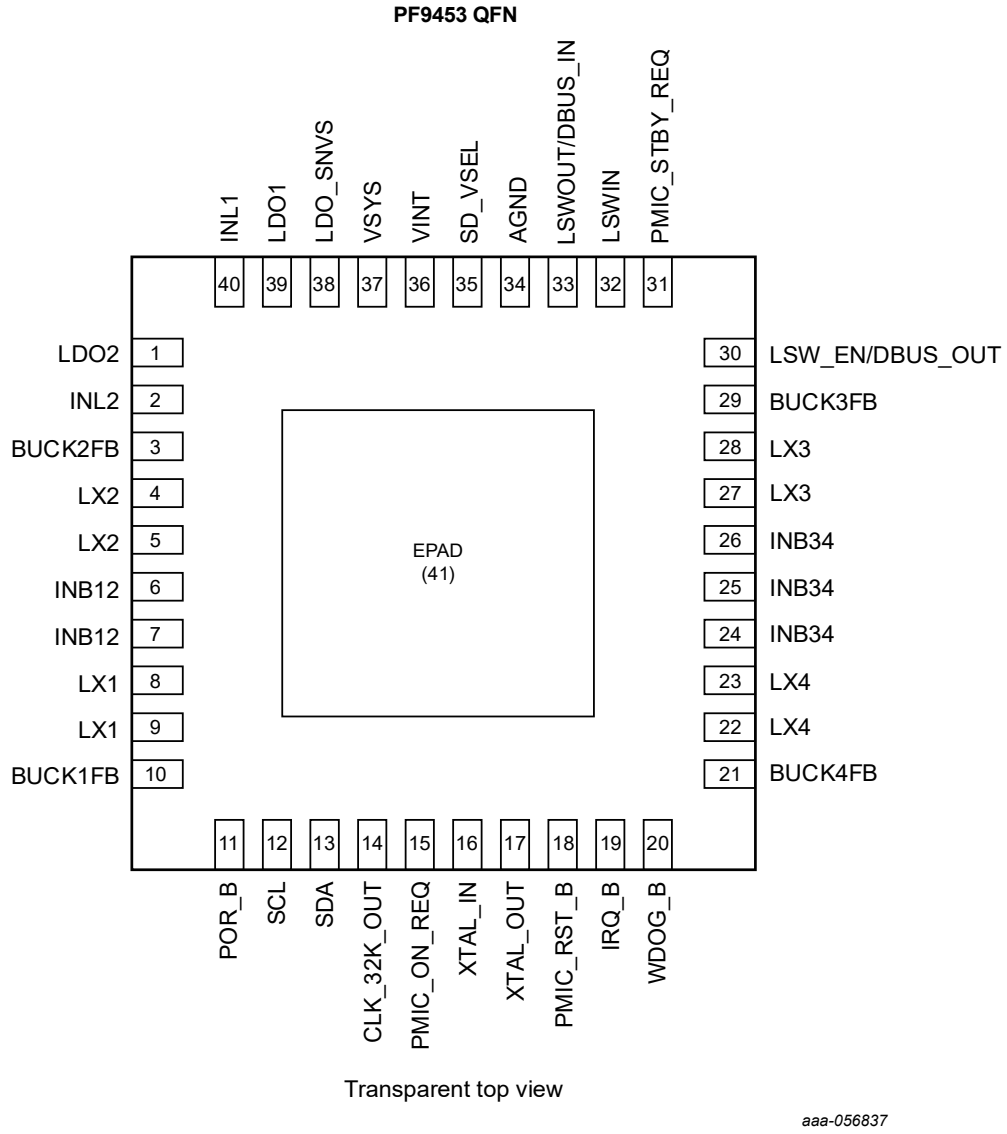


Figure 3. PF9453 pin map – HVQFN transparent top view

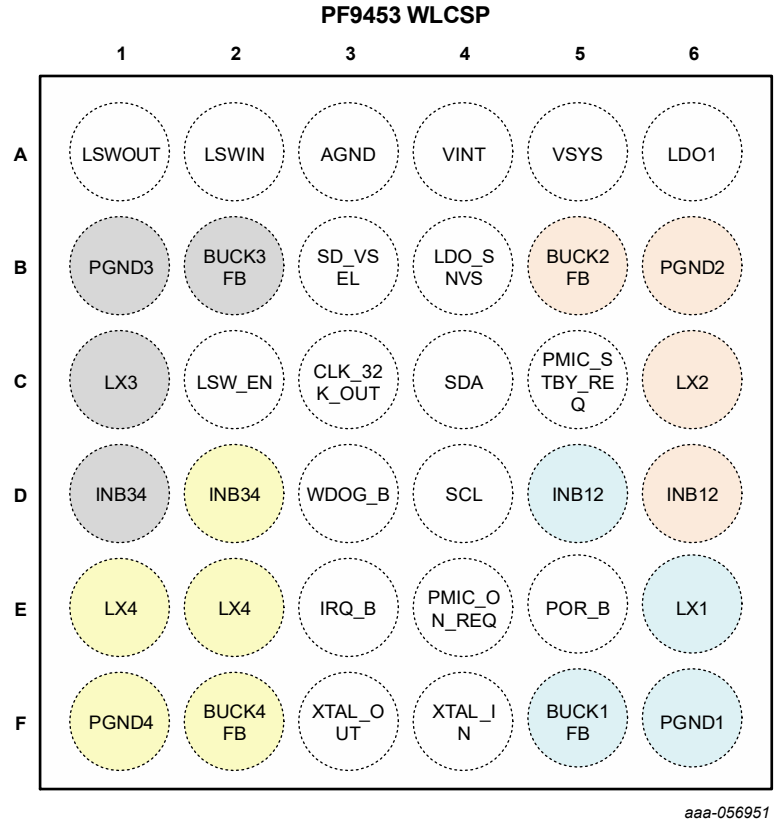


Figure 4. PF9453 pin map – WLCSP36 top view

6.2 Pin description

Table 2. Pin description – PF9453 QFN

Symbol	Pin	Type	Description
LDO2	1	P	LDO2 output, bypass with a 4.7 µF to GND
INL2	2	P	LDO2 input pin, bypass with a 4.7 µF to GND
BUCK2FB	3	AI	Buck 2 feedback pin
LX2	4, 5	P	Buck 2 switching node
INB12	6, 7	P	Buck 1 and Buck 2 input pins, bypass with 2 µF x 10 µF
LX1	8, 9	P	Buck 1 switching node
BUCK1FB	10	AI	Buck 1 feedback pin
POR_B	11	DO	Power-on reset (POR) output pin. Open-drain output requiring external pullup resistor
SCL	12	DI	I^2C serial clock pin
SDA	13	DIO	I^2C serial data pin
CLK_32K_OUT	14	DO	32.768 kHz clock CMOS output with LDO_SNVS power rail
PMIC_ON_REQ	15	DI	PMIC input from an application processor. When it is asserted high, the device starts power on sequence
XTAL_IN	16	AI	32.768 kHz crystal oscillator input, tie to GND if X-tal is not used

Table 2. Pin description – PF9453 QFN*...continued*

Symbol	Pin	Type	Description
XTAL_OUT	17	AO	32.768 kHz crystal oscillator output, leave floating if X-tal is not used
PMIC_RST_B	18	DI	PMIC reset input pin. Once it is asserted low, PMIC performs a Cold Reset
IRQ_B	19	DO	PMIC interrupt pin, open-drain output requiring external pullup resistor.
WDOG_B	20	DI	Watchdog reset input from application processor
BUCK4FB	21	AI	Buck 4 feedback pin
LX4	22, 23	P	Buck 4 switching node
INB34	24, 25, 26	P	Buck 3 and Buck 4 input pins, bypass with 2 µF x 10 µF
LX3	27, 28	P	Buck 3 switching node
BUCK3FB	29	AI	Buck 3 feedback pin
LSW_EN/DBUS_OUT	30	DI/DO	Load switch enable input pin. It has an internal 1.5 MΩ pulldown resistor or an output pin for the DBUS debounce filter function
PMIC_STBY_REQ	31	DI	Standby mode input from application processor. When it is asserted high, the device enters standby mode
LSWIN	32	P	Load switch input pin. Bypass with a 1 µF to GND
LSWOUT/DBUS_IN	33	P/DI	Load switch output pin, bypass with a 1 µF to GND. Or input pin for DBUS debounces filter function.
AGND	34	GND	Analog GND pin. It should be connected to the GND plane through via. Do not short to EPAD directly on the top layer.
SD_VSEL	35	DI	LDO1 voltage selection input pin. LDO1 output is 3.3 V when it is driven low and 1.8 V when driven high.
VINT	36	P	Internal power supply output, bypass with a 1 µF to GND
VSYS	37	P	Internal power input. Bypass with a 1 µF to GND
LDO_SNVS	38	P	LDO_SNVS output pin, bypass with a 2.2 µF to GND
LDO1	39	P	LDO1 output. Bypass with 2 µF x 4.7 µF to GND
INL1	40	P	LDO1 input pin, bypass with 2 µF x 4.7 µF to GND
EPAD	41	GND	Exposed pad, connect to GND.

Table 3. Pin description - PF9453 WLCSP

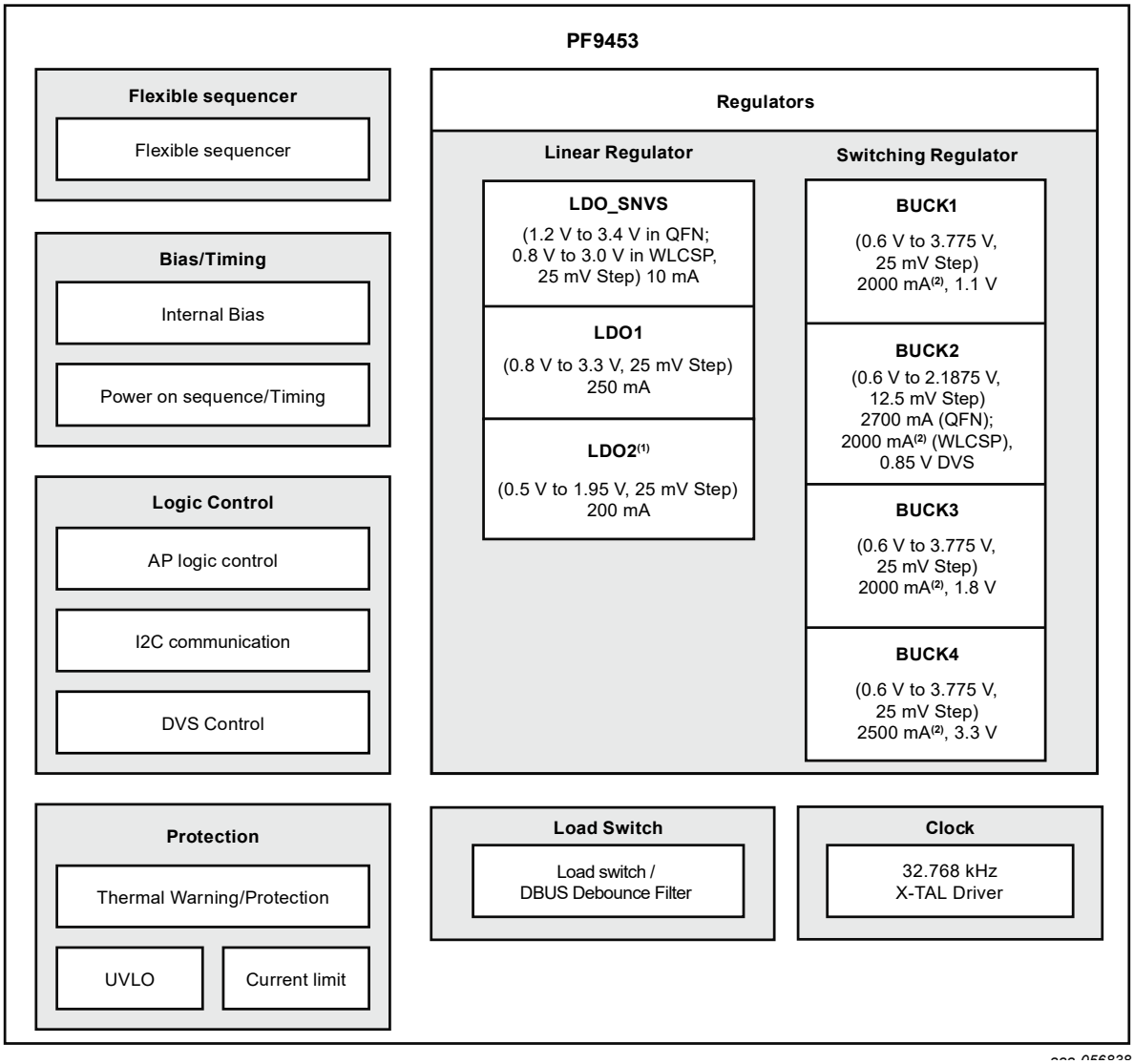
Symbol	Pin	Type	Description
LDO1	A6	P	LDO1 output. Bypass with 2 µF x 4.7 µF to GND.
LDO_SNVS	B4	P	LDO_SNVS output pin, bypass with a 2.2 µF to GND
POR_B	E5	DO	POR output pin. Open drain output requiring external pullup resistor
IRQ_B	E3	DO	PMIC interrupt pin, open drain output requiring external pullup resistor
VSYS	A5	P	Internal power input. Bypass with a 1 µF to GND
XTAL_IN	F4	AI	32.768 kHz crystal oscillator input, tie to GND if XTAL is not used
XTAL_OUT	F3	AO	32.768 kHz crystal oscillator output, leave float if XTAL is not used
CLK_32K_OUT	C3	DO	32.768 kHz clock CMOS output with LDO_SNVS power rail.
BUCK4FB	F2	AI	Buck 4 feedback pin

Table 3. Pin description - PF9453 WLCSP*...continued*

Symbol	Pin	Type	Description
PGND4	F1	GND	Buck 4 power GND
LX4	E1, E2	P	Buck 4 switching node
INB34	D1, D2	P	Buck 3 and buck 4 input pins, bypass with 2 µF x 10 µF
LX3	C1	P	Buck 3 switching node
BUCK3FB	B2	AI	Buck 3 feedback pin
PGND3	B1	GND	Buck 3 power GND
LSWIN	A2	P	Load switch input pin. Bypass with a 1 µF to GND
LSWOUT	A1	P	Load switch output pin. Bypass with a 1 µF to GND.
SCL	D4	DI	I^2C serial clock pin
SDA	C4	DIO	I^2C serial data pin
BUCK2FB	B5	AI	Buck 2 feedback pin
LX2	C6	P	Buck 2 switching node
PGND2	B6	GND	Buck 2 power GND
INB12	D5, D6	P	Buck 1 and Buck 2 input pins, bypass with 2 µF x 10 µF
LX1	E6	P	Buck 1 switching node
BUCK1FB	F5	AI	Buck 1 feedback pin
PGND1	F6	GND	Buck 1 power GND
WDOG_B	D3	DI	Watchdog reset input from application processor.
PMIC_STBY_REQ	C5	DI	Standby mode input from application processor. When it is asserted high, the device enters standby mode.
PMIC_ON_REQ	E4	DI	PMIC on input from application processor. When it is asserted high, the device starts power on sequence.
VINT	A4	P	Internal power supply output, bypass with a 1 µF to GND.
SD_VSEL	B3	DI	LDO1 voltage selection input pin. LDO1 outputs a voltage set by L1_OUT_L[6:0] when it is driven low and L1_OUT_H[6:0] when driven high.
LSW_EN	C2	DI	Load switch enable input pin. It has an internal 1.5 mohm (Ω) pulldown resistor .
AGND	A3	GND	Analog GND pin. It should be connected to the GND plane through via.

7 Functional description

7.1 Functional diagram



(1) QFN only

(2) For A1 and B1 OTP configuration, output current is different; see Table 1

Figure 5. PF9453 functional block diagram

7.2 PF9453 OTP version

The PF9453 can be configured to each regulator default voltage and startup sequence from the internal OTP configuration. Table 4 shows the power-up sequence.

Table 4. Power up sequence

Regulator	MPF9453AxMA1HN, MPF9453AxMA2HN, MPF9453AxMB1HN	PPF9453ACMA1UK, PPF9453ACMB1UK
LDO_SNVS	1.8 V, always on	1.8 V, always on
BUCK1	T4, 1.1 V	T4, 1.1 V
BUCK2	T1, 0.85 V	T1, 0.85 V
BUCK3	T3, 1.8 V	T3, 1.8 V
BUCK4	T5, 3.3 V	T5, 3.3 V
LDO1	T6, 3.3 V / 1.8 V	T2, 0.8 V
LDO2*	T2, 0.8 V	NA
Load Switch	T5	T5

Details of the OTP programming for each device can be found in PF9453 QFN OTP versionSection 9.

7.3 Power states

PF9453 has six power states: OFF, SNVS, RUN, PWRDN, PWRUP, and FAULT_SD. Figure 6 shows the state transition diagram with the conditions to enter and exit each state.

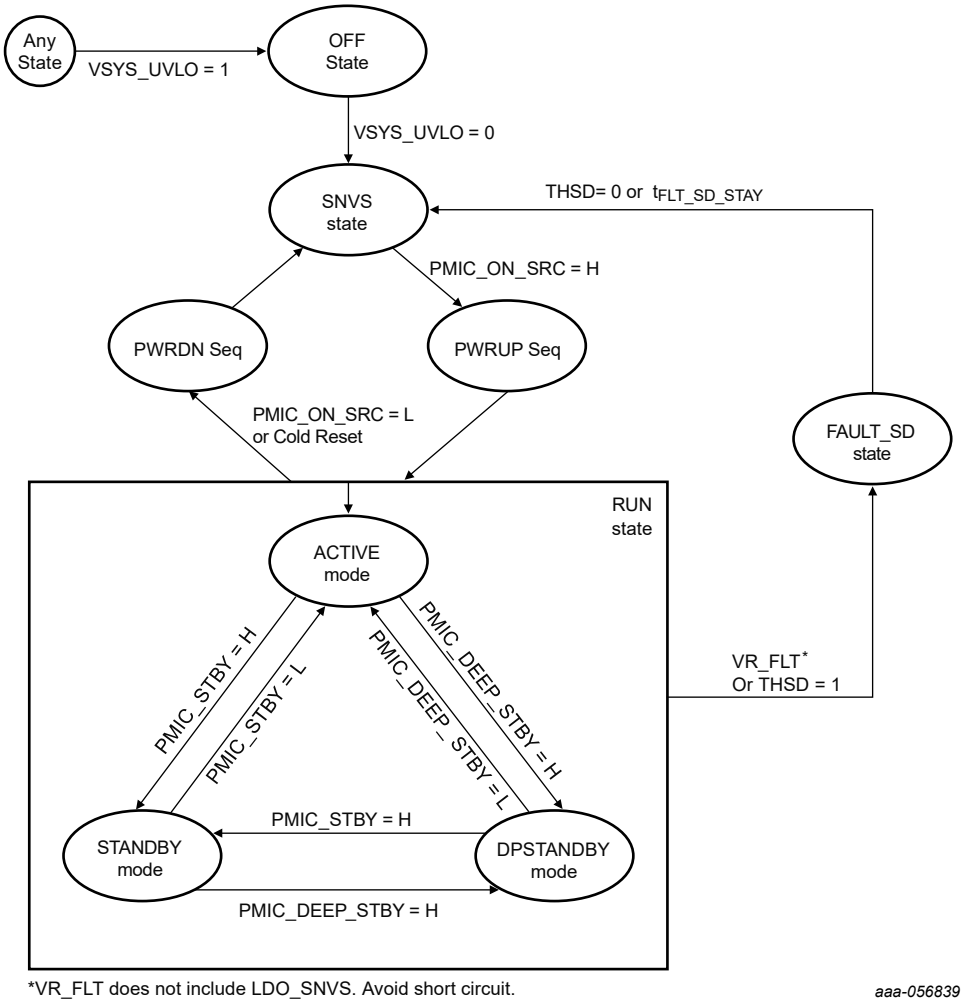


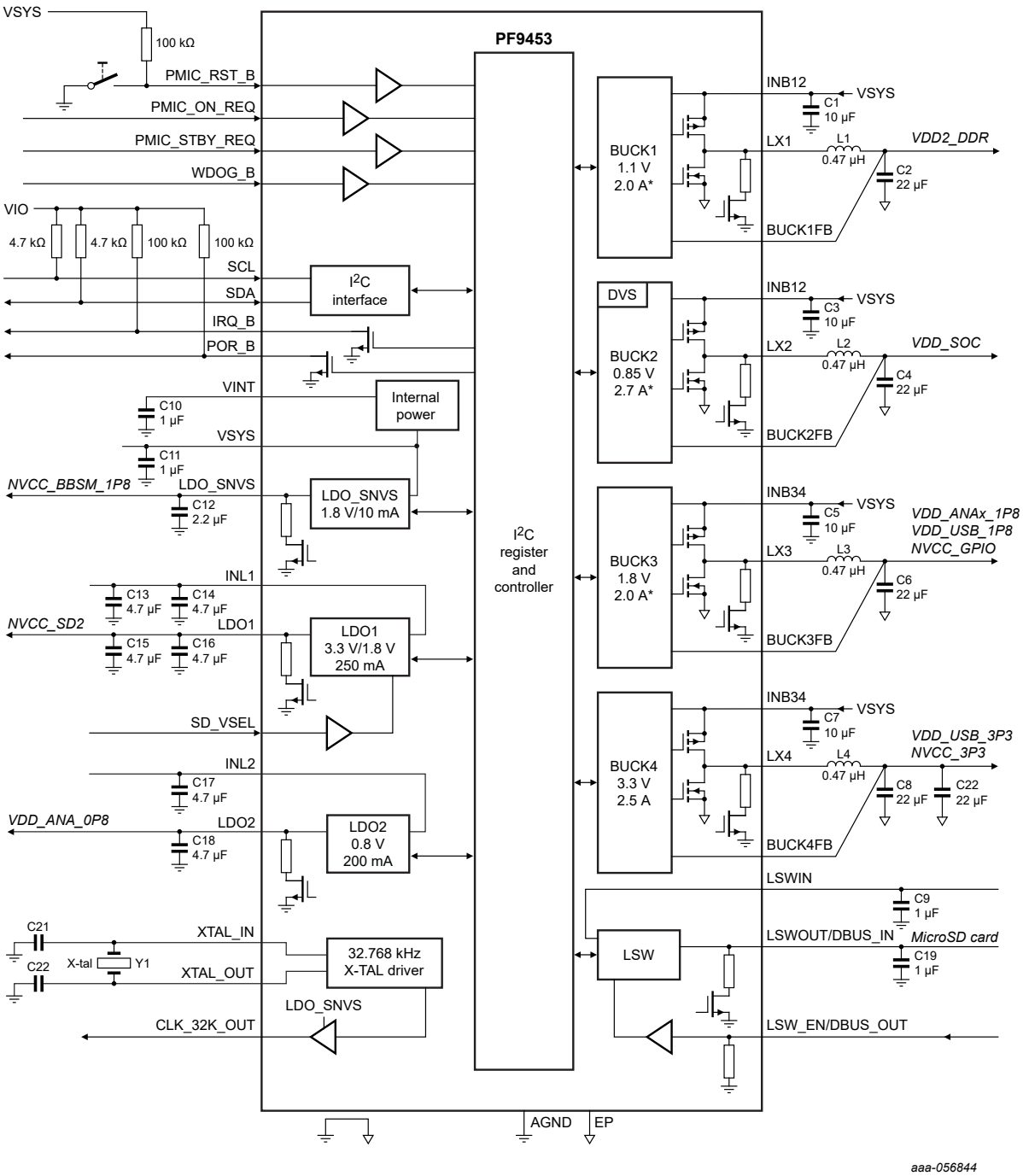
Figure 6. Power states diagram

8 Application design-in information

8.1 Reference schematic

8.1.1 PF9453 reference schematic

PF9453 (HVQFN40 and WLCSP36 package) reference schematics with i.MX 91 processor are illustrated in Figure 7 and Figure 8.



For A1 and B1 OTP configuration, output current is different; see Table 1

Figure 7. PF9453 QFN application schematic

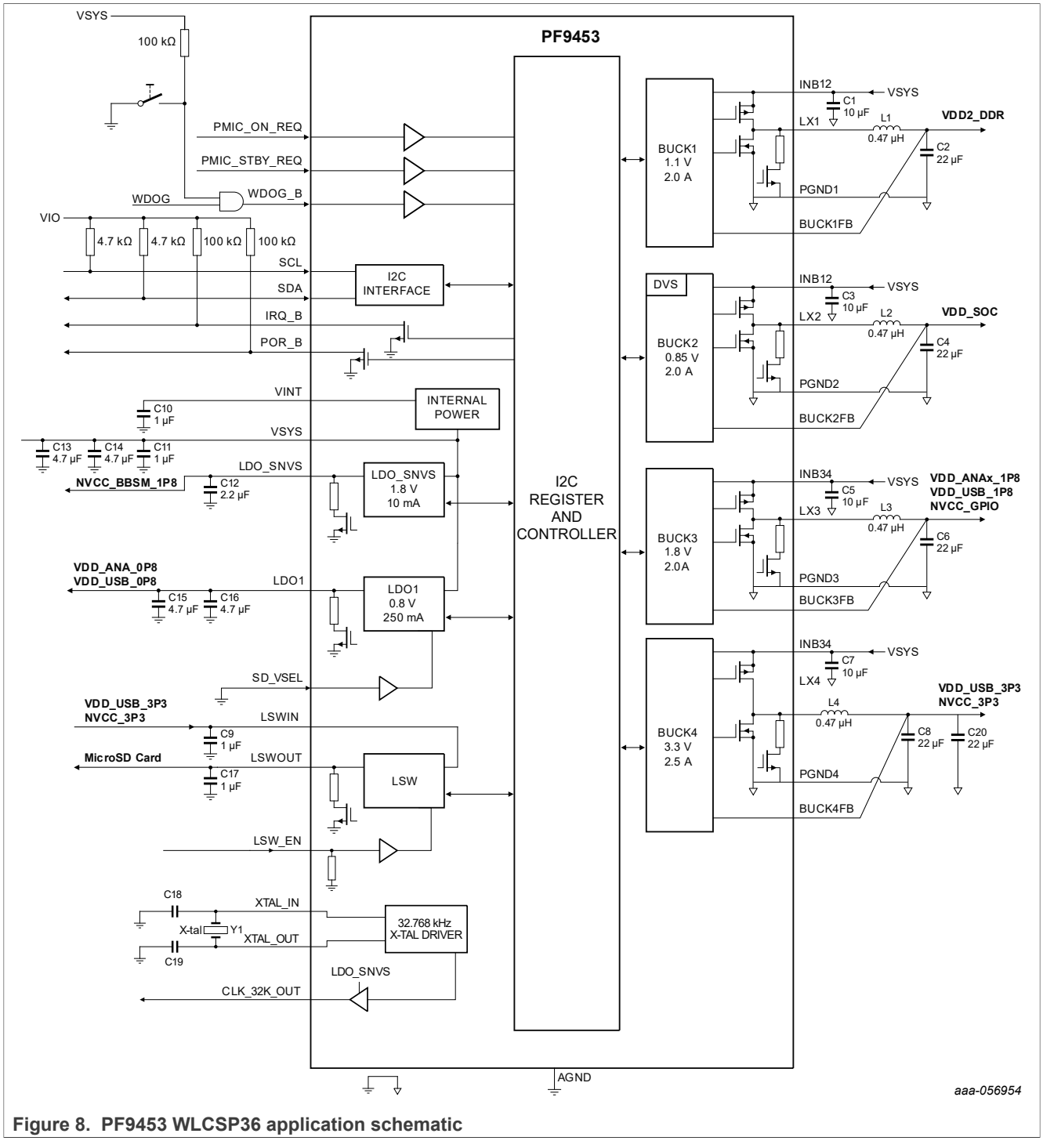


Figure 8. PF9453 WLCSP36 application schematic

8.2 Layout guide

For layout guidance, refer to Figure 9 and Figure 10.

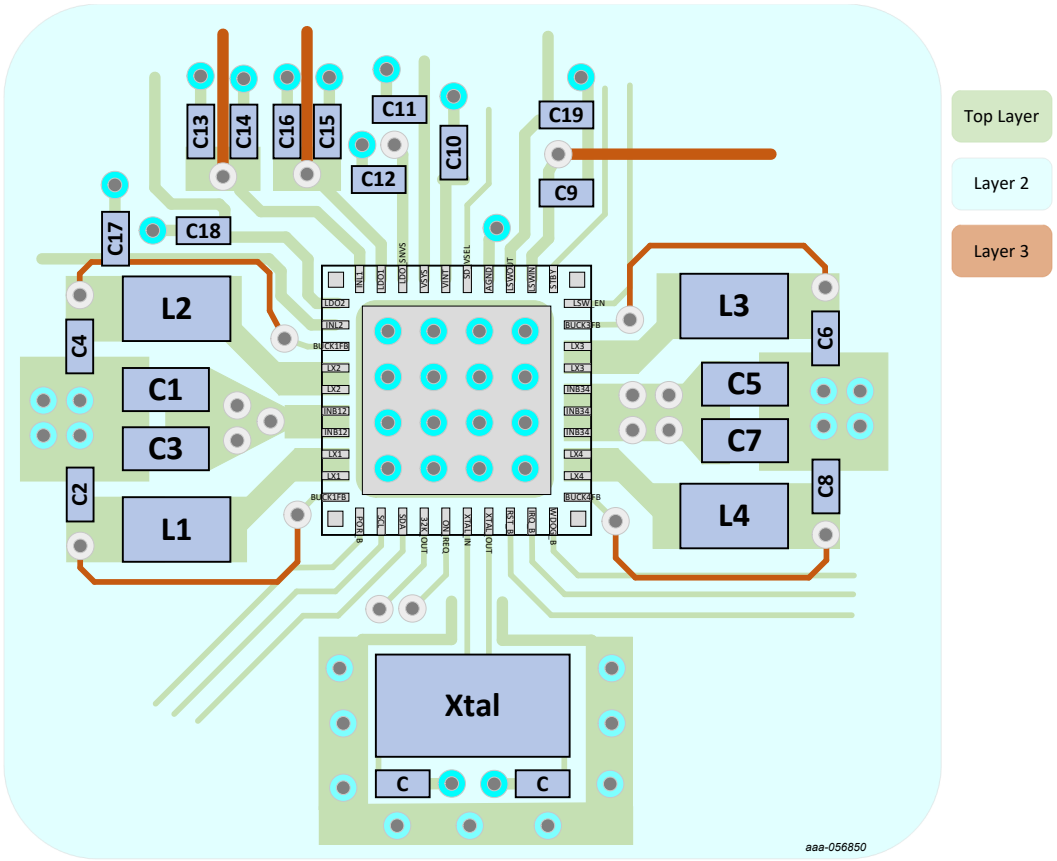


Figure 9. PF9453 HVQFN40 layout

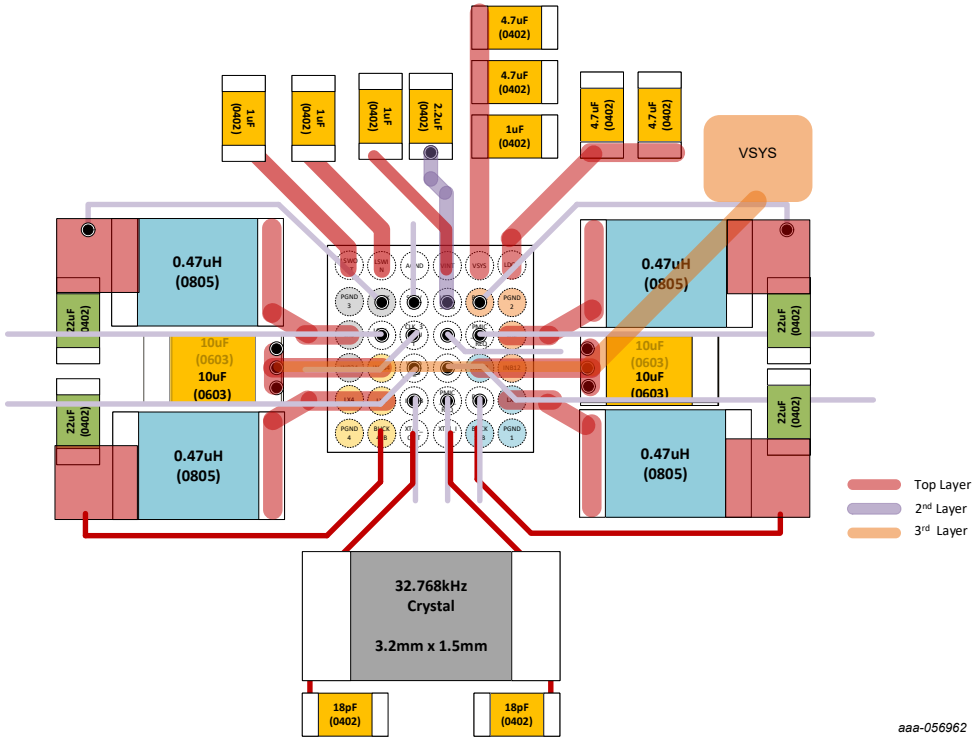


Figure 10. PF9453 WLCSP36 layout

9 PF9453 QFN/WLCSP OTP configuration differences

Table 5 shows the OTP registers that can be configured in the QFN and WLCSP packages. As an additional note the OTPs A1, A2, B1 of each package have the same configuration, but the current capabilities of each regulator are different, for more details refer to Table 1.

Table 5. OTP configuration

Functional block	Register	Feature	MPF9453AVMXXHN (QFN)	PPF9453ACMXXUK (WLCSP)
BUCK1	0x10 (BUCK1CTRL)	Buck1 enable mode	ON at RUN state (default)	ON at RUN state (default)
	0x10 (BUCK1CTRL)	Forced PWM mode	Automatic PFM and PWM mode transition (default)	Automatic PFM and PWM mode transition (default)
	0x10 (BUCK1CTRL)	Buck1 active discharge	Enable active discharge resistor when regulator is OFF(default)	Enable active discharge resistor when regulator is OFF(default)
	0x11 (BUCK1OUT)	BUCK1 output voltage	1.1 V	1.1 V
	0x3D (BUCK_POK_F_CFG)	BUCK1 POK falling threshold	75% of output voltage (default)	75% of output voltage (default)[1]
	* (Internal)	BUCK1 sequence	T4 (default)	T4 (default)
BUCK2	0x14 (BUCK2CTRL)	Buck2 enable mode	ON at RUN state (default)	ON at RUN state (default)

Table 5. OTP configuration*...continued*

Functional block	Register	Feature	MPF9453AVMXXHN (QFN)	PPF9453ACMXXUK (WLCSP)
	0x14 (BUCK2CTRL)	Forced PWM mode	Automatic PFM and PWM mode transition (default)	Automatic PFM and PWM mode transition (default)
	0x14 (BUCK2CTRL)	Buck2 active discharge	Enable active discharge resistor when regulator is OFF(default)	Enable active discharge resistor when regulator is OFF(default)
	0x14 (BUCK2CTRL)	BUCK2 DVS speed	25 mV/2 µs (default)	25 mV/2 µs (default)
	0x15 (BUCK2OUT)	BUCK2 output voltage	0.85 V	0.85 V
	0x1F (BUCK2OUT_MAX_LIMIT)	BUCK2 output voltage maximum limit	0.9 (0.95 for PPF9453AVMA2HN)	0.9 V
	0x20 (BUCK2OUT_MIN_LIMIT)	BUCK2 output voltage minimum limit	0.6125 V	0.6125 V
	0x3D (BUCK_POK_F_CFG)	BUCK2 POK falling threshold	75% of output voltage (default)	75% of output voltage (default)[1]
	* (Internal)	BUCK2 sequence	T1 (default)	T1 (default)
BUCK3	0x21 (BUCK3CTRL)	BUCK3 enable mode	ON at RUN state (default)	ON at RUN state (default)
	0x21 (BUCK3CTRL)	Forced PWM mode	Automatic PFM and PWM mode transition (default)	Automatic PFM and PWM mode transition (default)
	0x21 (BUCK3CTRL)	BUCK3 active discharge	Enable active discharge resistor when regulator is OFF(default)	Enable active discharge resistor when regulator is OFF(default)
	0x22 (BUCK3OUT)	BUCK3 output voltage	1.8	1.8
	0x3D (BUCK_POK_F_CFG)	BUCK3 POK falling threshold	75 % of output voltage (default)	75 % of output voltage (default)[1]
	* (Internal)	BUCK3 sequence	T3 (default)	T3 (default)
BUCK4	0x2E (BUCK4CTRL)	BUCK4 enable mode	ON at RUN State (default)	ON at RUN state (default)
	0x2E (BUCK4CTRL)	Forced PWM mode	Automatic PFM and PWM mode transition (default)	Automatic PFM and PWM mode transition (default)
	0x2E (BUCK4CTRL)	Buck4 active discharge	Enable active discharge resistor when regulator is OFF(default)	Enable active discharge resistor when regulator is OFF(default)
	0x2F (BUCK4OUT)	BUCK4 output voltage	3.3 V	3.3 V
	0x3D (BUCK_POK_F_CFG)	BUCK4 POK falling threshold	75 % of output voltage (default)	75 % of output voltage (default)[1]
	* (Internal)	BUCK4 Sequence	T5 (default)	T5 (default)

Table 5. OTP configuration*...continued*

Functional block	Register	Feature	MPF9453AVMXXHN (QFN)	PPF9453ACMXXUK (WLCSP)
LDO1	0x36 (LDO1_OUT_L)	LDO1 output voltage when SD_VSEL pin = Low	3.3 V	0.8 V
	0x37 (LDO1_CFG)	LDO1 enable mode	ON at RUN state (default)	ON at RUN state (default)
	0x37 (LDO1_CFG)	LDO1 active discharge control during OFF	Enable active discharge resistor when regulator is OFF(default)	Enable active discharge resistor when regulator is OFF(default)
	0x37 (LDO1_CFG)	LDO1 active discharge control during ON	Enable active discharge resistor for 2ms during LDO1 transition only from 3.3V to 1.8V by toggling SD_VSEL pin (default)	Enable active discharge resistor for 2ms during LDO1 transition only from 3.3V to 1.8V by toggling SD_VSEL pin (default)
	0x38 (LDO1_OUT_H)	LDO1 output voltage when SD_VSEL pin = High	1.8 V	0.8 V
	* (Internal)	LDO1 sequence	T6 (default)	T2 (Default)
LDO_SNVS	0x39 (LDOSNVS_ CFG1)	LDO_SNVS output voltage	1.8 V	1.8 V
	0x39 (LDOSNVS_ CFG1)	SNVS LDO active discharge enable	Enable active discharge resistor when regulator is OFF (default)	Enable active discharge resistor when regulator is OFF (default)
LDO2	0x3B (LDO2_CFG)	LDO2 enable mode	ON at RUN State (default)	NA
	0x3B (LDO2_CFG)	Total output capacitor selection	Auto cout detection (default)	NA
	0x3B (LDO2_CFG)	Output trace resistance compensation	15 Ω (default)	NA
	0x3B (LDO2_CFG)	LDO2 active discharge enable	Enable active discharge resistor when regulator is OFF (default)	NA
	0x3C (LDO2_OUT)	LDO2 output voltage	0.8 V	NA
	0x3C (LDO2_OUT)	INL2 voltage selection, effective only when L2_INL2_MDET = 1b	(VSYS – VINL2) > 0.7V (default)	NA
	0x3C (LDO2_OUT)	Manual detection for INL2 supply	Auto detection (default)	NA
	* (Internal)	LDO2 sequence	T2 (default)	NA
Load Switch	0x40 (LSW_CTRL1)	Load SW enable mode	Enabled by LSW_EN pin (default)	Enabled by LSW_EN pin (default)

Table 5. OTP configuration*...continued*

Functional block	Register	Feature	MPF9453AVMXXHN (QFN)	PPF9453ACMXXUK (WLCSP)
	0x40 (LSW_CTRL1)	Load SW active discharge	Enabled when load SW1 is off (default)	Enabled when Load SW1 is off (default)
	0x40 (LSW_CTRL1)	Program a short glitch timer (debounce time) on LSWIN pin	5 ms (default)	5ms (default)
	0x40 (LSW_CTRL1)	Load switch and DBUS debounce filter configuration	Load switch (default)	Load switch (default)
	* (Internal)	LoadSwitch sequence	T5 (default)	T5 (default)
PWR_SEQ_CTRL	0x0A (PWR_SEQ_ CTRL)	Time step configuration during power down sequence	8 ms (default)	8 ms (default)
	0x0A (PWR_SEQ_ CTRL)	Time step configuration during power on sequence	2 ms (default)	2 ms (default)
	0x0A (PWR_SEQ_ CTRL)	Debounce time for PMIC_RST_B pin for falling edge.	20 ms (default)	NA
	0x0A (PWR_SEQ_ CTRL)	Configure PMIC_RST_ B pin as Power ON source	Mask (default)	NA
SYS_CFG2	0x0C (SYS_CFG2)	VSYS UVLO threshold, rising threshold	2.85 V (default)	2.85 V (default)
	0x0C (SYS_CFG2)	POK reference during power up	POK is reference to turn on next power group (default)	POK is reference to turn on next power group (default)
	0x0C (SYS_CFG2)	ONKEY timer configuration after PMIC_RST_B pin falls low	2 sec (default)	NA
RESET_CTRL	0x08 (RESET_CTRL)	Time to stay regulators off during Cold reset	250 ms (default)	250 ms (default)
	0x08 (RESET_CTRL)	When PMIC_RST_B is asserted to low, PMIC reset behavior	Cold reset, all voltage regulators are recycled (default)	NA
	0x08 (RESET_CTRL)	When WDOG_B is asserted to low, PMIC reset behavior	WDOG_B reset is disabled (default)	WDOG_B reset is disabled (default)

[1] For WLCSP package falling threshold is fixed and cannot be change by OTP.

10 Package outline

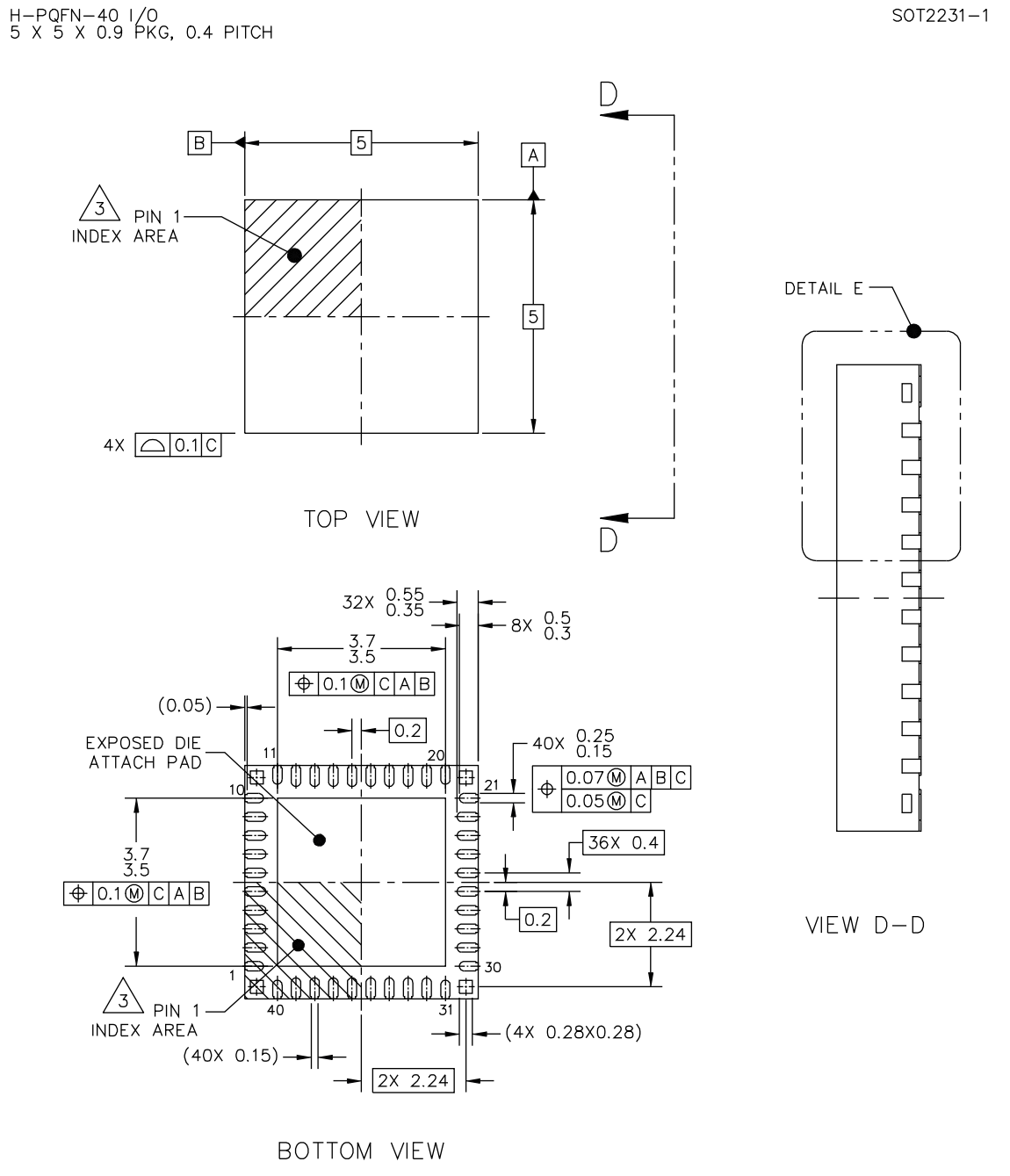
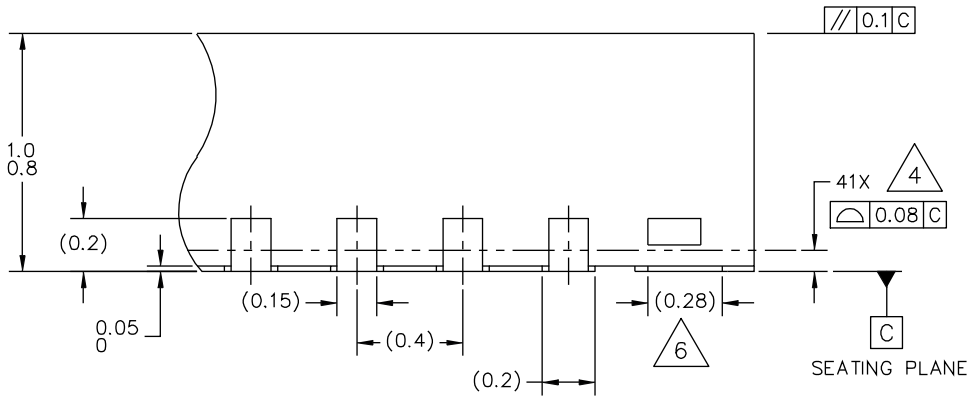


Figure 11. Package outline SOT2231-1 (HVQFN40)



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VIEW ROTATED 90° CW

DATE: 16 AUG 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02134D	REVISION: O	

Figure 12. Package outline SOT2231-1 (HVQFN40) detail E

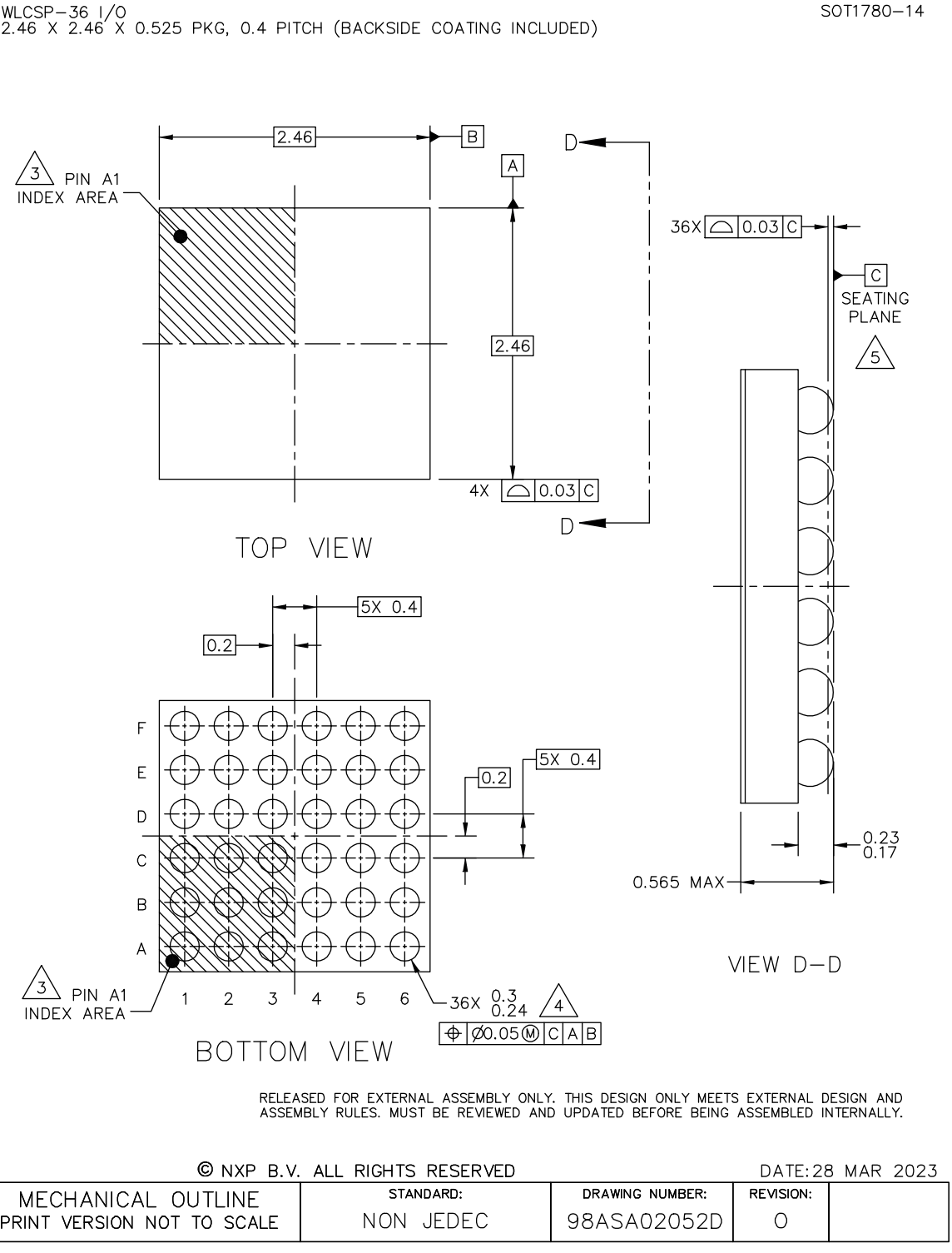


Figure 13. Package outline SOT1780-14 (WLCSP36)

11 Soldering

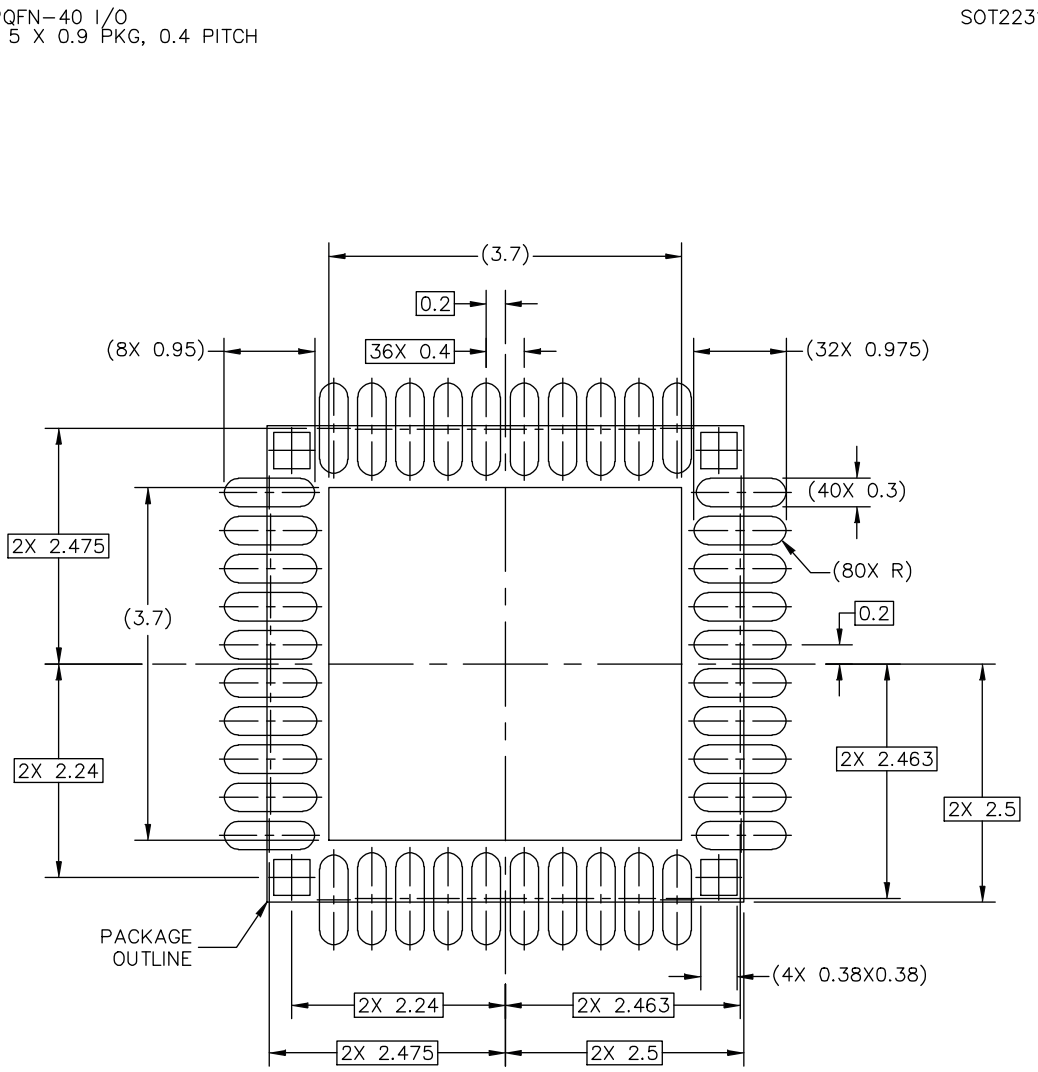
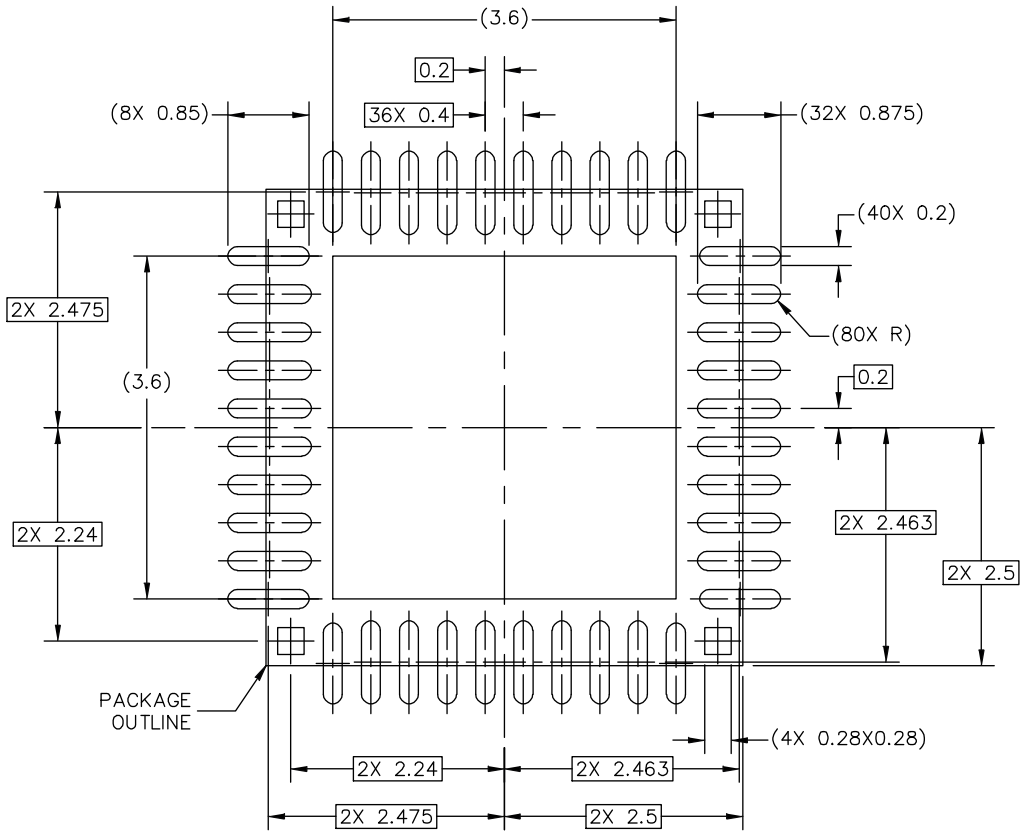


Figure 14. SOT2231-1 solder mask opening pattern



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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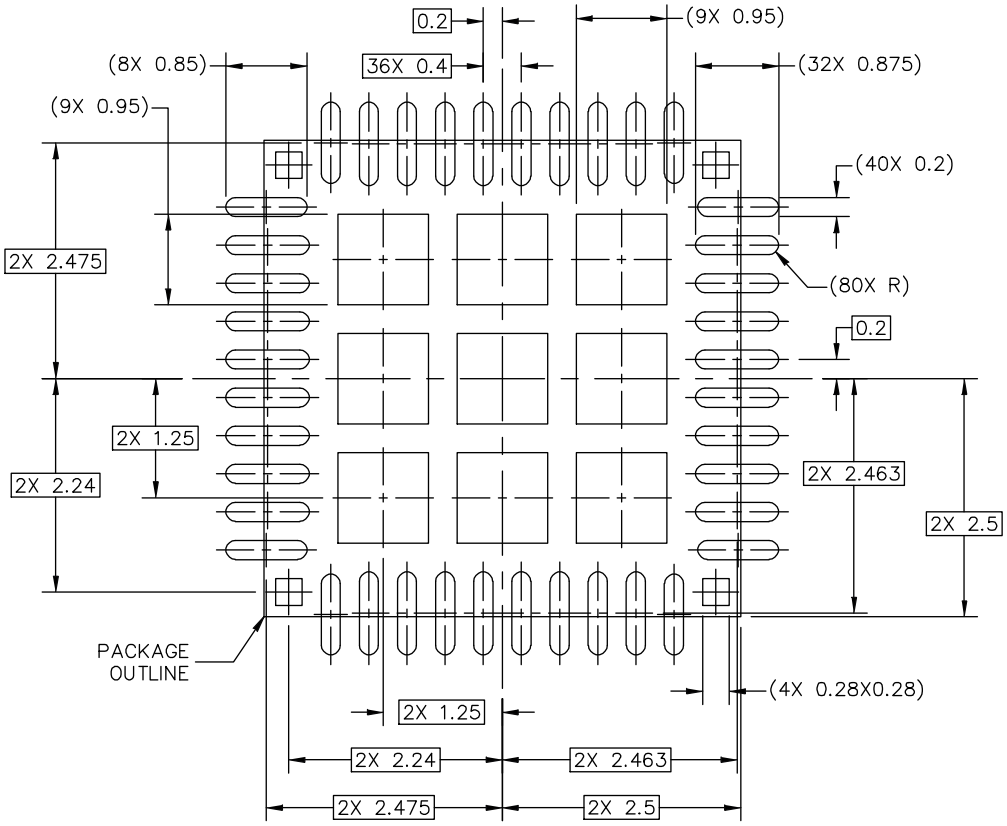
DATE: 16 AUG 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02134D	REVISION: O	

Figure 15. SOT2231-1 I/O pads and solderable area



RECOMMENDED STENCIL THICKNESS 0.1

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DATE: 16 AUG 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02134D	REVISION: O	

Figure 16. SOT2231-1 solder paste stencil

Figure 17. SOT2231-1 notes

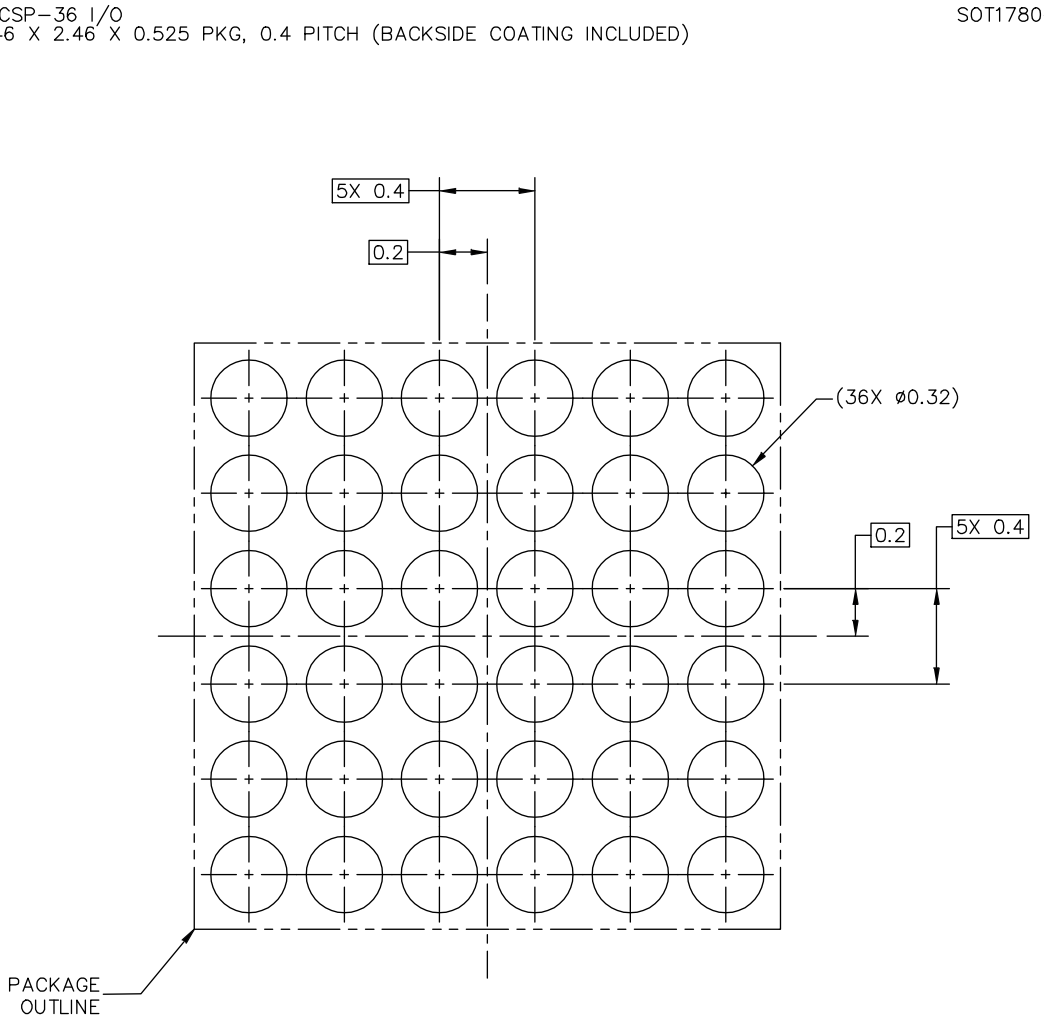
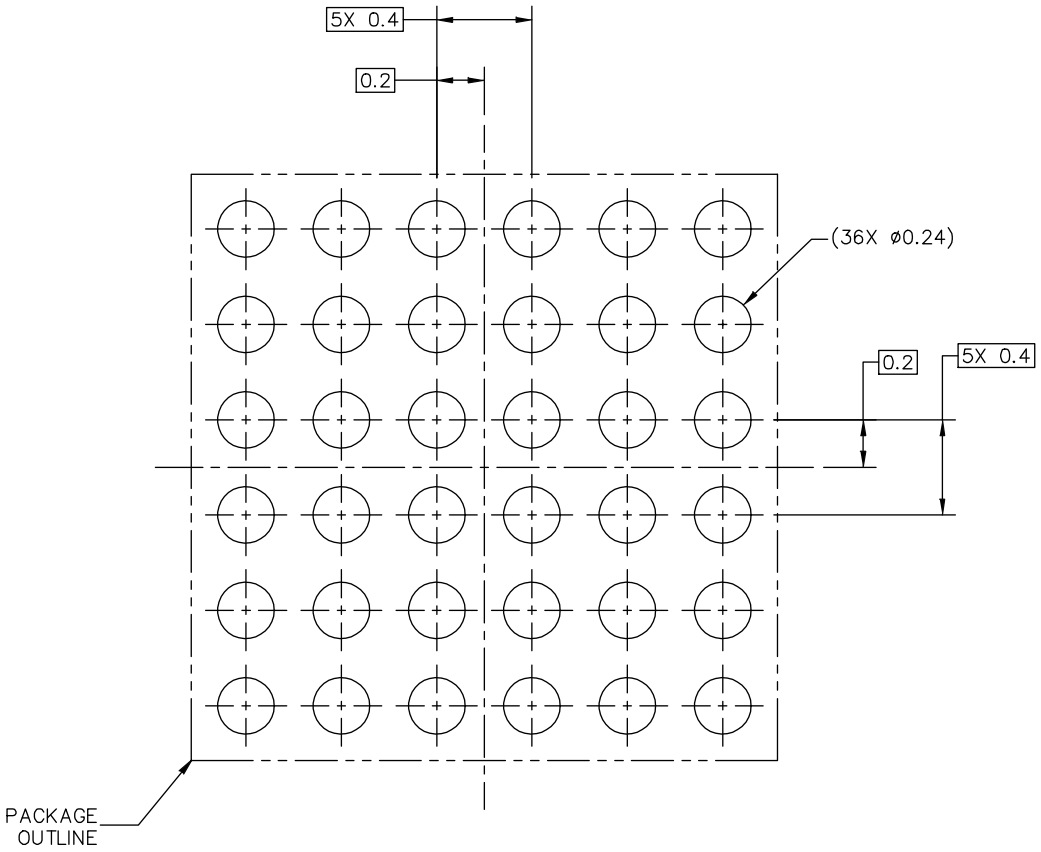


Figure 18. SOT1780-14 solder mask opening pattern

WLCSP–36 I/O
2.46 X 2.46 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1780–14



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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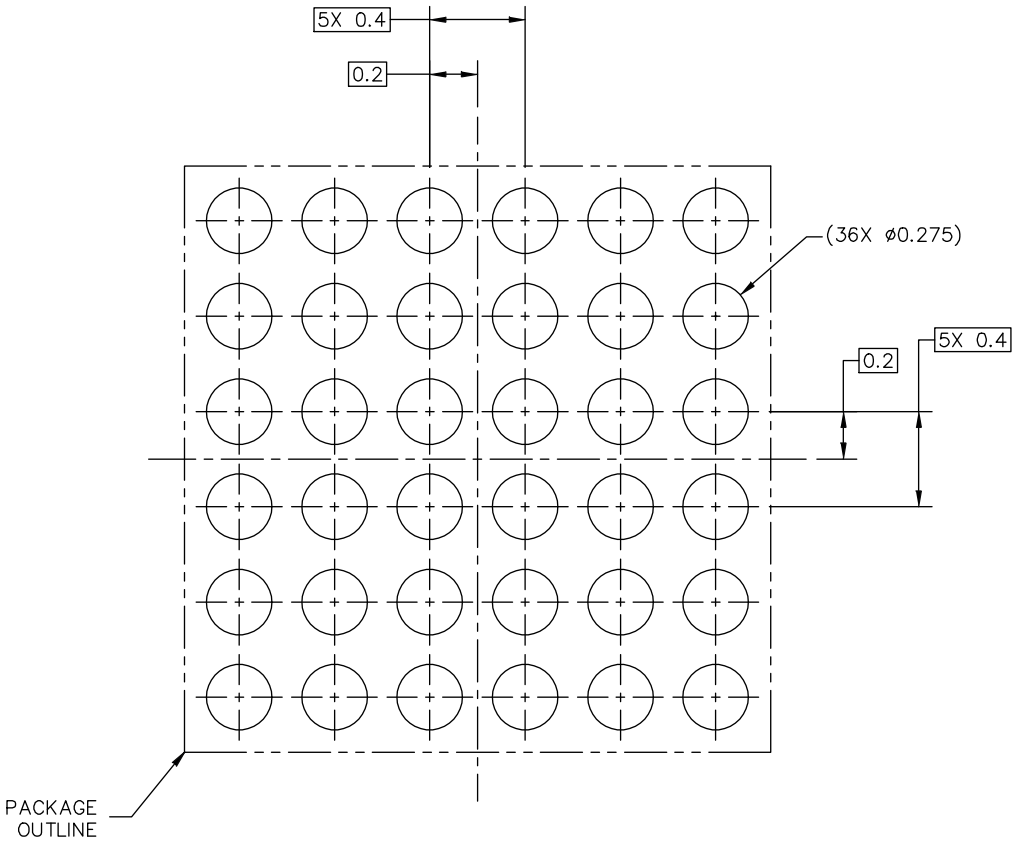
DATE: 28 MAR 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02052D	REVISION: O	

Figure 19. SOT1780-14 I/O pads and solderable area

WLCSP–36 I/O
2.46 X 2.46 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1780–14



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 28 MAR 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02052D	REVISION: O	

Figure 20. SOT1780-14 solder paste stencil

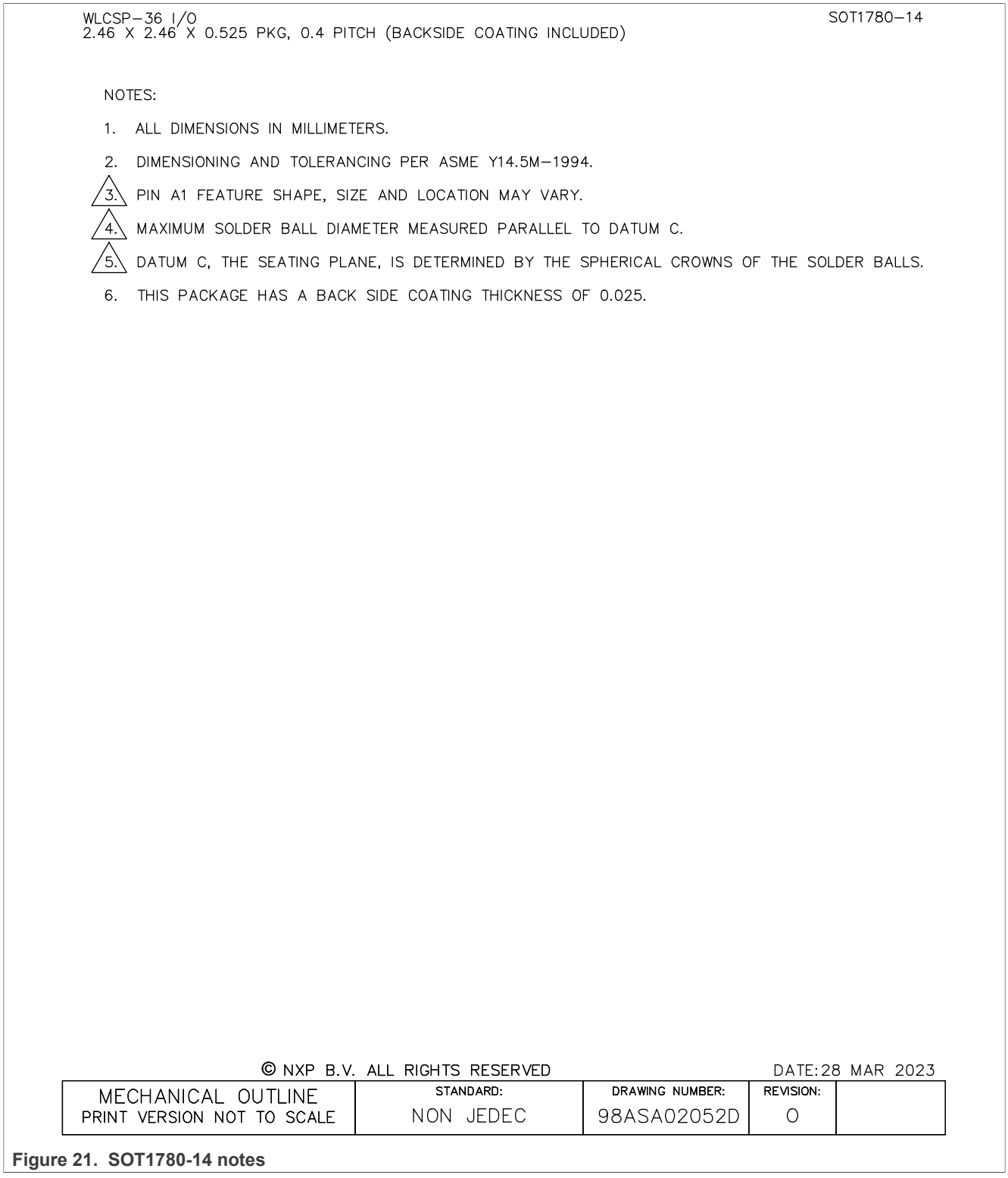


Figure 21. SOT1780-14 notes

12 Revision history

Table 6. Revision history

Document ID	Release date	Description
PF9453_SDS v.1.1	23 April 2025	• Final release. Updated Table 4 and Section 7.3
PF9453_SDS v.1.0	14 August 2024	• Initial version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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