NAFE93352

Software configurable universal high-speed AIO-AFE

Rev. 1.0 — 5 March 2025 Product data sheet

1 General description

The NAFE93352 is a software-configurable universal analog input and output (AIO) analog front-end (AFE) that meets high-precision measurement and control requirements of industrial-grade applications. The AIO-AFE integrates a precision 14/16/18-bit digital-to-analog converter (DAC), a 16/24-bit analog-to-digital converter (ADC), a low-drift voltage reference, low-offset drift buffers, high-voltage and high-precision amplifiers with 70 V input-protection circuit for EMC and miswiring scenarios. For open circuit and short-circuit detection, the output stage includes built-in diagnostic and protection circuitry. The input stage includes advanced diagnostic circuits enabling anomaly detection and facilitating predictive maintenance and functional safety.

The AIO-AFE is suitable for programmable logic controllers (PLC), I/O modules, data loggers, and high-precision data acquisition systems.

2 Features and benefits

- High-precision pin-to-pin and firmware compatible AIO-AFE family
- Multifunction and multiranges software configurable analog I/O
  - Voltage, current, resistance, temperature (RTD, thermocouple), load cell
- Integrated voltage references for end-to-end system calibration
- Both factory calibration and custom-user calibration options available
- Precise and fast response AIO-AFE architecture provides
  - 14-/16-/18-bit DAC and 16-/24-bit ADC
  - ADC 7.5 sps to 576 ksps data rate
  - DAC 0 to 200 ksps data rate
  - ±12.5 V, ±25 mA, 1 mΩ-1 MΩ I/O
  - ±0.01 % ADC accuracy at room
  - ±0.05 % ADC accuracy overtemperature (Voltage mode after room calibration)
  - INL 0.5 LSB max @ 16-bit; and 2 LSB max @ 18-bit
- Advanced diagnostic circuits for fault and anomaly detection and prediction
- Robust and flexible
  - ±36 V protected I/O (external transient voltage suppressor (TVS), required for ouptut)
  - ±7 V to ±28 V wide supply range, HVDD-HVSS = 14 V to 48 V
- -40 °C to 125 °C temperature range
- 6 mm x 6 mm small TQFN-40 package

2.1 IEC EMC ratings

IEC61004-2 ESD

IEC61004-4 Electrical Fast Transient/Burst test (EFT)

IEC61004-5 2 kV Surge Immunity Test

2.2 ESD stress rating and latch-up

Table 1. ESD stress rating and latch-up

Description	Max	Units
Human body model (HBM) on all pins	±7500	V
Charged device model (CDM) on all pins	±750	V
Latch-up at 150 ºC	±200	mA

Note: *These are stress ratings only. Functional operation of the product at conditions at or above its ratings is not implied.*

3 Applications

- Data acquisition system
- PLC, DCS I/O modules
- Industrial automation and process control

4 Ordering information

The NAFE93352 is a software-compatible family of products which can be used to design flexible and scalable analog output module from 1 to 4 outputs.

Table 3 shows a subset of the 16-bit resolution family. For the lower-resolution family of parts and different available configurations, contact the NXP factory.

Table 2. Part family

NAFE93352 DS[1]					
NAFE	9	3	3	5	2
NXP analog front-end	Power 3 = Low power 9 = High speed	PGA 3 = 1 and 16	Reference 3 = Factory calibrated 1 = Non-factory calibrated	Resolution (DAC-ADC) 5 = 18/24 4 = 16/16 3 = 14/16	Channels 2: 1 AIO - 2UI 1: 1 AIO 0: 1 AO

[1] Contact the NXP factory or an NXP sales representative to get further information and available part numbers.

Table 3. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
NAFE93352B40BS	FE93352	HVQFN40	Plastic thermal enhanced thin quad flat package; no leads; 40 terminals; body 6 mm x 6 mm x 0.85 mm	SOT618-20(D)

Table 4. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
NAFE93352B40BS	NAFE93352B40BSMP	HVQFN40	Reel 13" Q2 DP	4000	Ta = -40 °C to 125 °C
	NAFE93352B40BSE		Tray single DP bakeable	490	
	NAFE93352B40BSK		Tray multiple DP bakeable	2450	

Table 5. Product family

Part number	Power/speed	Factory calibration	Number of inputs/outputs	DAC Resolution [bits]	ADC resolution [bits]
NAFE93352	High speed	Yes	1x universal input/output 2x universal inputs	18	24

5 Block diagram

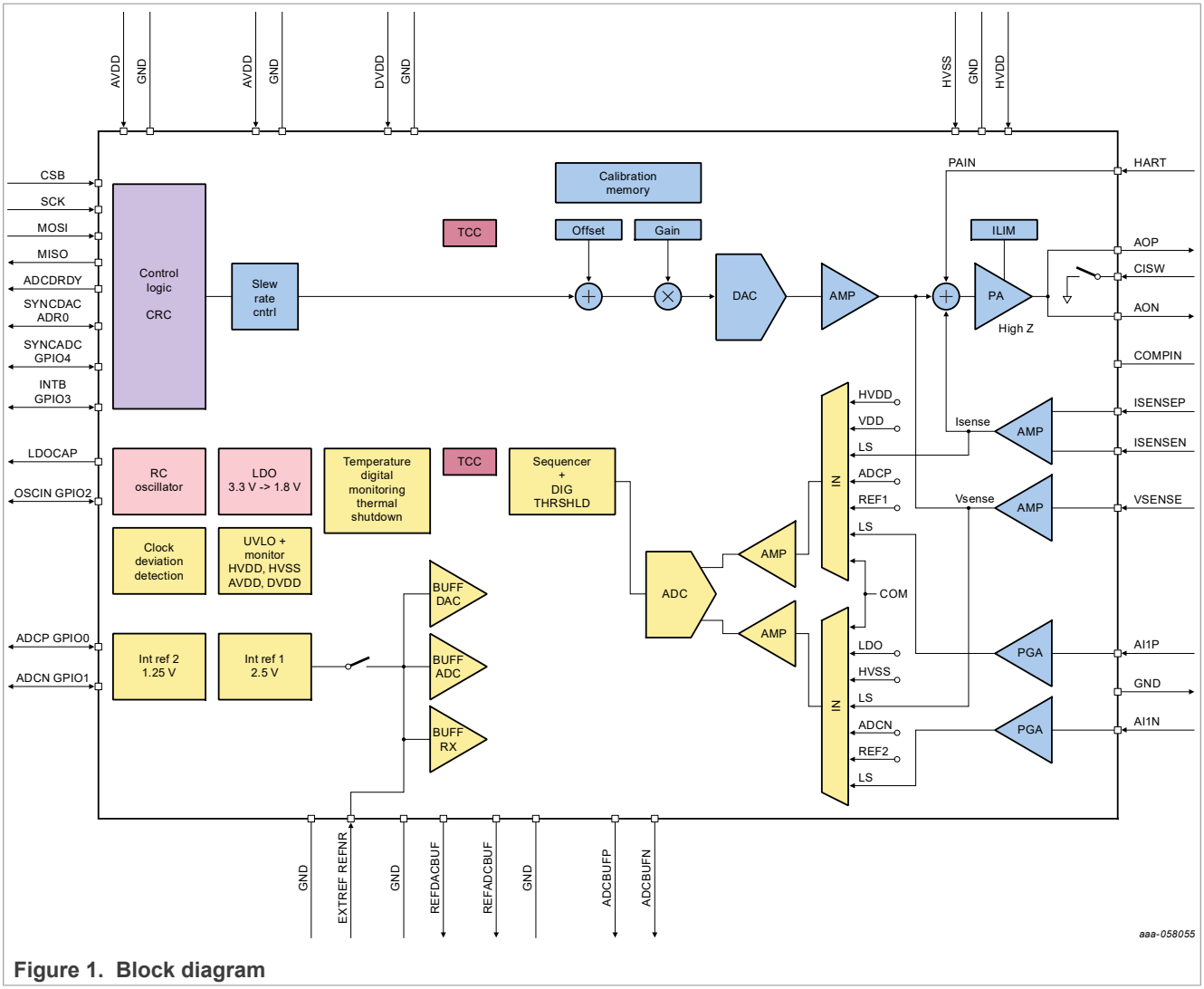


Figure 1. Block diagram

6 Pinning information

6.1 Pinning

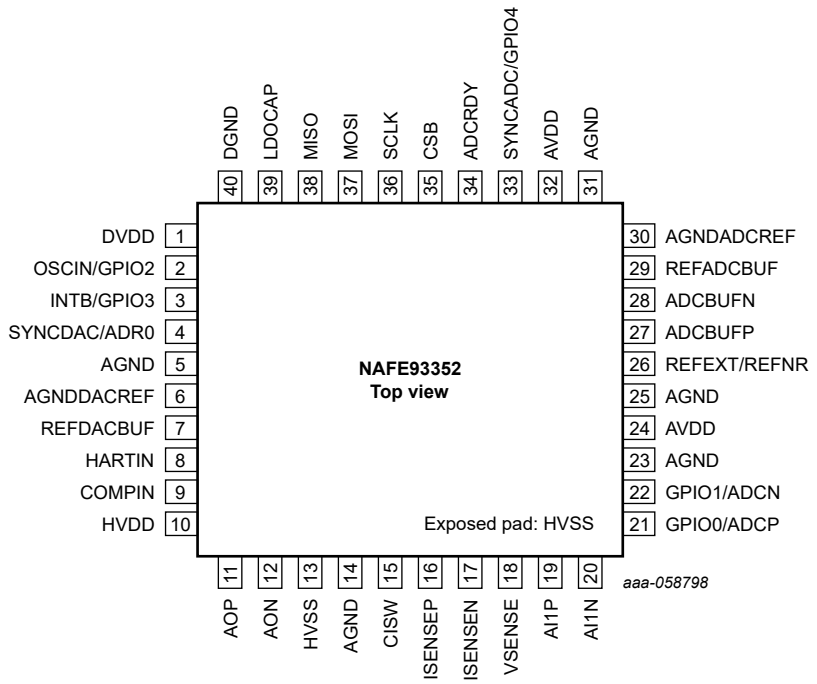


Figure 2. Top-down view, package: 6 mm x 6 mm 40 pins HVQFN

6.2 Pin description

Table 6. Pin number and pin description

Number	Name	I/O	Functional description
1	DVDD		3.3 V digital power supply.
2	OSCIN/GPIO2	DI	External clock input and GPIO2 multifunction pin. Default is an external clock input pin. It can be left floating if external clock function is not used. When it is configured as GPIO finctionality, it is functioned as a GPIO. Also refer to auto clock source selection for further details.
3	INTB/GPIO3	DO	Interrupt flag output (active-low) and GPIO3 multifunction pin. Default is INTB and it can be configured as GPIO3.
4	SYNCDAC/ADR0	DI	DAC sync input and ADR0 multifunction pin. Default is SYNCDAC and it can be configured as ADR0. It can be grounded if SYNCDAC is not used.
5	AGND		Analog ground.
6	AGNDDACREF	AI	DAC voltage reference GND sense.
7	REFDACBUF	AO	DAC voltage reference output bypass. Connect a 0.1 µF bypass capacitor close to the pin.
8	HARTIN	AI	HART signal input. A coupling capacitor is required.
9	COMPIN	AIO	External compensation for the output driver amplifier. External passive compensation network can be connected between AO and COMP_IN pins.
10	HVDD		High-voltage positive supply.

Table 6. Pin number and pin description*...continued*

Number	Name	I/O	Functional description
11	AOP	AO	High-side analog output. This pin is connected to the anode of an off-chip Schottky diode. The cathode of the Schottky diode is connected to the AIO onboard terminal through an off-chip current sensing resistor (50 Ω TYP).
12	AON	AO	Low-side analog output. This pin is connected to the cathode of an off-chip Schottky diode. The annode of the Schottky diode is connected to the AIO onboard terminal through an off-chip current sensing resistor (50 Ω TYP).
13	HVSS		High-voltage negative supply.
14	AGND		Analog ground.
15	CISW	AI	Current input switch pin (CISW). This pin is connected to the AIO onboard terminal through the current sensing resistor connected to the AOP and AON pins.
16	ISENSEP	AI	Positive input for an external current sense resistor. Must have an RC filter (5 kΩ and 100 pF).
17	ISENSEN	AI	Negative input for an external current sense resistor. Must have an RC filter (5 kΩ and 100 pF).
18	VSENSE	AI	Voltage sense input must have an RC filter (5 kΩ and 100 pF).
19	AI1P	AI	Analog input must have an RC filter (5 kΩ and 1 nF).[1] Connect to AGND if not used.
20	AI1N	AI	Analog input must have an RC filter (5 kΩ and 1 nF).[1] Connect to AGND if not used.
21	ADCP/GPIO0	AI, DI, DO	Analog input with general-purpose digital I/O. Connect to AGND if not used. Default is ADCP, and can be configured as GPIO0. Connect to AGND if not used.
22	ADCN/GPIO1	AI, DI, DO	Analog input with general-purpose digital I/O. Default is ADCN, and can be configured as GPIO1. Connect to AGND if not used.
23	AGND		Analog ground.
24	AVDD		3.3 V analog power supply.
25	AGND		Analog ground.
26	REFEXT/REFNR	AI	External reference voltage input/internal reference output bypass.
27	ADCBUFP	AO	ADC in-buffer positive output, 1 nF C0G to ADCBUFN.
28	ADCBUFN	AO	ADC in-buffer negative output, 1 nF C0G to ADCBUFP.
29	REFADCBUF	AO	ADC reference buffered output. Connect a 0.1 µF bypass capacitor close to the pin.
30	AGNDADCREF	AI	ADC voltage reference GND sense.
31	AGND		Analog ground.
32	AVDD		3.3 V analog power supply.
33	SYNCADC/GPIO4	DI	ADC sync input and GPIO4 multifunction pin. Default is SYNCADC and it can be configured as GPIO4. It can be grounded if SYNCADC is not used.
34	ADCRDY	DO	ADC data ready output, active-high.
35	CSB	DI	Chip-select input, active-low.
36	SCLK	DI	SPI clock input.
37	MOSI	DI	SPI data input.
38	MISO	DO	SPI data output.
39	LDOCAP		1.8 V regulator output bypass.
40	DGND		Digital ground.
	EP		Exposed pad (HVSS).

[1] See Section 7.6 for details.

7 Functional description

7.1 Overview

The NAFE93352 is a universal I/O software-configurable AFE for high-precision and high-accuracy measurements. The NAFE93352 platform includes a family of 1x AIO + 2x AI, 1x AIO, and 1x AO, devices pin-to-pin and firmware compatible.

Software-configurable voltage, current input/output.

All the analog input/output ranges and types have the full range or overload range 1.25 times the linear range.

The max voltage overload is ±12.5 V and the correspondent max linear range is ±10 V.

The max current overload is ±25 mA and the correspondent max linear range is ±20 mA.

Linear voltage ranges:

- ±10 V; ±5 V.
- Load resistance > 1 kΩ

In addition, the NAFE93352 fits the most common output current ranges and load resistance

- ±20 mA; 0 to +20 mA; 4 mA-20 mA
- Load resistance from 0 Ω; 1 kΩ

The NAFE93352 includes a readback path to measure voltage and current output (Vsense, Isense), and an LVMUX connection to ADC to digitize external and internal signal for condition monitoring. The combination of current output and voltage input allows measurement of the resistance and the temperature using RTD or thermistor.

The integrated programmable current output source provides a wide range of current from 1 uA to 20 mA which allows the user to measure the resistance values from 1 mΩ to 10 MΩ.

7.2 System self-calibration

The NAFE93352 is capable of system self-calibration without an external calibrator. The NAFE93352 integrates an accurate readback signal path between the DAC and the ADC, replacing the need for an external calibrator. The measurement of a known voltage source allows the gain and offset compensation of all the error sources included in the signal path. Factory-calibrated ADC can be used to calibrate the DAC, or vice-versa, to give better accuracy on the user board.

7.3 Digital factory calibration

Users who want to save time and the cost of calibration have the option to select the parts that are already digitally calibrated and don’t require further and long calibration procedures. The NAFE93352 integrates a non-volatile memory (NVM), which allows digital calibration of the AFE in the factory and stores the coefficient values for offset and gain in the NVM memory.

7.4 Precise and fast analog input/output

The NAFE93352 integrates a high-precision DAC, low-drift voltage reference and a precise high-voltage amplifier to precisely generate small and wide output signals. In addition, the DAC and the amplifier have been designed to provide fast-output response with 10 µs settling time.

The total error of end-to-end acquisition system is:

- ±0.01 % of full-scale range at 25 °C with factory calibration

- ±10 ppm of full scale/°C temperature coefficient (Voltage mode)
- ±0.05 % of full-scale range over I/O module temperature range from 0 °C to 60 °C

The NAFE93352 provides a wide range programmable data rate. The fast data rate fits systems with fast response time requirements.

DAC output data rate is determined by the host processor update rate.

The update rate is 0 ksps to 200 ksps.

To provide a fast response, the precise HV amplifiers have been designed with wide GBW product and fast slew rate for short settling time and the DAC with fast update rate and low propagation delay.

Figure 3 shows the main delay sources of the output settling time.

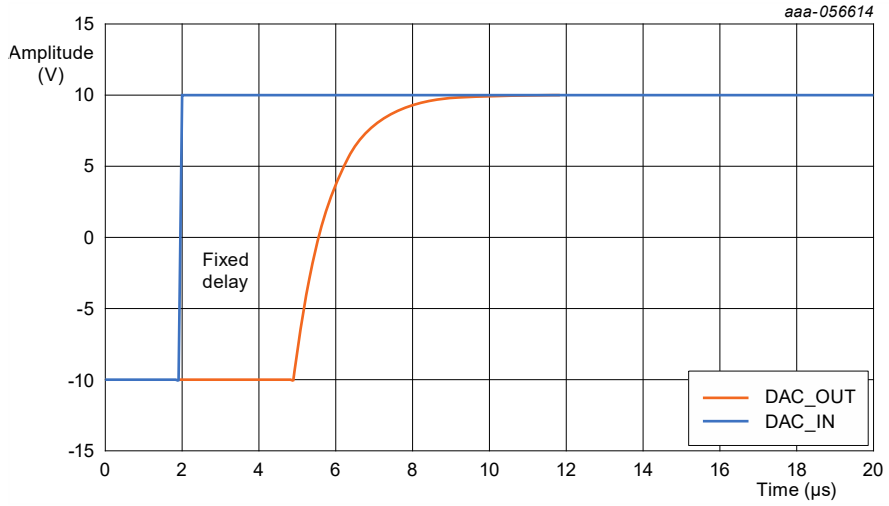


Figure 3. Main delay sources of output settling time

7.5 AO signal path

The analog output can be configured as Voltage-output mode and Current-output mode.

As shown in Figure 4, an on-chip precise DAC is used as output signal source followed by gain stage and Power Amplifier which can be configured for Voltage output, current output or High Impedance (Hi-Z state). The output of voltage feedback amplifier (VFB) and current feedback Amplifier (CFB) is routed to ADC for user to read-back. The CFB amplifier output is also used to monitor current limits and trigger protection mode to avoid damage in the system.

7.5.1 Power amplifier output

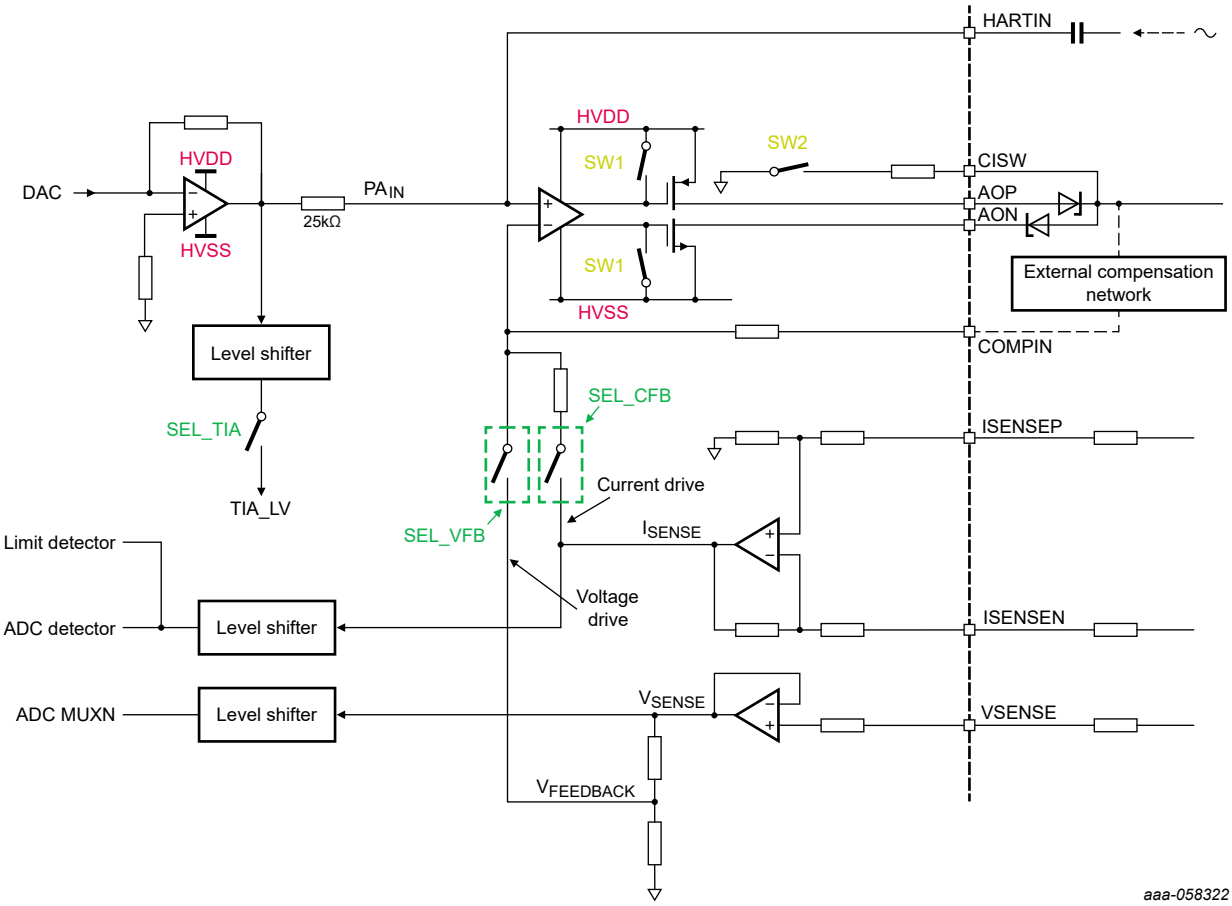


Figure 4. AO block diagram

As shown in Figure 4, there are several switches in the output stage which allow different modes of operation AO pin - high-Z, Vout, Cout, Vin, Cin.

Two switches are connected at the analog-output pin. The high-Z switch SW1 connects or disconnects the PA out to analog output pin while the ShortGND switch SW2 connect the output pin to GND.

To configure the device in Input mode or high-Z, SW1 should be open. While the SW1 is open, if the SW2 is open, the device exhibits high impedance, so it can be used for Voltage input mode. If SW1 is open and SW2 is closed, the device exhibits low impedance, so it can be used for Current-input mode.

To configure the device in Output mode, SW1 should be closed and SW2 open while the appropriate power amplifier (PA) feedback path (VFB or CFB, using SEL_VFB or SEL_CFB, respectively) is enabled (using SEL_VFB or SEL_CFB respectively). PA input feedback path can be floated for High-Z mode at the AO.

AO_MODE

Pre-configured AO modes.

1. 00\b: High-Z mode, PA_ON = 0, VSA_ON = x, CSA_ON = x
2. 10\b: Voltage-output mode, PA_ON = 1, VSA_ON = 1, CSA_ON = x
3. 11\b: Current-output mode, PA_ON = 1, VSA_ON = x, CSA_ON = 1
4. VSA ON = 1 turn ON VSA.
5. Exception: AO_MODE = 10\b

6. Voltage-output mode force VSA ON = 1, this bit cannot be overwritten.
7. CSA ON = 1 turn ON CSA.
8. Exception: AO_mode = 11\b
9. Current-output mode force CSA ON = 1, this bit cannot be overwritten.
10. CISW_ON = 1 turn on the current input SW connected to ground.
11. CISW is used in conjunction with external Rsense for Current-input mode configuration.

Note: *To avoid short-circuit, CSIW_ON should be 0\h when the PA_ON = 1 if CISW pin is connected to AOP/AON path.*

7.5.2 Output modes

NAFE93352 supports both Voltage output and Current output modes with programmable FS ranges of 12.5 V and ±25 mA, respectively.

7.5.2.1 Voltage output

NAFE93352 voltage output can drive the maximum Rload of 10 MΩ and maximum Cload of 2 µF. The output settling time depends on the combined RC loading at the AO pin.

The voltage output will settle to 0.1 % accuracy for 10 V output swing with no Rload as below:

- 50 µs with Rload = open and Cload = 20 nF
- 0.5 ms with Rload = open and Cload = 2 µF

The NAFE93352 will settle to 0.1 % of a 10 V swing within 10 µs for CL in a range of 1n F to 10 nF. If CL > 20 nF, the system can hit the current limit and overcurrent will drive the device into High-Z protection mode. In order to avoid it, the user can utilize the slew rate control to ramp up the DAC softly or utilize the current limiter to clamp the current to a specified level within the current limiter duration. The current limiter response time is dependent on the load capacitance. An external component can also be used to dampen the overvoltage and overcurrent condition at the device input pins. See Section 7.5.6 for overcurrent protection details.

7.5.2.2 Current output

NAFE93352 current output can drive the maximum Rload of 10 kΩ and maximum Lload of 1 mH.

The current output will settle to 0.1 % accuracy for a 25 mA output swing with no Rload as below:

- 50 µs with Rload = open and Lload = 47 µH
- 0.5 ms with Rload = open and Lload = 1 mH

The user can achieve fast settling and limit the maximum current during the step response by keeping load inductance below 10 µH. If Lload > 10 µH, the user can avoid overcurrent triggered High-Z protection mode by utilizing the slew rate control to ramp up the DAC softly or placing an RC filter at the HART input pin. See Section 7.5.7 for details. If required, an external component (such as a TVS diode) can be used to mitigate the current surge at the AO pin.

7.5.3 DAC output slew rate control

The slew rate control feature of the NAFE93352 allows the user to control the rate at which the output value changes. This feature is available on both the current and voltage outputs. The user can program the slew rate control parameters in register AO_SLR_CTRL defined in Table 21. With the slew rate control feature disabled, the output value changes at a rate limited by the output drive circuitry and the attached load. To reduce the slew rate, this can be achieved by enabling the slew rate control feature. With the feature enabled via the SLREN bit of the slew rate control register (see Table 8), the output, instead of slewing directly between two values, steps

digitally at a rate defined by two parameters accessible via the slew rate control register, as shown in Table 7 and Table 8.

The user can program the slew rate control parameters in register AO_SLR_CTRL defined in Table 21. The parameters are SLR_CLOCK and SR_STEP. SR_CLOCK defines the rate at which the digital slew is updated, for example, if the selected update rate is 8 kHz, the output updates every 125 µs. In conjunction with this, SLR_STEP defines by how much the output value changes at each update. Together, both parameters define the rate of change of the output value. Table 7 and Table 8 outline the range of values for both the SLR_CLOCK and SLR_STEP parameters.

Table 7. Slew rate update clock selection

SLR_CLOCK [2:0]	Update clock frequency in Hz.
0 0 0	**4000**
0 0 1	**6000**
0 1 0	**9000**
0 1 1	**12000**
1 0 0	**40000**
1 0 1	**60000**
1 1 0	**90000**
1 1 1	**150000**

Table 8. Slew rate steps

DAC's resolution	SLR_STEP							
	0	1	2	3	4	5	6	7
Step_ size: 18-bit	1024	2048	4096	8192	16384	32768	65536	131072
Step_ size: 16-bit	256	512	1024	2048	4096	8192	16384	32768
Step_ size: 14-bit	64	128	256	512	1024	2048	4096	8192
Step_ size: 12-bit	16	32	64	128	256	512	1024	2048

When the slew rate control feature is enabled, SLREN = 1, all output changes occur at the programmed slew rate. For example, if the RESET command is asserted, the output slews to the clear value at the programmed slew rate (assuming that the clear channel is enabled to be cleared). The update clock frequency for any given value is the same for all output ranges. The step size, however, varies across output ranges for a given value of step size because the LSB size is different for each output range.

The following equation describes the slew rate as a function of the step size, the update clock frequency, and the LSB size:

$$Slew\ time\ =\ Output\ change \big/ \left(Step\ size^{*}Update\ clock\ freq.^{*}LSB\ size\right)$$

Where: Slew time is expressed in seconds.

Output change is expressed in amps for IOUT_x or volts for VOUT_x.

7.5.3.1 DAC conversion during digital slew active

When DAC slew is active, new DAC codes sent from the SPI host will be ignored. The host must wait for the completion of the current DAC's conversion. Figure 5 shows the DAC's code sent from the SPI host during the DAC's output slewing active.

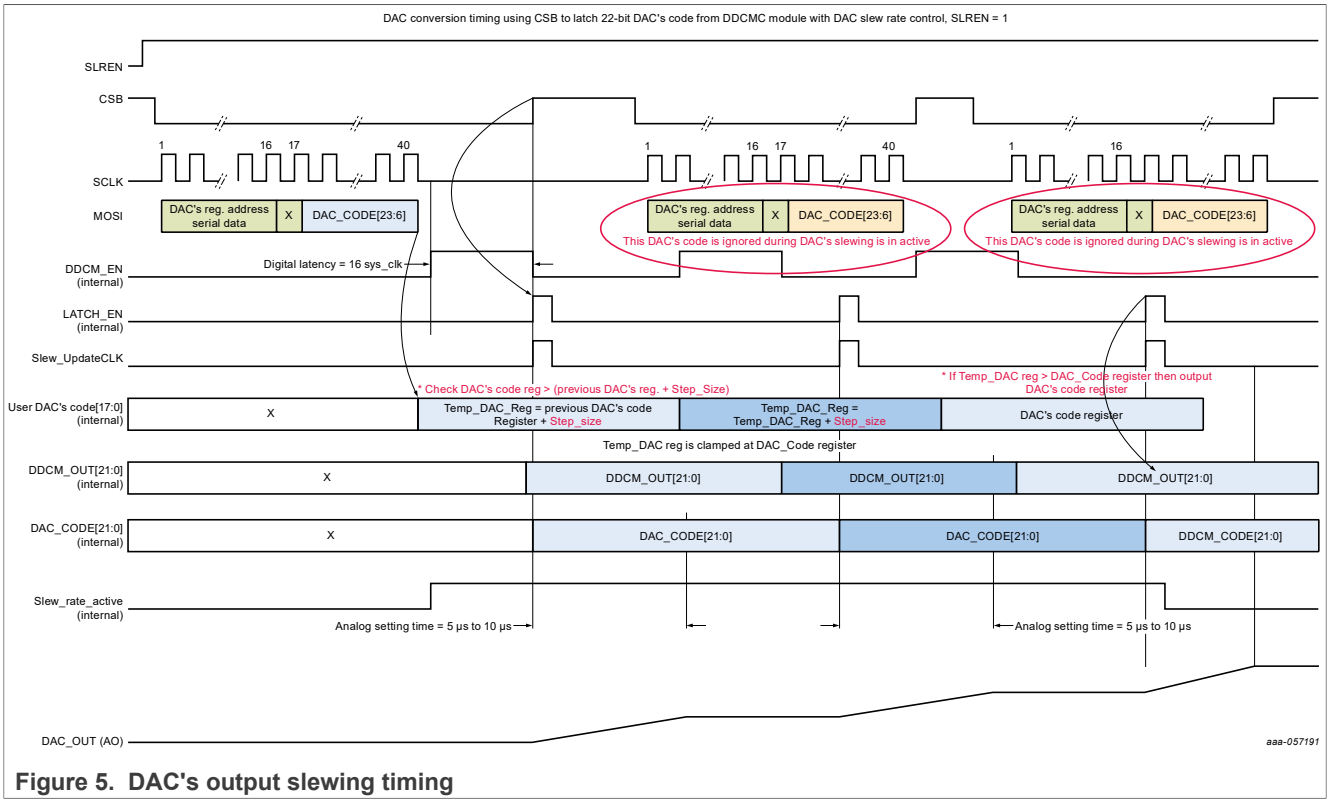


Figure 5. DAC's output slewing timing

7.5.4 Auto-DAC waveform generator

The Auto-DAC waveform generator can be triggered by the SPI host sending DAC's command CMD_WGEN. Before issuing this command, all the waveform parameters in AWG_AMP_MAX[23:0], AWG_AMP_MIN[23:0], STEP_AMP[2:0], and STEP_FREQ[2:0] registers are programmed to get the desired output waveform. See Table 21 and Table 22 for the register address of these AWG parameters. CMD_WGEN_START continuously executes until CMD_WGEN_STOP is told to stop. When the waveform generator is enabled, AIO_CHOP is ignored. The chopping feature is not supported for auto-waveform generator.

Table 9. Step frequency selection

STEP_FREQ[2:0]	Update clock frequency in Hz.
0 0 0	**4000**
0 0 1	**6000**
0 1 0	**9000**
0 1 1	**12000**
1 0 0	**40000**
1 0 1	**60000**
1 1 0	**90000**
1 1 1	**150000**

Table 10. Auto-DAC waveform generator step size

DAC's resolution	STEP_AMP[2:0]							
	0	1	2	3	4	5	6	7
Step_size: 18-bit	1024	2048	4096	8192	16384	32768	65536	131072
Step_size: 16-bit	256	512	1024	2048	4096	8192	16384	32768
Step_size: 14-bit	64	128	256	512	1024	2048	4096	8192

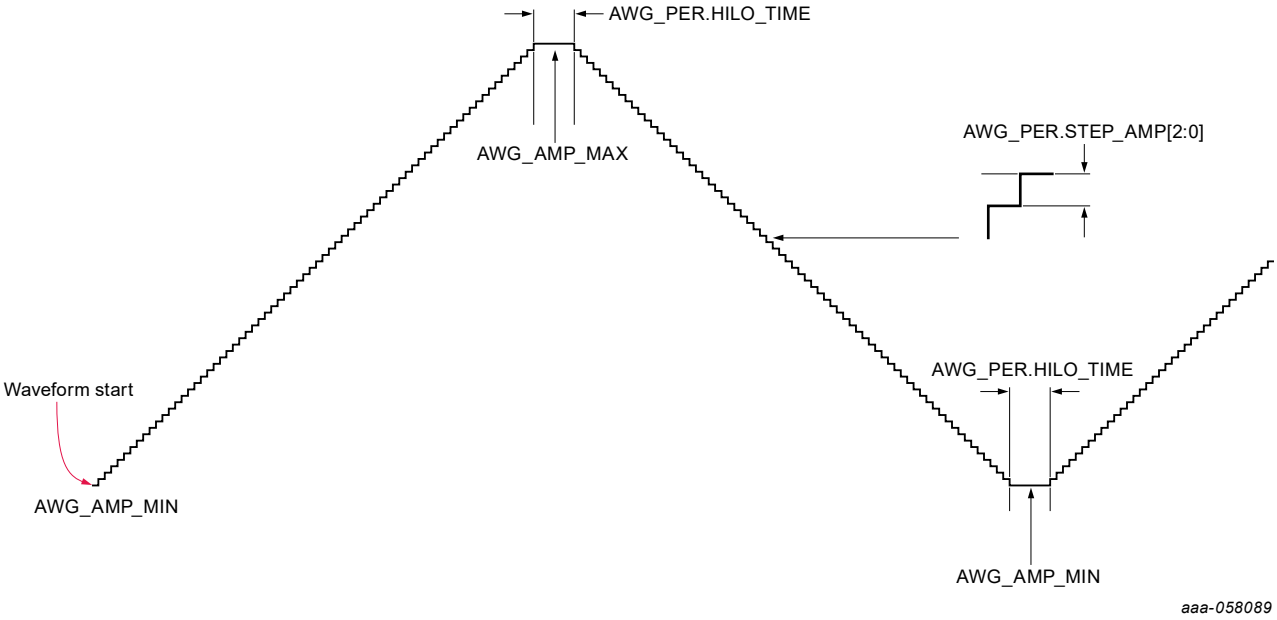


Figure 6. Auto-waveform generator timing

Note: *For some instances with different programming STEP_AMP value, AWG_AMP_MAX, or AWG_AMP_MIN value would not be possible to reach exactly. In these cases, the maximum, minimum code must be clamped to AWG_AMP_MAX, AWG_AMP_MIN value respectively.*

$$AMPmintomax\_steps = (Amp\_max - Amp\_min)/(step\_size * LSB)$$

$$AMPmintomax\_time = (AMPmintomax\_steps)/step\_freq$$

$$Waveform\_period = 2*(AMPmintomax\_time + HILO\_time)$$

$$Waveform\_freq = 1/Waveform\_period$$

For example:

For 18 bits

$$LSB = (25)/2\text{^}18 = 95.367\ \mu V$$

If Step_size(Code = 0) = 1024, Amp_max = 12.5 V, Amp_min = -12.5 V then AMPmintomax_steps = 256

If Step_period(Code = 0) = 4000, then AMPmintomax_time = 0.064 s

If HILO_time = 0, then WF_freq = 7.8125 Hz.

Table 11. Generated waveform frequency with HILO time = 0

Generated waveform frequency (Hz)		STEP_Amp (18-bit)							
		0	1	2	3	4	5	6	7
Code	Step_period (Hz)	1024	2048	4096	8192	16384	32768	65536	131072
0	**4000**	7.8125	15.6250	31.2500	62.5000	125.0000	250.0000	500.0000	1000.0000
1	**6000**	11.7188	23.4375	46.8750	93.7500	187.5000	375.0000	750.0000	1500.0000
2	**9000**	17.5781	35.1563	70.3125	140.6250	281.2500	562.5000	1125.0000	2250.0000
3	**12000**	23.4375	46.8750	93.7500	187.5000	375.0000	750.0000	1500.0000	3000.0000
4	**40000**	78.1250	156.2500	312.5000	625.0000	1250.0000	2500.0000	5000.0000	10000.0000
5	**60000**	117.1875	234.3750	468.7500	937.5000	1875.0000	3750.0000	7500.0000	15000.0000
6	**90000**	175.7813	351.5625	703.1250	1406.2500	2812.5000	5625.0000	11250.0000	22500.0000
7	**150000**	292.9688	585.9375	1171.8750	2343.7500	4687.5000	9375.0000	18750.0000	37500.0000

7.5.5 ±36 V at the screw terminal AIO pin

The IO module is protected at the AIO screw terminal pin for voltage surge (IEC61004-5) with the help of the TVS mounted on the board. The TVS should clamp the voltage within ±36 V.

The device should sustain ±36 V DC protection at the AIO screw terminal pin with the help of a Schottky diode and series resistor as reported in Figure 49.

In addition, when the device is in High-Z mode, the device should not load the AIO pin at the screw terminal up to ±36 V.

7.5.6 Overcurrent protection in Voltage-output mode

The NAFE93352 is protected against overload and short-circuit.

Since the AIO-AFE can operate in Voltage mode with different load, the current limit should be smart and configurable to adapt to different scenarios.

A typical scenario is the Voltage mode with capacitive load. In this case, during a voltage transient a surge current will happen to charge the capacitor. The slew rate, voltage-step amplitude, and load capacitor will determine the surge current. The overcurrent protection should be able to manage the short surge current to satisfy the settling time of the system. At same time, the device should be protected in case of real short.

For this reason, dual protection mechanisms are considered with a different current threshold and reaction time. The fast-reaction and high-current threshold protects against severe short-circuit, while the slow-reaction and low-current threshold protect against long-period overload.

The figures below report the time dependent threshold profile and the current surge. When the surge current is below the current protection profile, see Figure 7, the protection circuit is not activated and the AIO-AFE can charge the capacitor without interruption.

If the surge exceeds the short-circuit limit of 70 mA or lasts longer than the reaction time of 5 uA, as shown in Figure 8, the protection circuit will activate and part will go in High-Z mode. The following section explains how the user can handle such situations by using a device-programmable current limiter.

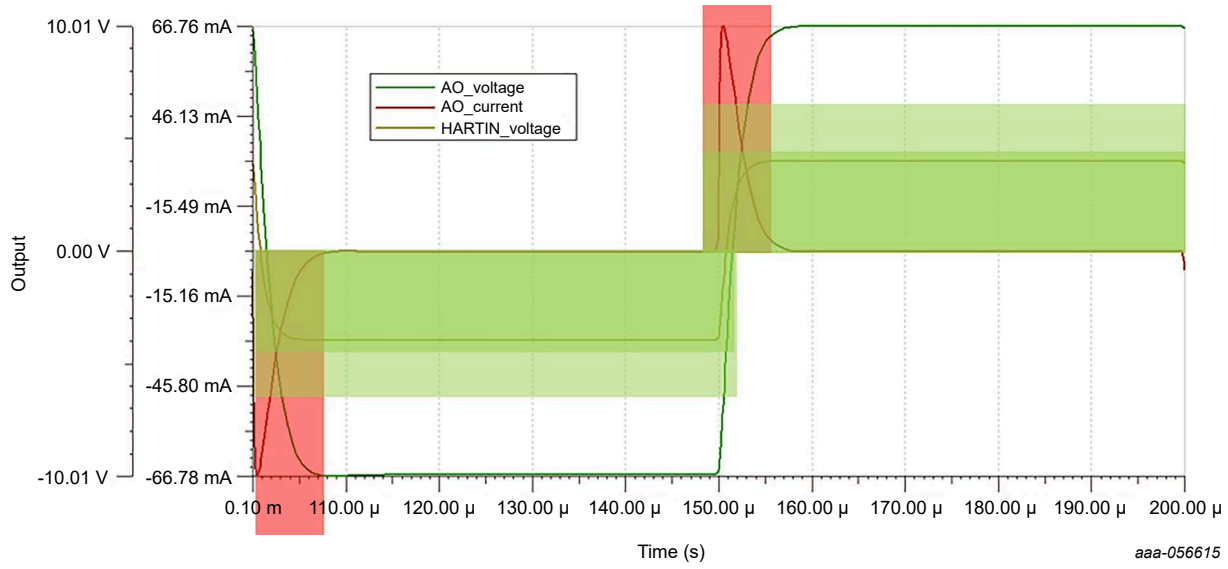


Figure 7. Current output profile in Vout mode with small CL < 10 nF

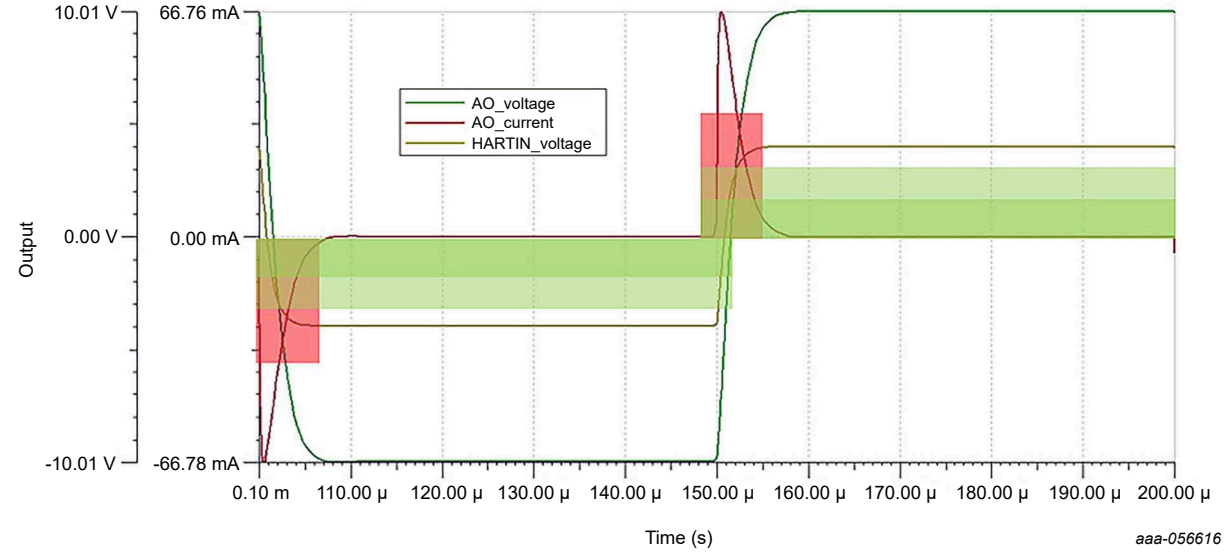


Figure 8. Current output profile in Vout mode with large CL < 100 nF

Once short-circuit is detected, the fast-current limiter limits the current to a max value of ~150 mA.

7.5.6.1 Overcurrent limits

7.5.6.1.1 Short-circuit limits

- Short current threshold ~ ±70 mA (output stage coarse current limiter)
- Reaction time < 5 µs (faster)
- The current limiter limits the maximum current at ~ ±70 mA
- Overload is detected in approximately 1 µs-2 µs, but is not activated if the overload lasts < programmable 10 µs/20 µs/50 µs/100 µs

7.5.6.1.2 Overload circuit limits

- Overload current threshold can be programmed to 5 mA, ±10 mA, ±20 mA, or ±25 mA.
  - If the overload condition happens, even after the deglitch timer, the user can handle this situation by choosing to trigger High-Z protection mode or initiate the programmable current limiter.
- Reaction time (for current limit to settle) can be programmed to 25 µs, 50 µs, 100 µs, 200 µs with default being 25 µs.
  - After the reaction time expires and if the overload (comparator output) is still active high, the output stage does the following:
    - Switch to Current-input mode and set a configured current limit output (< abs (±25) mA).
    - Set to high Z. (default Safe state)
  - The programmed current is written by the user on a shadow register. Default ±25 mA.
  - If, after a defined reaction time (current settling time), the current output is still over the current threshold, then the output stage is set in high Z. An alarm is issued and the output stage status register is updated accordingly.
  - If, after a defined reaction time (current settling time), the current output is under the current threshold, then the output stage maintains the current output for a defined period.
    - Current limiter period
      - Infinite
      - Finite = 1 ms, 2 ms, 5 ms, 10 ms
    - After the current limiter period, the digital control logic switches from Current mode to Voltage mode.

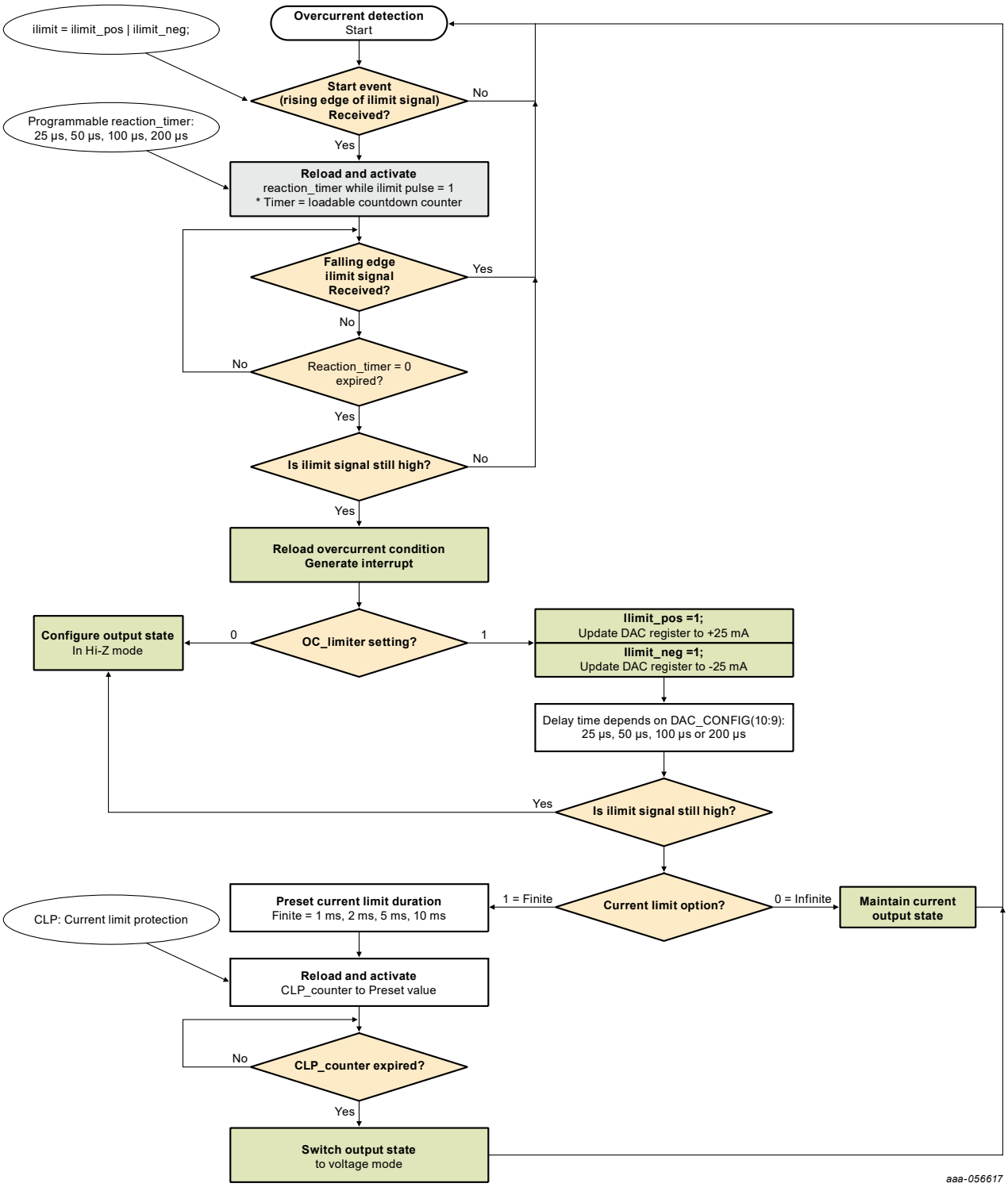


Figure 9. Overcurrent detection start

7.5.7 Overcurrent protection in Current input mode

A dedicated analog and digital circuit provides protection and detection of overcurrent to protect the device from a misused wire or fault condition.

A fast-analog circuit limits the maximum current to a safe level (~50 mA) in case of a fault. A digital, configurable circuit allows the user to set the max duration to open the CISW in case of persistent overcurrent.

Overcurrent threshold ± ~~25 mA

Overcurrent limit ± ~~50mA

The programmable period before opening the CISW after the overcurrent detection is between 50 µs to 10 ms.

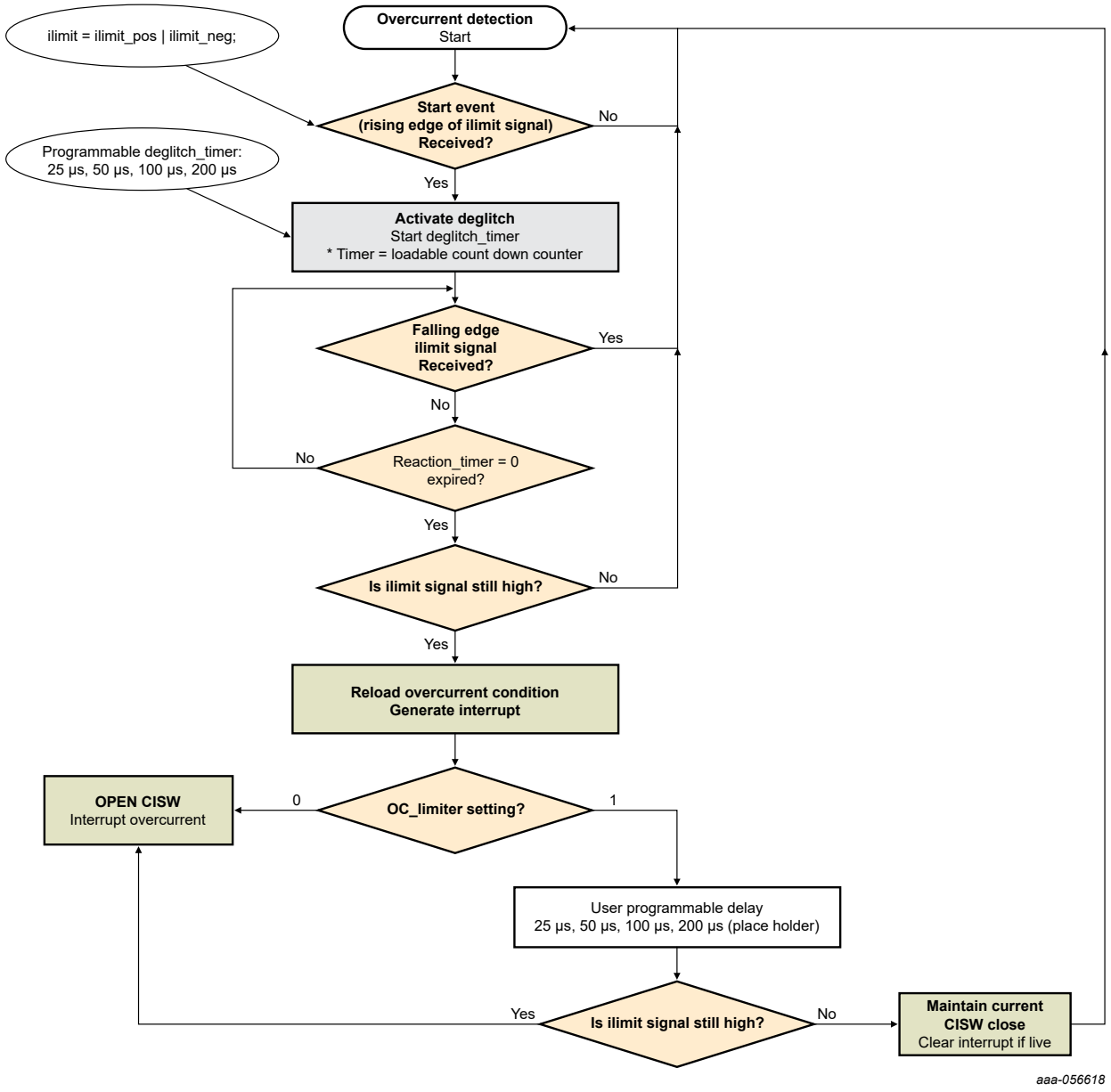


Figure 10. Overcurrent detection

7.5.8 Voltage sources polarity switching (AC excitation)

If VIEX_CHOP is set, two ADC conversions will be performed, such that the first conversion will take on the current polarity set by VIEX_POL and the second conversion will then follow with the opposite polarity. The final ADC output is an average of the differences. The DAC value will be reverted to the initial value at end of the

second conversion. This feature allows the device to compensate for offset generated internally, externally, or by input leakage current.

Moreover, by switching the polarity of the output voltage or current source, the input Common mode voltage could be removed.

The start of the second reading processes triggers the polarity change on the DAC. This allows synchronization between DAC and ADC.

If the VIEX_CHOP bit is set, upon the reading start event the ADC starts the first reading process, while the DAC uses current (initial) polarity. At the completion of the first ADC conversion, the DAC polarity is inverted and the ADC starts the second reading process. The programmable delay should be set accordingly by the user to allow TX and RX signal paths to settle.

7.6 Analog input signal paths

The analog inputs of the NAFE93352 consists of clamping circuits for electrostatic discharge (ESD) and surge protection, followed by PGA, and two input multiplexers, which route external or internal inputs to the precision ADC.

7.6.1 Analog input protection diodes and clamping

As shown in Figure 11, the external analog input pins of the NAFE are followed by clamping circuits for electrostatic discharge (ESD) and surge protection. Each input pin is equipped with input protection diodes connected to HVDD, HVSS.

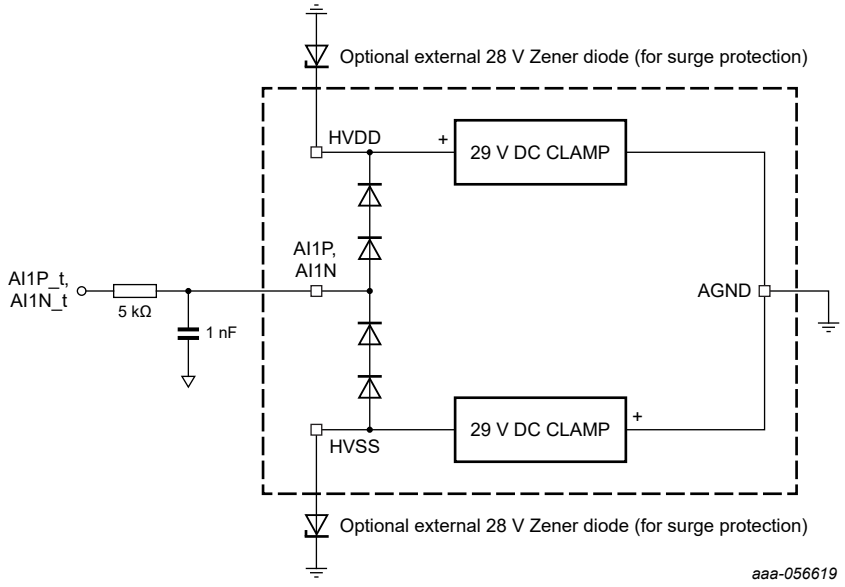


Figure 11. Analog input protection diodes and clamping

It is recommended, for reliability, that an external series 5 kΩ resistor with a 1 nF or 10 nF capacitor to AGND is installed for each HV input pin.

The integrated clamping circuits, shown in Figure 11, protect the NAFE inputs from possible surge voltage and from ESD events occurring during the manufacturing process and during printed-circuit board (PCB) assembly. If an analog input is driven below HVSS, or above HVDD, the internal protection diodes may conduct a current. A 3 kΩ or greater external series resistor is required to limit the input current to the specified value.

7.6.2 Analog input RC filter

The AI inputs must have an RC filter. This RC filter performs multiple functions - low-pass filter (LPF), current limiter, and slew-rate limiter as, as explained by the following:

- LPF: For antialiasing and to reduce external noise. An LPF with -3 dB BW < DRO/2 is recommended to achieve this. For example, an LPF with a BW < 9 kHz is recommended for a conversion data rate of 18 ksps.
- Current limiter: Set by the resistor and sized to limit the maximum current.
  - The resistor should limit the peak current to < 330 mA for a surge test with ~100 µs duration. For example, if the surge peak voltage is 1 kVp → the minimum resistance needed is 3 kΩ and a metal electrode leadless face (MELF) resistor is recommended to handle high voltage.
  - The max current should be less than 165 mA for miswiring protection. For example, if the voltage is ±36 V → the minimum resistance is 36 V/165 mA = 50 kΩ MELF resistor.
- The slew-rate limiter is set by the resistor and is sized to limit the maximum current. Slew rate must be limited to 20 V/µs for parts protection and operation. For example, if the max input step expected is 25 V (-12.5 V to 12.5 V), the input RC filter should be designed to have a time constant >1 µs. This can be achieved with a 5 kΩ resistor and a capacitor > 200 pF. NXP recommends 1 nF for most applications.

The following are the RC value recommendations for different user applications:

- 5 kΩ and 1 nF for high-speed applications (≥72 ksps). The LPF is 31.8 kHz and meets the current-limiter and slew-rate limiter requirements.
- 5 kΩ and 4.7 nF for medium-speed applications (≥12 ksps and < 72 ksps). The LPF is ~6 kHz and meets the current-limiter and slew-rate limiter requirements.
- 5 kΩ and 10 nF for low-speed applications (<12 ksps). The LPF is 3.18 kHz and meets the current-limiter and slew-rate limiter requirements.

7.6.3 HV input

The AFE is capable of measuring the differential, pseudo-differential, and single-ended signal, selecting the appropriate inputs. When the input is used in Differential mode, the AFE provides high Common mode rejection.

The differential configuration is obtained connecting the positive wire of signal to AI1P input and the negative wire of signal to AI1N input, then via software configuration selecting the respective inputs of LVMUX.

The single-ended configuration is obtained by connecting the positive wire of signal to either of the AI1P or AI1N inputs and the negative wire of signal to GND, and via software configuration by selecting the respective inputs of LVMUX.

HV input positive: AI1P, Isense

HV input positive: AI1N, Vsense

7.6.4 Transimpedance amplifier

A transimpedance amplifier (TRIAMP) is used to readback the voltage output for diagnostic purpose.

7.6.5 Programmable gain amplifier

The programmable gain amplifier (PGA) is a low-noise, programmable gain, differential-input, differential-output amplifier. Typically, the PGA is programmed to adjust the input range of the AFE to the full-scale range of input signal. The PGA has two gain options: 1 and 16.

7.6.5.1 PGA input operating ranges

The maximum input voltage of each channel gain setting is defined in Table 52.

PGA input common mode voltage range depends on PGA gain.

For cases with fully differential input voltages, the maximum allowable input common mode voltage can be calculated as below:

If $V_{in+} = VCM + V_{DIFF} / 2$ and $V_{in-} = VCM - V_{DIFF} / 2$

Then, $VCM_{max} = \left(V_{REF} - CH_{GAIN} \cdot V_{DIFF} / 2\right)$

CH_{GAIN}= 1,16

And V_{REF} = 2.5 V with internal reference voltage.

7.6.6 Analog inputs to low-voltage multiplexer (LV_MUX)

As shown in Figure 1, the input of low-voltage multiplexer is connected to PGA output, power rails supply, internal voltage reference, and the GPIO0 and GPIO1.

Table 12. Analog input selection

ANALOG INPUT SELECTION (AI_Config0 at address 0x20\h -> IN_SEL bits 7:3)					
S.No	IN_SEL	Input MUXP	Input MUXN	Measure type	Transfer function
0	00000	VCM	VCM	DIFF	Vvcm-vcm = adc_code*20*2.5/(12.5*2^24)
1	00001	AI1P	AI1N	DIFF	Vaipn = adc_code*20*2.5/(Gain*2^24)
2	00010	AI1P	VSNS	DIFF	(Vaip-Vsns)* PGA_Gain = adc_code*20*2.5/2^24
3	00011	ADCP/GPIO0	ADCN/GPIO1	DIFF	Vgpio01 = adc_code*20*2.5/(12.5*2^24)
4	00100	AI1P	VCM	SE	Vaip = adc_code*20*2.5/(Gain*2^24)
5	00101	VCM	AI1N	SE	Vain = adc_code*20*2.5/(Gain*2^24)
6	00110	ISNS	VCM	SE	Visns = adc_code*20*2.5/(3.7989*2^24), where CSA gain = 3.7989 with 5 kΩ external resistors.
7	00111	VCM	VSNS	SE	Vvsns = adc_code*20*2.5/2^24, where VSA gain = 1
8	01000	TIA	VCM	SE	Vtia = adc_code*20*2.5/(2.5*2^24)
9	01001	ADCP/GPIO0	VCM	SE	Vgpio0 = adc_code*20*2.5/(12.5*2^24) + 1.5 (VCM voltage)
10	01010	VCM	ADCN/GPIO1	SE	Vgpio1 = adc_code*20*2.5/(12.5*2^24) + 1.5(VCM voltage)
11	01011	REF_BYP	VCM	SE	REF_BYP = adc_code*20*2.5/(12.5*2^24) + 1.5 (VCM voltage) ≥ ~2.5 V
12	01100	VCM	REF_BYP	SE	REF_BYP = (adc_code-2^24)*20*2.5/(12.5*2^24) - 1.5 (VCM voltage) ≥ ~ -2.5 V
13	01101	VCM	BG	SE	BG = (adc_code-2^24)*20*2.5/(12.5*2^24) + 1.5 (VCM voltage) where adc_code > 2^23 ≥ ~1.25 V
14	01110	VADD	VCM	SE	Vavdd = adc_code*2*20*2.5/(12.5*2^24) + 1.5 (VCM voltage) ≥ ~ AVDD
15	01111	VCM	LDO	SE	LDO = adc_code*20*2.5/(12.5*2^24) + 1.5(VCM voltage) ≥ ~1.8 V
16	10000	VHDD	VCM	SE	Vhvdd = adc_code*40*20*2.5/(12.5*2^24) ≥ ~ HVDD
17	10001	VCM	VHSS	SE	Vhvss = adc_code*40*20*2.5/(12.5*2^24) ≥ ~ HVSS
18	10010	DAC_REF	VCM	SE	Vdac_ref = adc_code*20*2.5/(12.5*2^24) + 1.5 (VCM voltage) ≥ ~2.5 V

7.6.7 ADC buffer

The ADC buffer provides the necessary signal strength to drive the sampling circuit of the ADC.

7.6.8 ADC modulator

The ADC modulator is a third order sigma-delta (ΣΔ) modulator. The modulator samples the analog-input voltage at a high sample rate (fMOD = fCLK/4) and converts the analog input to a bit stream that will processed by the following digital filter.

7.6.9 ADC digital filter

The digital filter processes the modulator output data to produce the high-resolution conversion result. The digital filter filters and decimates the data. By adjusting the type of filtering, tradeoffs are made between resolution, data rate, and line cycle rejection.

The ADC digital filter consists of two SINC filter stages. The first stage is a variable-decimation SINC4 filter while the second is a variable-decimation, variable-order sinc filter. The first stage SINC4 filter averages and down-samples the modulator data (fCLK/4) to produce a high-speed data rate from 288 ksps to 6 ksps. These data outputs bypass the second filter stage, and as a result, have response characteristics of the first stage SINC4 filter. The second stage receives the first stage output data and performs additional filtering and decimation to produce data rates of 4.5 ksps to 7.5 sps in Normal settling mode.

The AIO-AFE has four configurable digital filters to optimize speed and noise performance: SINC1, SINC2, SINC3, SINC4.

The second stage order filter (in effect the data rate) is programmed by the CONFIG REGISTER bits of the register.

In addition, the AIO-AFE provides a programmable settling time (one sample, two samples, three samples, four samples) to optimize the data rate in case of multichannel system.

Section 7.6.10 shows the programmable data rate for different SINC digital filters and settling modes.

The Single-cycle settling mode is suggested for a multichannel system to avoid the settling time error, while the Normal settling mode is suggested for a single channel to get a faster data rate.

Table 13 shows the controller clock, system clock, and modulator clock.

Table 13. Clock reporting

Controller clock	18,432,000.00	Hz
System clock	9,216,000.00	Hz
Modulator clock	4,608,000.00	Hz

The system clock is 4608000 Hz and the modulator clock is 4608000/2 Hz.

7.6.10 Data rates, SINC filter orders, and Settling modes

Table 14. ADC data rate (system clock: 9.216 MHz)

		Normal settling					Single-cycle settling				
DRO code	OSR	SINC4	SINC4+ SINC1	SINC4+ SINC2	SINC4+ SINC3	SINC4+ SINC4	SINC4	SINC4+ SINC1	SINC4+ SINC2	SINC4+ SINC3	SINC4+ SINC4
0	8	576000	—	—	—	—	144000	—	—	—	—
1	12	384000	—	—	—	—	96000	—	—	—	—
2	16	288000	—	—	—	—	72000	—	—	—	—
3	24	192000	—	—	—	—	48000	—	—	—	—
4	32	144000	—	—	—	—	36000	—	—	—	—
5	48	96000	—	—	—	—	24000	—	—	—	—
6	64	72000	—	—	—	—	18000	—	—	—	—
7	96	48000	—	—	—	—	12000	—	—	—	—
8	128	36000	—	—	—	—	9000	—	—	—	—
9	192	24000	—	—	—	—	6000	—	—	—	—
10	256	18000	—	—	—	—	4500	—	—	—	—
11	384	12000	—	—	—	—	3000	—	—	—	—
12	512		9000.00	9000.00	9000.00	9000.00	—	4500.00	3000.00	2250.00	1800.00
13	768		6000.00	6000.00	6000.00	6000.00	—	3000.00	2000.00	1500.00	1200.00
14	1024		4500.00	4500.00	4500.00	4500.00	—	2250.00	1500.00	1125.00	900.00
15	2048		2250.00	2250.00	2250.00	2250.00	—	1125.00	750.00	562.50	450.00
16	4096		1125.00	1125.00	1125.00	1125.00	—	562.50	375.00	281.25	225.00
17	5760		800.00	800.00	800.00	800.00	—	400.00	266.67	200.00	160.00
18	7680		600.00	600.00	600.00	600.00	—	300.00	200.00	150.00	120.00
19	11520		400.00	400.00	400.00	400.00	—	200.00	133.33	100.00	80.00
20	23040		200.00	200.00	200.00	200.00	—	100.00	66.67	50.00	40.00
21	38400		120.00	120.00	120.00	120.00	—	60.00	40.00	30.00	24.00
22	46080		100.00	100.00	100.00	100.00	—	50.00	33.33	25.00	20.00
23	76800		60.00	60.00	60.00	60.00	—	30.00	20.00	15.00	12.00
24	92160		50.00	50.00	50.00	50.00	—	25.00	16.67	12.50	10.00
25	115200		40.00	40.00	40.00	40.00	—	20.00	13.33	10.00	8.00
26	153600		30.00	30.00	30.00	30.00	—	15.00	10.00	7.50	6.00
27	230400		20.00	20.00	20.00	20.00	—	10.00	6.67	5.00	4.00
28	307200		15.00	15.00	15.00	15.00	—	7.50	5.00	3.75	3.00

7.6.11 Frequency response

The low-pass filtering effect of the sinc filters sets the overall frequency response of the ADC.

The frequency response of data rates x sps, y sps, and z sps is that of the first filter stage.

In Normal Settling mode, the frequency response of data rates 12000 sps to 57600 sps is determined by the transfer function of SINC4, while the frequency response of data rates 2.5 sps to 9000 sps is the product of the transfer function of first digital filter stage (SINC4) and the selected digital filter of second stage (SINC1, SINC2, SINC3, SINC4).

An example of filter response is reported in Figure 12.

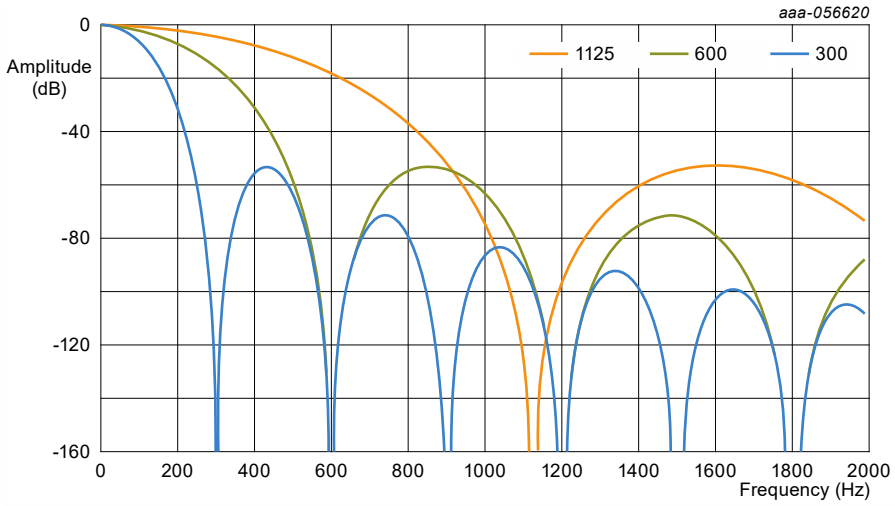


Figure 12. SINC filter transfer function

7.6.12 50 Hz/60 Hz Normal mode noise rejection

The AIO AFE features a digital filter that provide a 50 Hz and 60 Hz Normal mode rejection.

Typical transfer functions for 50 Hz and 60 Hz Normal mode rejection are reported in Figure 13 and Figure 14.

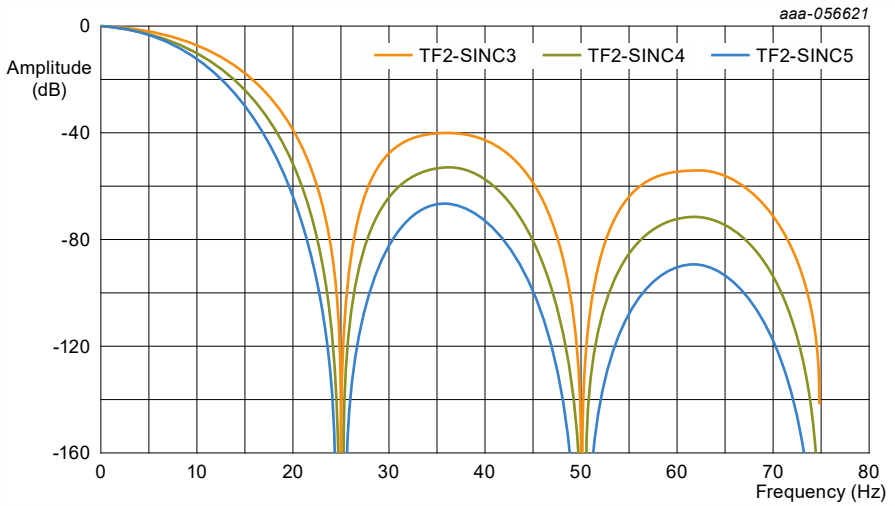


Figure 13. SINC filter transfer function

SINC4 provides enough NMR at 50 Hz.

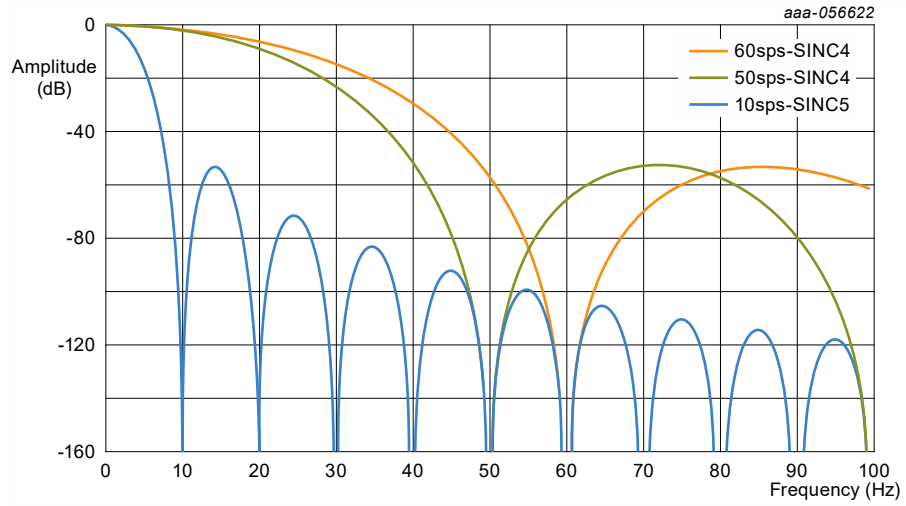


Figure 14. SINC Normal mode rejection vs frequency vs data

7.6.13 Step response

The AIO-AFE could be configured for the following Settling mode

- Normal settling: fits better for single-channel reading
- Single-cycle settling: fits better for multichannel reading

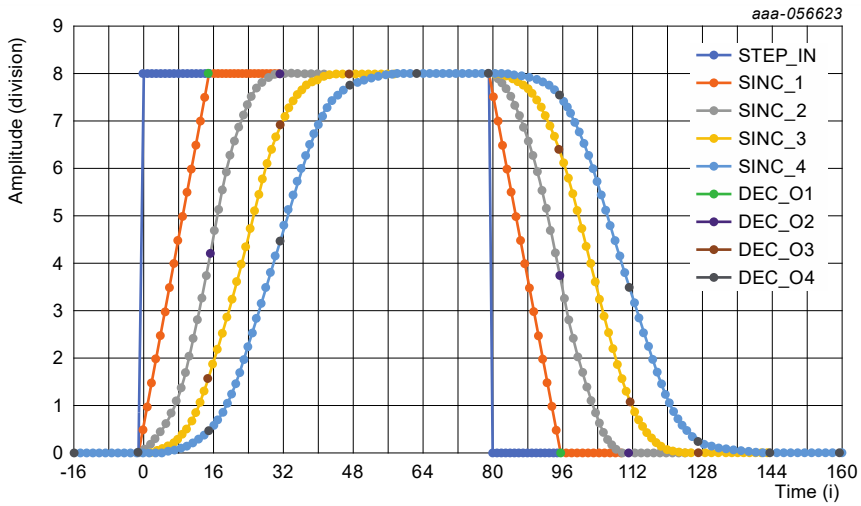


Figure 15. Transfer function SINC filter - decimator

7.6.13.1 Normal settling at 36 ksps vs. Single-cycle settling at 9 ksps

Figure 16 shows a 100 Hz digitized square wave sampled at 36 ksps. The digital filter is SINC4 and the Settling mode is set to normal. As expected during the square wave transition from low to high, the output takes four samples to settle.

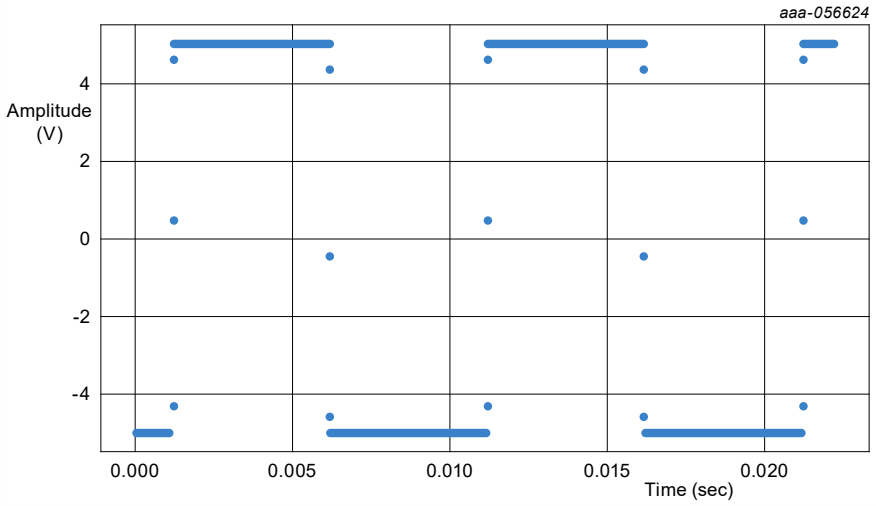


Figure 16. Normal Settling mode and SINC4

Figure 17 shows a 100 Hz digitized square wave with Settling mode set to single-cycle. The waveform is sampled at 9 ksps and the digital filter is SINC4. As expected during the square wave transition from low to high, the output takes one sample to settle.

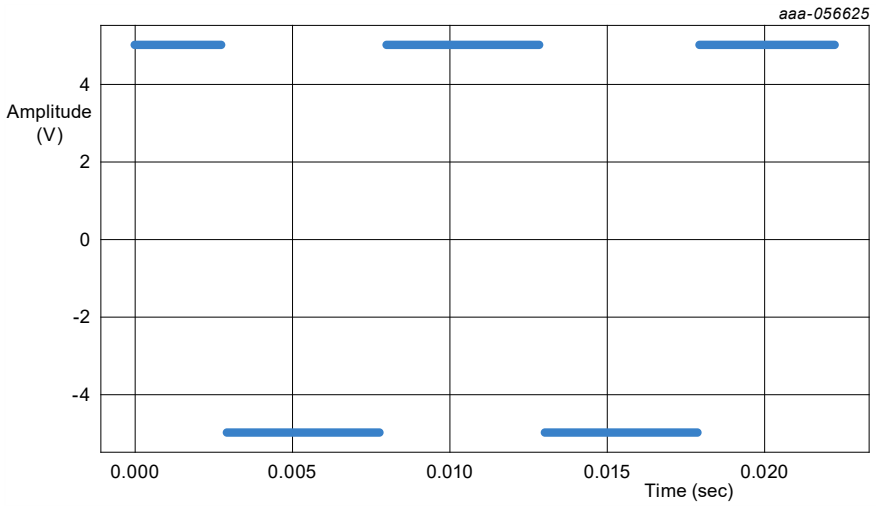


Figure 17. Single-Cycle Settling mode and SINC4

7.7 Common system

7.7.1 Voltage reference sources

7.7.1.1 Voltage reference selector

The voltage reference selector enables the selection of internal or external reference. The device uses an internal reference by default on power up and the user can assert SYS_CONFIG.REF_SEL to use an external 2.5 V reference.

7.7.1.2 Low-drift internal voltage reference 1

The AIO-AFE integrates a precise voltage reference with low-temperature coefficient to reduce the drift error overtemperature.

7.7.1.3 External-voltage reference input

The AIO-AFE features a dedicated input pin to allow the connection to an external voltage reference.

7.7.1.4 Internally buffered reference for ADC and DAC

The AIO-AFE has two independent internal buffers (sourced by either internal or external reference) to provide individual reference sources to ADC and DAC block. The ADC reference buffer is enabled by default whereas the DAC reference buffer need to be turned on by setting AO_SYSCFG.DAC_SEL_REFBUF_ON = 0x10 or 0x11 (see Table 21).

7.7.2 Temperature sensor

The AIO-AFE includes a temperature sensor to monitor the IC junction temperature with accuracy of ±3 °C.

7.7.3 General-purpose input/output

The AIO-AFE has five pins (2, 3, 21, 22, 33) that serve dual puposes and can be configured as GPIO. The operating input and output voltage ranges are 0 V to VDD when pins GPIO0..5 are configured as GPIO.

GPIO0 and GPIO1 are shared with the ADCP and ADCN (pin21 and pin22) that serve as single-ended and differential analog input by setting LVMUX. The input common voltage range for ADCP/ADCN is from 0.5 V to 2.5 V.

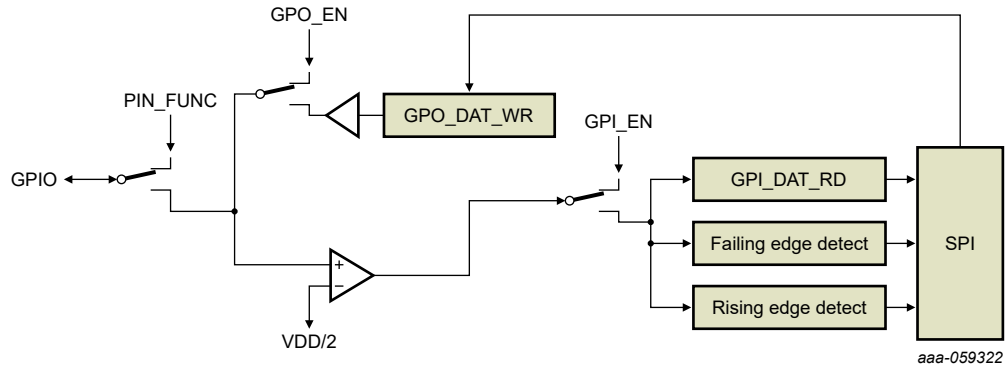


Figure 18. General-purpose input/output

The GPIO control and data registers are organized by 4x5 bits register.

1. GPI_DATA (0x23\h): Read (R) only register and it detects a level logic from the pad.
2. GPO_ENABLE (0x24\h): Read/Write (R/W) GPO_EN register. It enables an output path.
3. GPIO_FUNCTION(0X25\h): R/W PIN_FUNC register.
4. GPI_ENABLE (0x26\h): R/W GPI_ENABLE. It enables the input path to allow reading data from the pad, looping back from the GPO_DATA register and/or GPIO edges detection.

GPIO both edges detection results in 2x5-bit register 0x27 for positive and 0x28 for negative respectively are implemented as follow.

While GPI_EN = 1 and GPIO_CON =1, during any transition from 0 ≥ 1 (positive edge) or 1 ≥ 0 (negative edge), the edge detection register will be set to 1. This edge detection register is defined as a sticky by nature and require the host to clear it by writing 1 to the bit that is set to 1 (W1C).

7.7.4 Clock sources

The NAFE93352 provides flexible and configurable operating modes that can function with two different clock sources: internal RC oscillator and external oscillator.

Figure 19 shows the clock architecture.

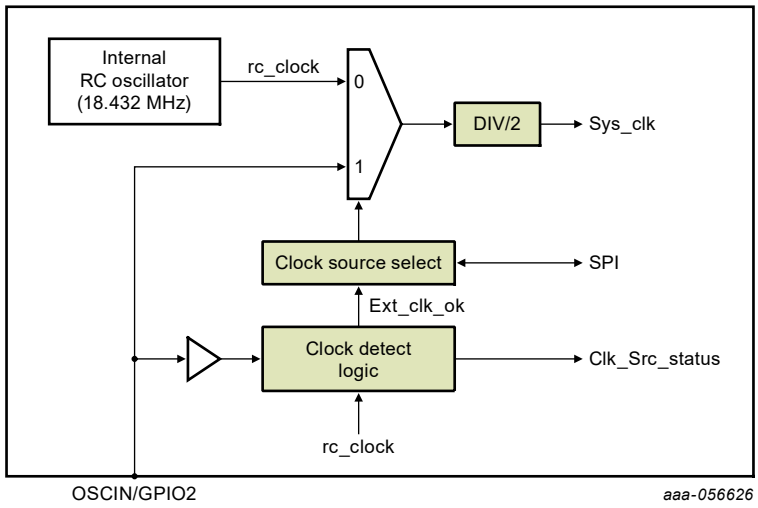


Figure 19. Clock source selector

7.7.4.1 Internal RC oscillator

The AIO-AFE integrates an internal oscillator to allow autonomous and cost-effective operation without support of any external clock source.

The internal oscillator nominal frequency is 18.432 MHz.

7.7.4.2 External oscillator

The AFE can also operate with an external oscillator to enable applications that require synchronization between the AFE and the host, as well as coherent sampling of the input signal.

The external oscillator should be applied to pin OSCIN. If not used, OSCIN can be left floating.

7.7.4.3 Clock selection

At the power on, the AFE starts with the internal RC oscillator.

The NAFE93352 provides the following mechanisms for system clock selection:

- User selection via system register configuration
  - The AIO-AFE detects the presence of the external oscillator before activating the external oscillator input.
  - If the external oscillator is not detected, the AFE continues to operate with the internal clock and provides an error message via the error status register.

See Table 23.

7.7.4.4 User selection of clock sources

The user selection option allows the user to select the desired clock after power on. The clock source can be selected by writing to the clock source system configuration register.

Check the presence of the external clock while making external clock selection in system configuration register to ensure proper functioning of the NAFE93352. If the external clock is detected and the NAFE93352 switches to the external clock, the system status register is updated accordingly. If the external clock is not detected, the NAFE93352 maintains the previous clock configuration.

7.7.4.5 Clock frequency drift detection

Whenever clock_src_sel [1:0] is set to 2'b11 or 2'b10 by the user, the clock period monitoring circuit is activated to continuously measure the clock frequency difference between the external clock and the internal RC oscillator INTOSC.

The default value of the clock frequency difference is set to 20 % at power-on reset (POR). The clock comparison logic issues an alarm when the running average clock count difference is greater than 20 %. The alarm status bit for clock variation is user accessible via SPI register. The average time window is ~64 ms. If the external clock is selected as the system clock source and while the EXTCLK_FREQ_ALRM bit is enabled, and the external clock alarm interrupt is triggered (EXTCLK_FREQ_INT = 1) whenever the EXTCLK is not within the 20 % period difference.

7.8 Reading modes

The AI-AFE provides five reading (conversion) modes with the correspondent commands.

1. Single-channel single-reading (SCSR) set by the CMD_SS command
2. Single-channel continuous-reading (SCCR) set by the CMD_SC command
3. Multichannel single-reading (MCSR) set by the CMD_MS command
4. Multichannel multireading (MCMR) set by the CMD_MM command
5. Multichannel continuous-reading (MCCR) set by the CMD_MC command

To complete a reading process, the AIO-AFE must perform a sequence of steps:

1. Idle state. Wait and sense the start event: SPI start command or SYNC pulse.
2. Update and enable the channel configuration.
3. Wait for the timer of the programmable delay to expire.
4. Start and complete ADC conversion on the selected channel.
    a. In Multichannel reading mode (MCSR, MCMR, and MCCR), the channel configuration pointer is automatically incremented to the next selected channel.
    b. In Single-reading mode (SCSR and MCSR), the AFE returns to step 1.
    c. In Continuous mode (SCCR, MCCR), jump to step 2 and repeat the cycle.
    d. In Multireading mode, MCMR jumps to step 2 until completing the reading of the last enabled channel. Then return to step 1.

In Single-reading mode (SCSR mode), the host triggers the conversion start issuing the CMD_SS or the SYNC pulse. After the reading process is complete, the device returns to waiting state and awaits the next instruction command or conversion start event from the host.

In Continuous-reading mode (SCCR and MCCR), the host starts the reading, issuing the CMD_SC, CMD_MC or the SYNC pulse. After the first reading is complete the device jumps to step 2 and continues the reading process forever or until it is interrupted or restarted.

The CMD_END, CMD_ABORT ends or aborts the conversion, respectively.

If the bit ADC_SYNC = 0, the last falling edge of the SPI command will start a new conversion. If the bit ADC_SYNC = 1, a rising edge signal at the SYNC pin will restart a new conversion based on the last valid issued reading command.

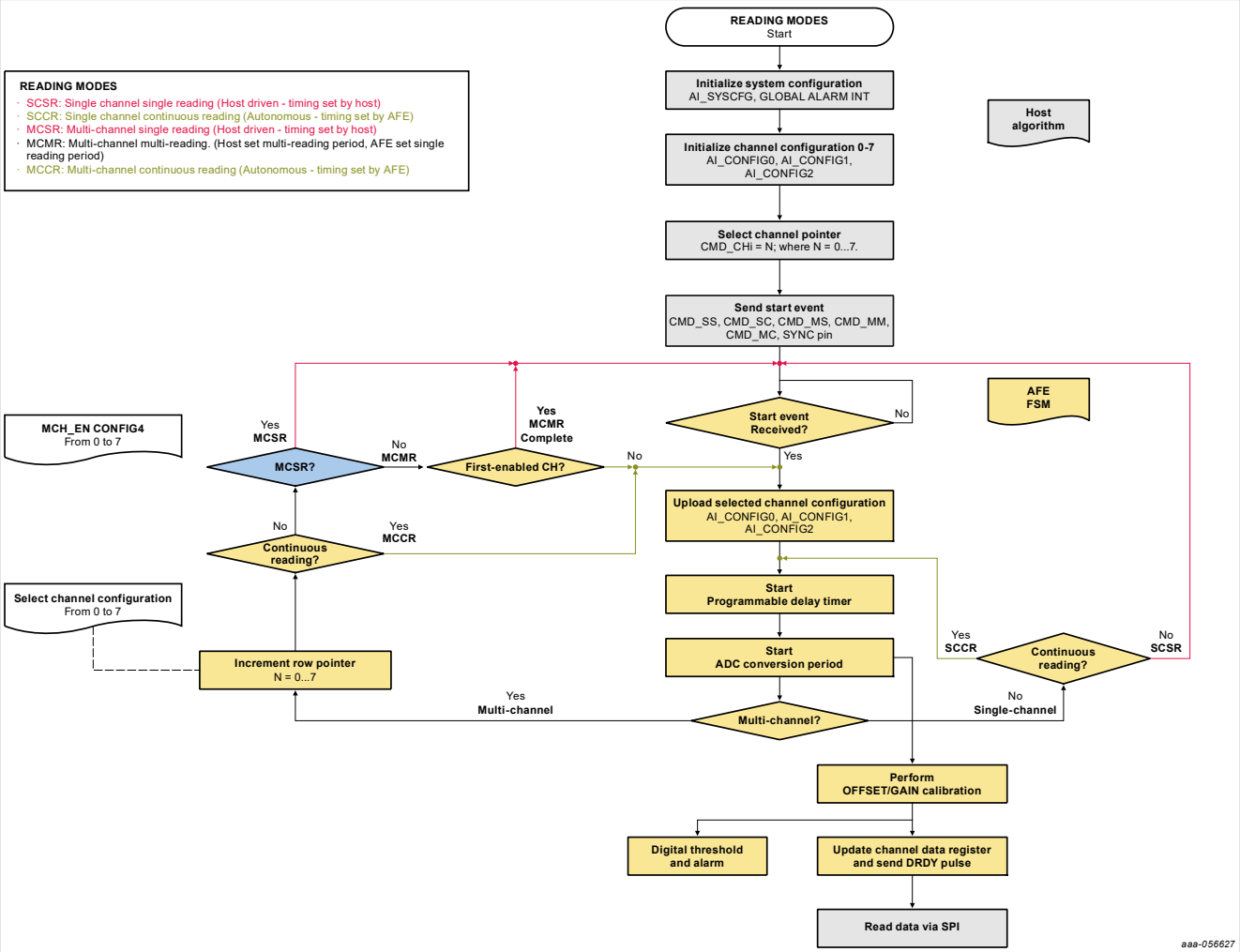


Figure 20. Reading modes flow chart

7.9 Conversion start triggers

The AIO-AFE features two types of events to trigger the conversion start: a SPI command-based event and a signal-based event at the SYNC pin.

The ADC_SYNC bit defines if the trigger is enabled on SPI command or SYNC pin.

If ADC_SYNC bit = 0, the conversion start is triggered by the last SPI clock falling edge of SPI conversion commands.

Note: *In this case the CMD_xy implements two functions, select the reading mode and trigger the conversion start.*

If ADC_SYNC bit = 0, the SPI commands that sets and starts a new conversion are as follow

1. CMD_SS is a single-channel and single-reading command
2. CMD_SC is a single-channel and continuous-reading command
3. CMD_MS is a multichannel and single-reading command

4. CMD_MM is a multichannel and multireading command
5. CMD_MC is multichannel and continuous-reading command

If ADC_SYNC bit = 1, the conversion start is triggered by a rising edge at SYNC pin.

Note: *In this case, the CMD_xy implements only the function to select the conversion mode, therefore the conversion start is only triggered by a rising edge at the SYNC pin.*

The conversion start with SYNC pulse is supported in all reading modes.

Table 15 summarizes the reading mode and start commands

Table 15. Conversion start trigger

		Conversion start trigger	
		ADC_SYNC = 0	ADC_SYNC = 1
Reading modes	SCSR	CMD_SS	SYNC pin
	SCCR	CMD_SC	SYNC pin
	MCSR	CMD_MS	SYNC pin
	MCMR	CMD_MM	SYNC pin
	MCCR	CMD_MC	SYNC pin

Table 16. Reading modes

Reading modes	Abbreviation	SPI command mnemonic
Single-channel single-reading	SCSR	CMD_SS
Single-channel continuous-reading	SCCR	CMD_SC
Multichannel single-reading	MCSR	CMD_MS
Multichannel multireading	MCMR	CMD_MM
Multichannel continuous-reading	MCCR	CMD_MC

7.10 Reading time

The reading time is function of system clock, reading mode, fixed delay, data rate and programmable delay.

- Reading modes: SCSR, SCCR, MCSR, MCMR, MCCR
- Fixed delay
- The system clock is the internal or external clock divided by 2

For example, with the internal clock at 18.432 MHz, the system clock frequency is 9.216 MHz and the period of system (T_sysclk) is 1/(9.216 MHz) = 108.5 ns.

Table 17. Programmable delay

Controller clock		**18,432,000**
System clock		**9,216,000**
Prog delay code	**Prog delay (# sysclk)**	**Delay time (s)**
0	0	000.000E+0
1	2	217.014E-9
2	4	434.028E-9
3	6	651.042E-9

Table 17. Programmable delay*...continued*

Controller clock		**18,432,000**
System clock		**9,216,000**
Prog delay code	**Prog delay (# sysclk)**	**Delay time (s)**
4	8	868.056E-9
5	10	1.085E-6
6	12	1.302E-6
7	14	1.519E-6
8	16	1.736E-6
9	18	1.953E-6
10	20	2.170E-6
11	28	3.038E-6
12	38	4.123E-6
13	40	4.340E-6
14	42	4.557E-6
15	56	6.076E-6
16	64	6.944E-6
17	**76**	**8.247E-6**
18	90	9.766E-6
19	128	13.889E-6
20	154	16.710E-6
21	178	19.314E-6
22	204	22.135E-6
23	224	24.306E-6
24	256	27.778E-6
25	358	38.845E-6
26	512	55.556E-6
27	716	77.691E-6
28	1024	111.111E-6
29	1664	180.556E-6
30	3276	355.469E-6
31	7680	833.333E-6
32	19200	2.083E-3
33	23040	2.500E-3

Note: *The data rate output (DRO) of low-power version is half of DRO of high speed for the same DRO code. For example, code 0 corresponds to 576 ksps for the HS option and 288 ksps for LP option.*

7.10.1 Reading-time calculation

The general reading time formula is:

$$Total\_reading\_time = T\_fixed + T\_prog\_delay + T\_conv$$

The fixed delay depends on the reading mode. In addition, the fixed delay is different for the first reading and subsequent readings.

7.10.2 Reading time on first reading is:

$$Total\_reading\_time = T\_fixed + T\_prog\_delay + T\_conv$$

Where

$$T\_sys\_clk = 1/System\_freq = 1/9.216\ Mhz = 108.5\ ns$$

$$T\_fixed = 2 \times T\_sys\_clk \pm 1 \times T\_sys\_clk$$

T_prog_delay = see Table 17

T_conv = 1/DRO see Table 14

Example, given

T_prog_delay set to code 16, CH_Delay = 64 counts;

T_conv set to code 2, DRO = 36000 sps.

Then

$$Total\ reading\ time = 2 * 108.5\ ns \pm 108.5\ ns + 64 * 108.5\ ns + 27.78\ \mu s = 35.05\ \mu s \pm 108.5\ ns$$

7.10.3 Reading time after first reading:

$$Total\_reading\_time = T\_prog\_delay + T\_conv$$

Where

$$T\_sys\_clk = 108.5\ ns$$

$$T\_fixed = 0 \times T\_sys\_clk$$

T_prog_delay = see Table 17

T_conv = 1/DRO see Table 14

Example, given

T_prog_delay set to code 16, CH_Delay = 64 counts;

T_conv set to code 2, DRO = 36000 sps.

Then

$$Total\ reading\ time = (0 + 64) \times T\_sys\_clk + 1/DRO = 6.95\ \mu s + 27.78\ \mu s = 34.73\ \mu s$$

7.10.4 Fastest reading time in Single-Channel Continuous-Reading mode

The fastest reading period is achievable in Single-Channel Continuous-Reading mode. In particular, after the first reading, it is possible to achieve a data rate up to 288 ksps.

7.11 Flexible data rate output with programmable delay

In addition to the programmable date rate provided by the ADC, the AFE offers further data rate output availability with the combination of ADC conversion and programmable delay.

Table 18 shows examples of the most common reading periods.

Table 18. Popular reading periods

System clock = 9,216,000						
ADC data rate (sps)	ADC conversion period (s)	Fixed delay (# sysclk)	Prog delay (# sysclk)	Prog delay (s)	Actual reading period (s)	Target reading period (s)
576000.00	1.736E-6	0	0	000.0E+0	1.7E-6	2.0E-6
576000.00	1.736E-6	0	2	217.0E-9	2.0E-6	2.0E-6
384000.00	2.604E-6	0	4	434.0E-9	3.0E-6	3.0E-6
384000.00	2.604E-6	0	6	651.0E-9	3.3E-6	3.3E-6
288000.00	3.472E-6	0	4	434.0E-9	3.9E-6	4.0E-6
288000.00	3.472E-6	0	14	1.5E-6	5.0E-6	5.0E-6
192000.00	5.208E-6	0	8	868.1E-9	6.1E-6	6.0E-6
192000.00	5.208E-6	0	12	1.3E-6	6.5E-6	6.7E-6
192000.00	5.208E-6	0	16	1.7E-6	6.9E-6	7.0E-6
144000.00	6.944E-6	0	10	1.1E-6	8.0E-6	8.0E-6
144000.00	6.944E-6	0	18	2.0E-6	8.9E-6	9.0E-6
144000.00	6.944E-6	0	28	3.0E-6	10.0E-6	10.0E-6
96000.00	10.417E-6	0	20	2.2E-6	12.6E-6	12.5E-6
96000.00	10.417E-6	0	42	4.6E-6	15.0E-6	15.0E-6
72000.00	13.889E-6	0	56	6.1E-6	20.0E-6	20.0E-6
48000.00	20.833E-6	0	38	4.1E-6	25.0E-6	25.0E-6
36000.00	27.778E-6	0	20	2.2E-6	29.9E-6	30.0E-6
36000.00	27.778E-6	0	90	9.8E-6	37.5E-6	37.5E-6
36000.00	27.778E-6	0	204	22.1E-6	49.9E-6	50.0E-6
24000.00	41.667E-6	0	76	8.2E-6	49.9E-6	50.0E-6
18000.00	55.556E-6	0	40	4.3E-6	59.9E-6	60.0E-6
18000.00	55.556E-6	0	64	6.9E-6	62.5E-6	62.5E-6
18000.00	55.556E-6	0	178	19.3E-6	74.9E-6	75.0E-6
18000.00	55.556E-6	0	224	24.3E-6	79.9E-6	80.0E-6
12000.00	83.333E-6	0	154	16.7E-6	100.0E-6	100.0E-6
9000.00	111.111E-6	0	128	13.9E-6	125.0E-6	125.0E-6
9000.00	111.111E-6	0	358	38.8E-6	150.0E-6	150.0E-6
4500.00	222.222E-6	0	256	27.8E-6	250.0E-6	250.0E-6
4500.00	222.222E-6	0	716	77.7E-6	299.9E-6	300.0E-6
2250.00	444.444E-6	0	512	55.6E-6	500.0E-6	500.0E-6
2250.00	444.444E-6	0	1,664	180.6E-6	625.0E-6	625.0E-6
2250.00	444.444E-6	0	3,276	355.5E-6	799.9E-6	800.0E-6
1125.00	888.889E-6	0	1,024	111.1E-6	1.0E-3	1.0E-3
800.00	1.250E-3	0	0	000.0E+0	1.3E-3	1.3E-3
400.00	2.500E-3	0	0	000.0E+0	2.5E-3	2.5E-3
200.00	5.000E-3	0	0	000.0E+0	5.0E-3	5.0E-3
120.00	8.333E-3	0	0	000.0E+0	8.3E-3	8.3E-3
100.00	10.000E-3	0	0	000.0E+0	10.0E-3	10.0E-3
60.00	16.667E-3	0	0	000.0E+0	16.7E-3	16.7E-3
60.00	16.667E-3	0	19,200	2.1E-3	18.8E-3	18.8E-3
50.00	20.000E-3	0	0	000.0E+0	20.0E-3	20.0E-3
50.00	20.000E-3	0	23,040	2.5E-3	22.5E-3	22.5E-3
40.00	25.000E-3	0	0	000.0E+0	25.0E-3	25.0E-3

Table 18. Popular reading periods*...continued*

System clock = 9,216,000						
30.00	33.333E-3	0	0	000.0E+0	33.3E-3	33.3E-3
20.00	50.000E-3	0	0	000.0E+0	50.0E-3	50.0E-3
15.00	66.667E-3	0	0	000.0E+0	66.7E-3	66.7E-3
15.00	66.667E-3	0	7,680	833.3E-6	67.5E-3	67.5E-3
15.00	66.667E-3	0	0	000.0E+0	66.7E-3	180.0E-3

7.12 CMD_SS, single-channel single-reading command

CMD_SS: Set Single-Channel Single-Reading (conversion) mode.

If bit ADC_SYNC = 0, the conversion start is triggered by this SPI command at the last SPI clock falling edge.

If bit ADC_SYNC = 1, the conversion start is triggered by SYNC rising edge.

In both cases, the conversion is executed on the selected channel.

After the conversion completion, the device returns to waiting state.

Data can be read serially via the MISO pin after the DRDY pin asserts high or after the reading is completed.

7.12.1 Single-Channel Single-Reading mode flow chart

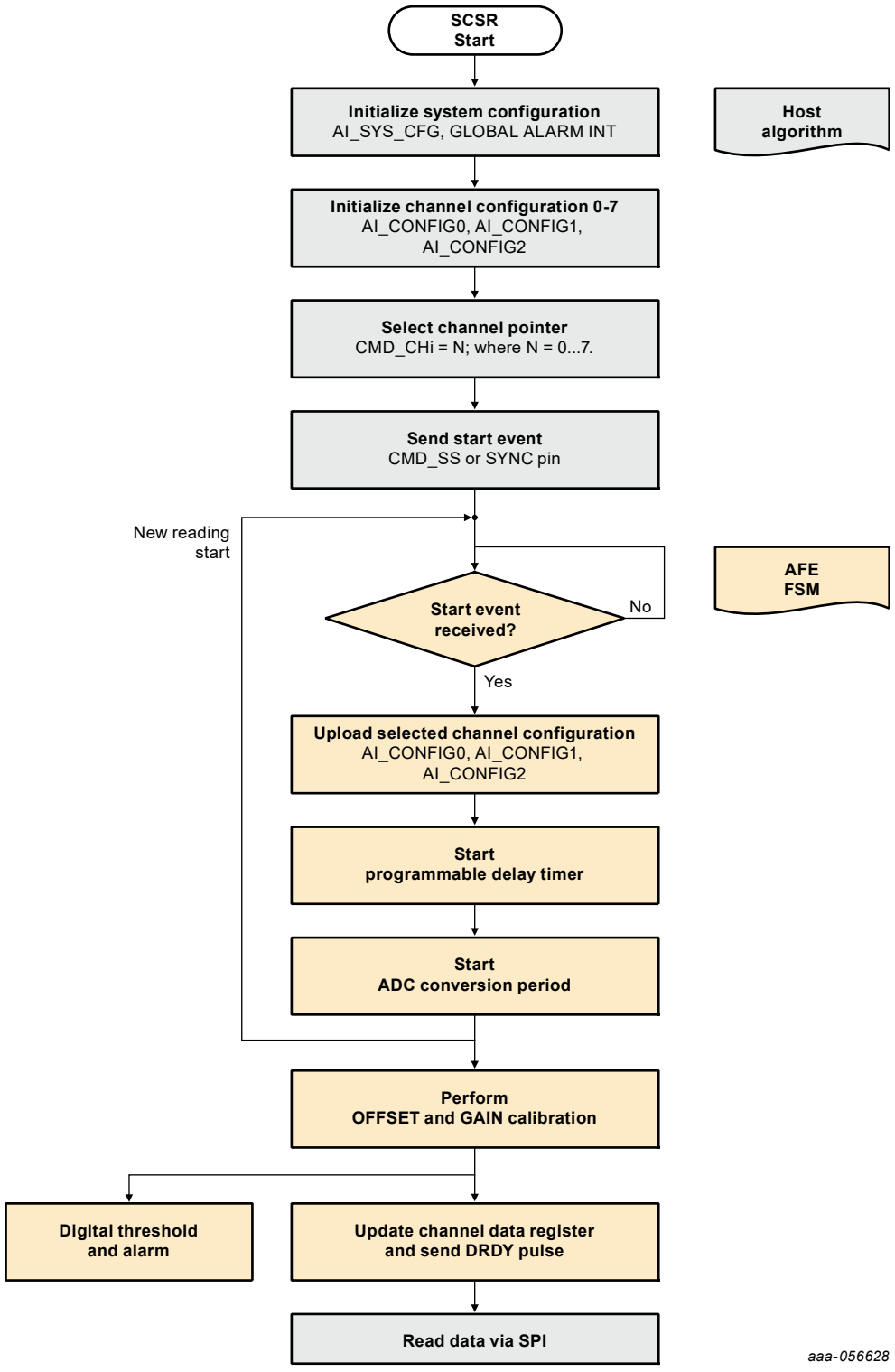


Figure 21. SCSR flow chart

7.12.2 Example code sequence

```
Reg_write (`SYS_CONFIG, config_data); //
Reg_write (`CH_CONFIGi, config_data); // i = 0…to . 7
Set CMD_CHi; // i = 0…to . 7
Send CMD_SS;
```

7.12.3 Single-channel single-reading timing diagram

Host can fetch single channel data after AFE reading period by the two methods:

1. Keeping the CSB low after command was issued.
2. De-asserting the CSB high, then waiting for DRDY goes low and fetch the channel data.

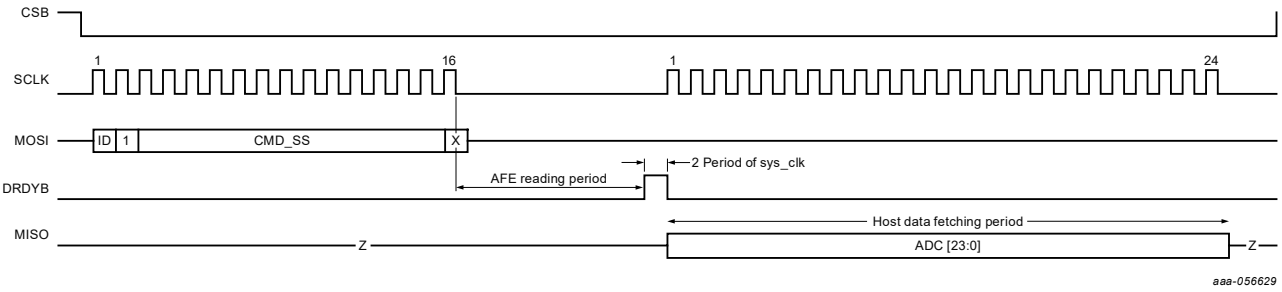


Figure 22. Single-channel single-reading timing diagram with CSB stays low after CMD_SS

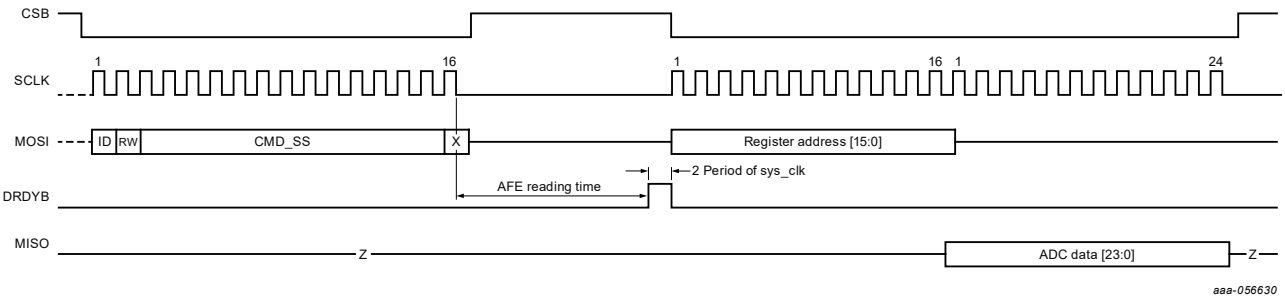


Figure 23. Single-channel single-reading timing diagram with CSB asserts high after CMD_SS

7.13 CMD_SC, single-channel continuous-reading command

CMD_SC sets Single-Channel Continuous-Reading (conversion) mode.

If bit ADC_SYNC = 0, the conversion start is triggered by this SPI command at the last clock falling edge.

If bit ADC_SYNC = 1, the conversion start is triggered by SYNC rising edge.

In both cases, the conversions are executed on the selected channel until they are interrupted or restarted. The conversion could be interrupted by CMD_ABORT and CMD_END or could be aborted and restarted by SYNC pulse if ADC_SYNC = 1 or any conversion command if ADC_SYNC = 0.

Data can be read serially via the MISO pin after the DRDY pin asserts high or after the reading is completed.

7.13.1 Single-Channel Continuous-Reading mode flow chart

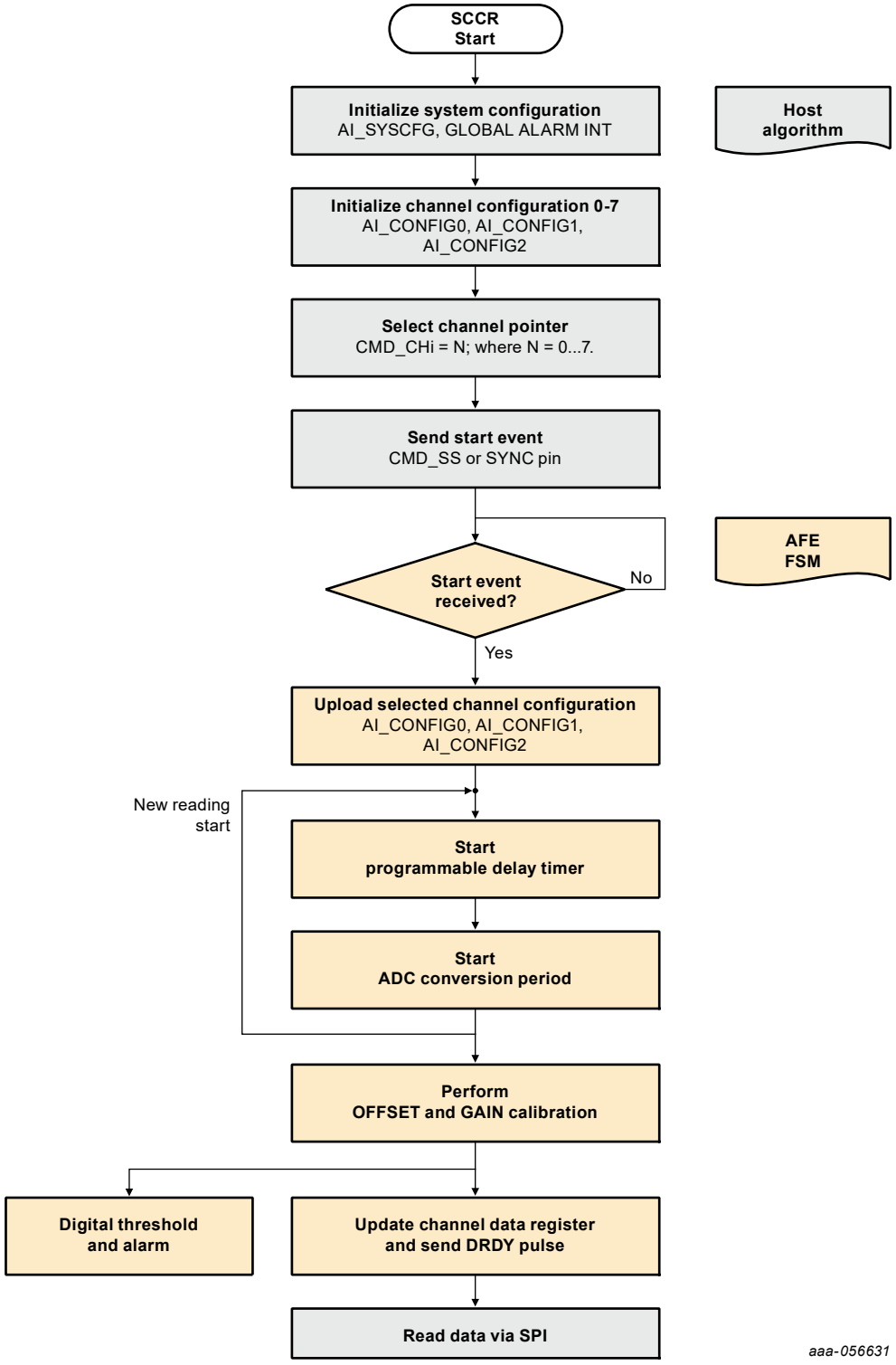


Figure 24. SCCR flow chart

7.13.2 Example code sequence

```
Reg_write (`SYS_CONFIG, config_data);
Set CMD_CHi; // i = 0…7
Reg_write (`CH_CONFIGi, config_data); // i = 0…7
Send CMD_SC;
```

7.13.3 Single-channel continuous-reading timing diagram

The reading time for a single-channel continuous-reading is reported in the following equation. For the detailed analysis on reading time, see Section 7.10.

$$AFE\ reading\ first\ period\ =\ T\_fix\_delay\ +\ T\_prog\_delay\ +\ T\_conv;$$

If ADC_FILTER_RESET = 1;

$$AFE\ reading\ second\ period\ and\ after\ =\ T\_prog\_delay\ +\ T\_conv;$$

If ADC_FILTER_RESET = 0;

$$AFE\ reading\ second\ period\ and\ after\ =\ T\_conv;$$

Where

$$T\_sys\_clk\_sync\ =\ 2{*}108.5\ ns\ \pm\ 108.5\ ns$$

$$T\_fix\_delay\ =\ 6.076\ \mu s$$

T_prog_delay = see Table 17

T_conv = 1/DRO, see Table 14

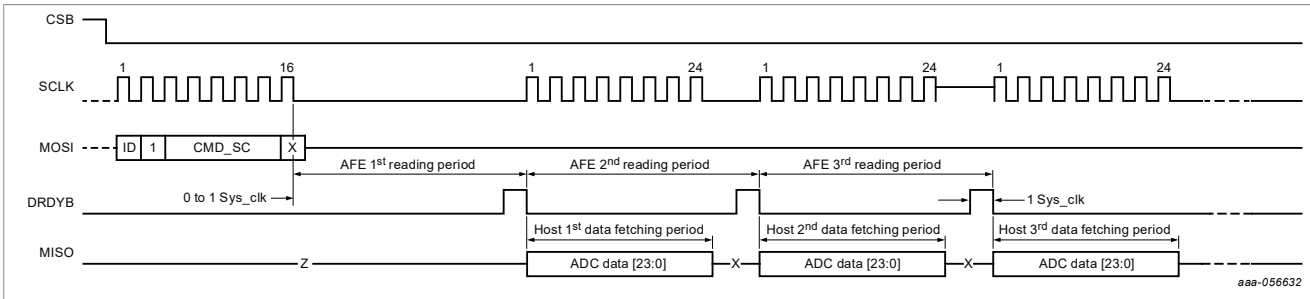


Figure 25. Single-channel continuous-reading timing diagram CSB low

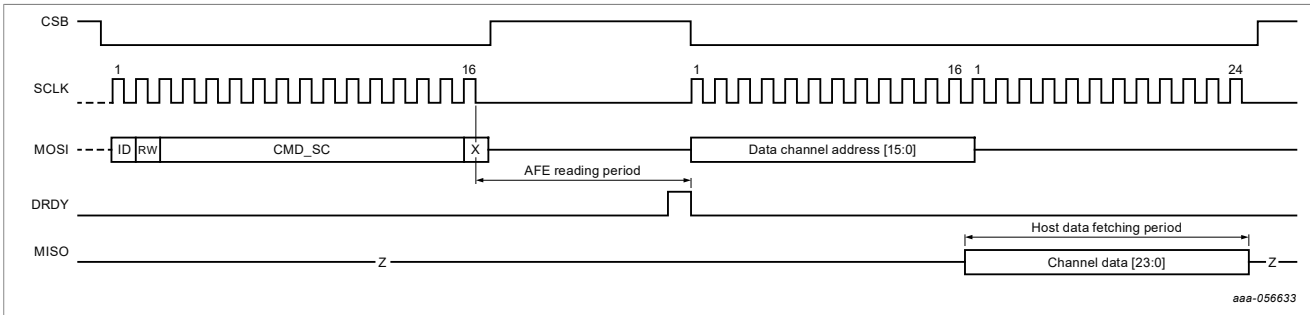


Figure 26. Single-channel continuous-reading timing diagram CSB high

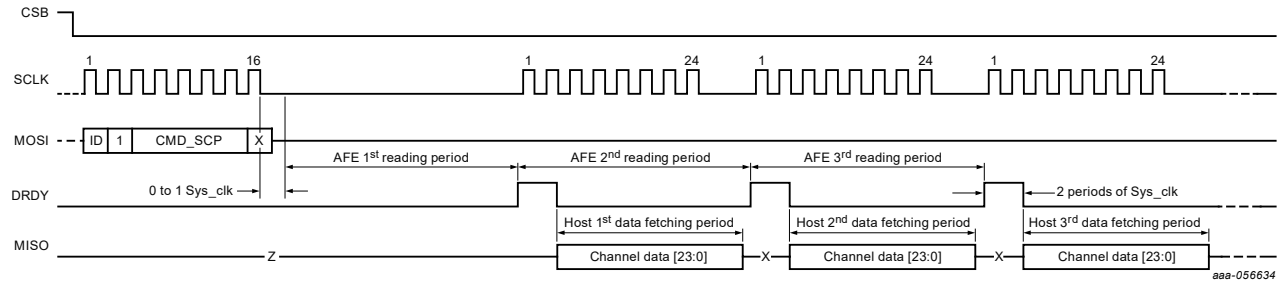


Figure 27. Data capture with CMD_SC method 1

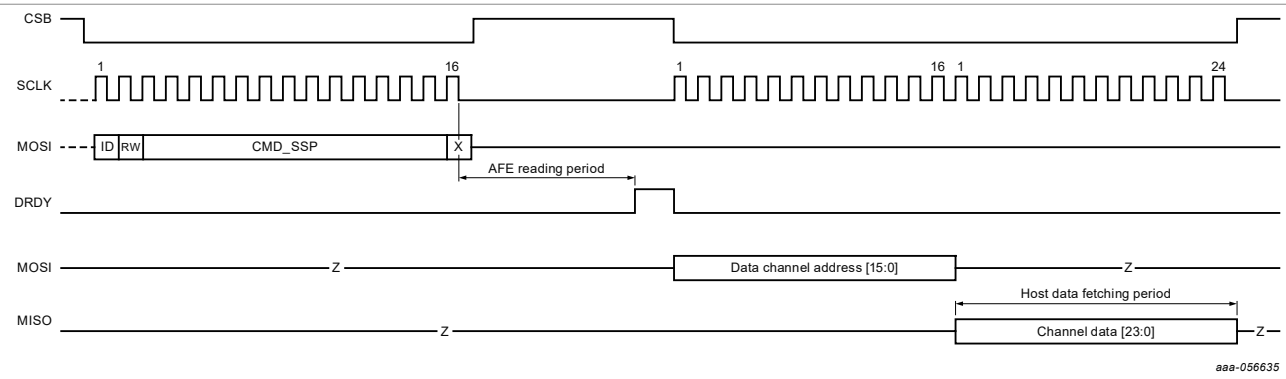


Figure 28. Data capture with CMD_SC method 2

7.14 CMD_MM, multichannel multireading command

CMD_MM: Set Multichannel Multireading (conversions) mode.

If bit ADC_SYNC = 0, the conversion start is triggered by this SPI command at the last clock falling edge.

If bit ADC_SYNC = 1, the conversion start is triggered by SYNC rising edge.

After the first conversion, the sequencer will start the conversion by sequencing on the enabled channel set via MCH_EN[15:0] register, from CH0 to CH15. After the conversion completion of the last enabled channel, the device returns to the waiting state.

The conversion could be interrupted by CMD_ABORT and CMD_END or could be aborted and restarted by SYNC pulse if ADC_SYNC = 1 or any conversion command if ADC_SYNC = 0.

If a SPI conversion CMD or a SYNC pulse is issued before completion of the current conversion, ADC will abort the conversion immediately and restart the conversion, starting from the first enabled channel.

Data can be read serially via the MISO pin after the DRDY pin asserts high or after the reading is completed.

7.14.1 Multichannel Multireading mode flow chart

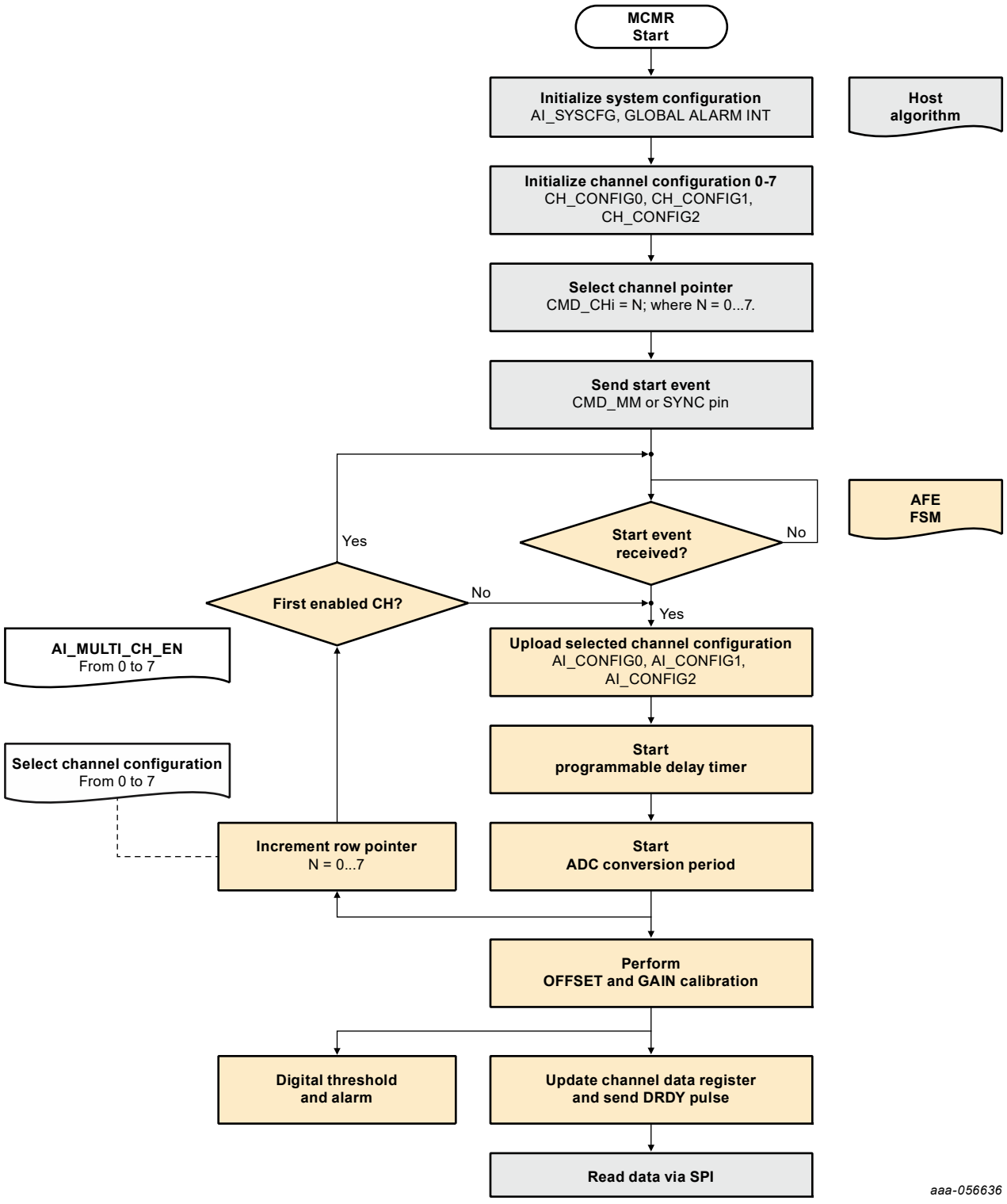


Figure 29. MCMR flow chart

7.14.2 Example code sequence

```
Reg_write (`SYS_CONFIG, config_data);
Reg_write (`CH_CONFIGi, config_data); // i = 0…7
Send CMD_MM;
```

7.14.3 Multichannel multireading timing diagram

The timing diagram for a multichannel multireading is shown in Figure 30. For the detailed analysis on reading time, see Section 7.10.

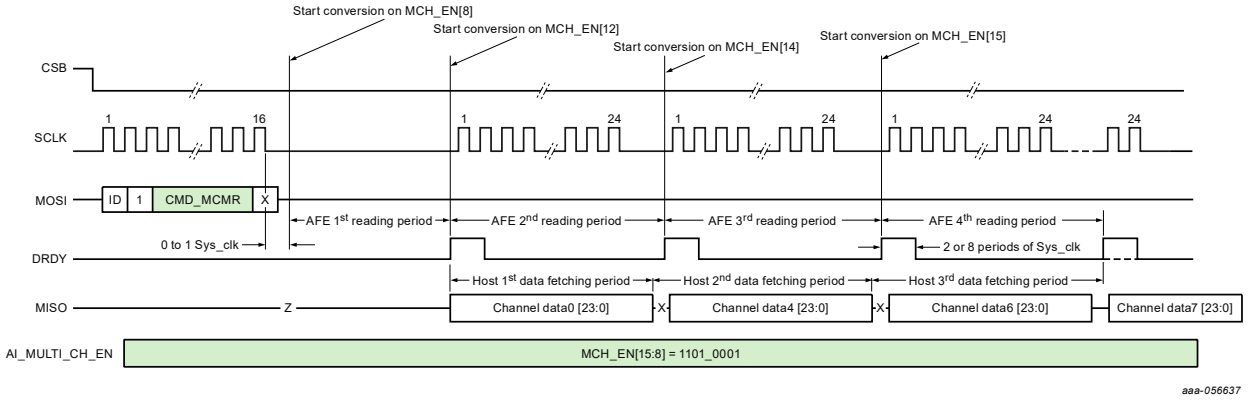


Figure 30. MCMR timing

Channel 0, 4, 6, and 7 are enabled in multichannel conversion, as shown in Figure 30, MCH_EN = 1101_0001. The sequencer generates four conversion results based on the four configurations stored at these respective locations 0, 4, 6, and 7 in the sequencer table.

7.15 CMD_MC, multichannel continuous-reading command

CMD_MC sets Multichannel Continuous-Reading (conversions) mode.

If bit ADC_SYNC = 0, the conversion start is triggered by this SPI command at the last clock falling edge.

If bit ADC_SYNC = 1, the conversion start is triggered by SYNC rising edge.

After the first conversion, the sequencer will start the conversion by sequencing on the enabled channel set via MCH_EN[15:8] register, from CH0 to CH7. After the conversion completion of last enabled channel, the device restarts a new cycle in an infinite loop.

The conversion could be interrupted by CMD_ABORT and CMD_END or could be aborted and restarted by SYNC pulse if ADC_SYNC = 1 or any conversion command if ADC_SYNC = 0.

If a SPI conversion CMD or a SYNC pulse is issued before completion of the current conversion, ADC will abort the conversion immediately and restart the conversion starting from the first enabled channel.

Data can be read serially via the MISO pin after the DRDY pin asserts high or after the reading is completed.

7.15.1 Multichannel continuous-reading mode flow chart

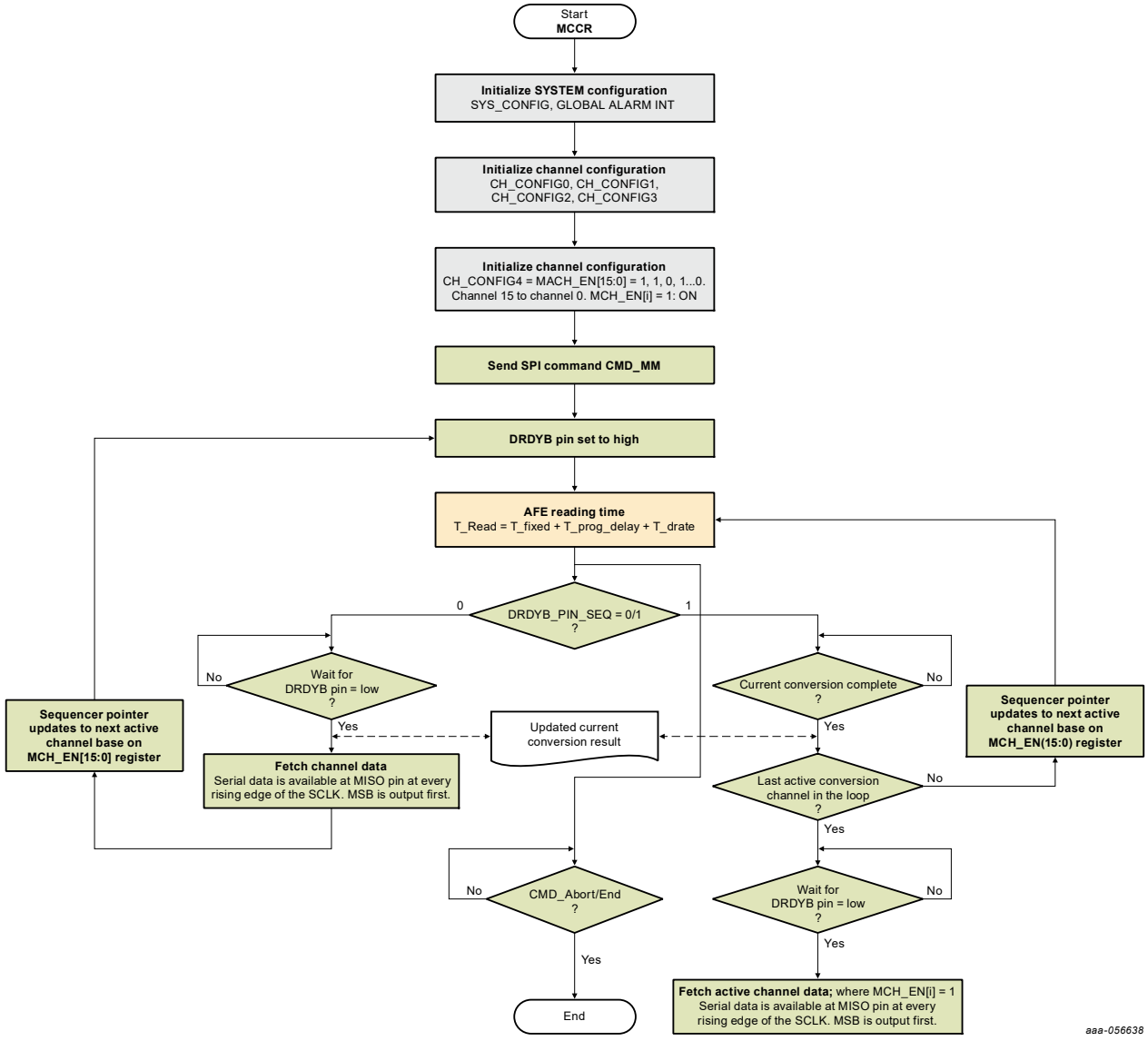


Figure 31. MCCR flow chart

7.15.2 Example code sequence

```
Reg_write (`SYS_CONFIG, config_data);
Reg_write (`CH_CONFIGi, config_data); // i = 0…7
Send CMD_MC;
```

Channels 0 and 7 are enabled in multichannel conversion as shown in Figure 31, MCH_EN[15:8] = 1000_0001. For CMD_MC command, the sequencer generates looping through two conversions based on the two configurations stored at these respective locations (0 and 7) in the sequencer table. The conversions keep running through the loop until CMD_ABORT or CMD_END are issued.

7.15.3 Multichannel continuous-reading timing diagram

The timing diagram for a multichannel continuous-reading is shown in Figure 32. For a detailed analysis of the reading time, see Section 7.10.

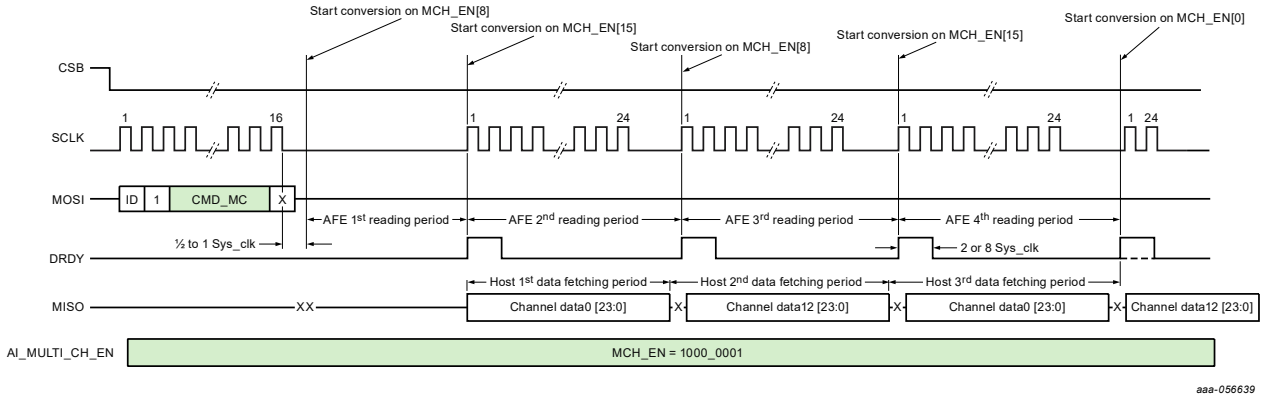


Figure 32. MCCR timing

7.16 SYNC signal as conversion start event

If ADC_SYNC = 1, a new ADC conversion will start at each rising edge of the SYNC pulse at the pin.

If there is a conversion in progress when the SYNC pulse is issued, the reading in progress will be aborted and a new reading based on the last sent command conversion will start.

The SYNC pulse width should be a minimum of 1 system clock cycles 108.5 ns.

Figure 33 shows an ADC conversion triggered by pulse at the SYNC pin in Single-Channel Continuous-Reading mode (CMD_SC). The Continuous-Reading mode, in combination with SYNC, allows the fastest reading mode while requiring only one SYNC pulse to collect many or infinite reading samples. In addition, it mitigates the timing requirements for fetching channel data on the SPI bus. In fact, the fetching period is close to the reading period for the second reading and beyond.

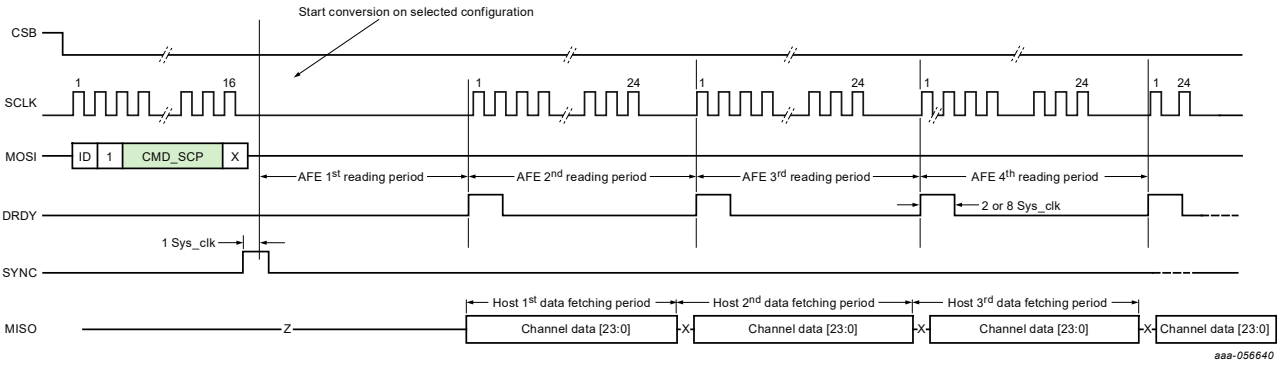


Figure 33. CMD_SC with SYNC trigger timing diagram and CSB low

Note: *NAFE93352 Rev. A silicon supports the start event triggered by a SYNC pulse on single-channel reading modes, CMD_SS and CMD_SC.*

7.17 Conversion stop command and signal

The conversion stop signal could be issued by SPI commands. The SPI commands to stop reading in progress are CMD_ABORT and CMD_END.

7.17.1 Abort command

While the AIO-AFE reading period is active and ADC is converting, if CMD_ABORT command is received, the ongoing conversion is aborted, and the device returns to initial waiting state. The corresponding CH_DATA register will not be updated.

7.17.2 End command

While the AIO-AFE reading period is active and the ADC is converting, if CMD_END is received, the ongoing conversion is completed, and the device returns to its initial waiting state. The CH_DATA register will be updated.

7.18 ADC synchronization

The AIO-AFE supports four different types of synchronization.

1. Synchronization of Multi AIO-AFE with a SYNC pulse at the SYNC pin.
2. Synchronization of the AIO-AFE to host conversion starts through SYNC pulse.
3. Synchronization of the host to AIO-AFE DRO through DRDY signal.
4. Synchronization of the AIO-AFE and the host clock to the same controller clock using the external clock input.

To synchronize multi-NAFE93352, the same SYNC signal generated by the host is connected to the SYNC pin of many AIO-AFEs. When the host issues the SYNC pulse, all the connected AIO-AFEs trigger the start conversion on the rising edge of the SYNC pulse. Enabling this functionality is required to set ADC_SYNC = 1. A SYNC pulse width should be greater or equal to two clock periods.

The SYNC input enables the host to control the start conversion of the AIO-AFE. Consequently, this provides a synchronization mechanism driven by the host also for a single AIO-AFE.

The host to be synchronized to AI-AFE data rate output (DRO) can detect the rising edge of DRDY signal. This enables the host to estimate the effective DRO and to be in SYNC with the AI-AFE on fetching the data at the right time, also in case of infinite readings.

To synchronize the AI-AFE and the host clock to the same controller clock, the user may apply an external 18.432 MHz clock to XI/EXTCLK, and CK_SRC_SEL = 1. This implementation enables coherent measurements and the possibility to synchronize the SPI data fetching with a timer.

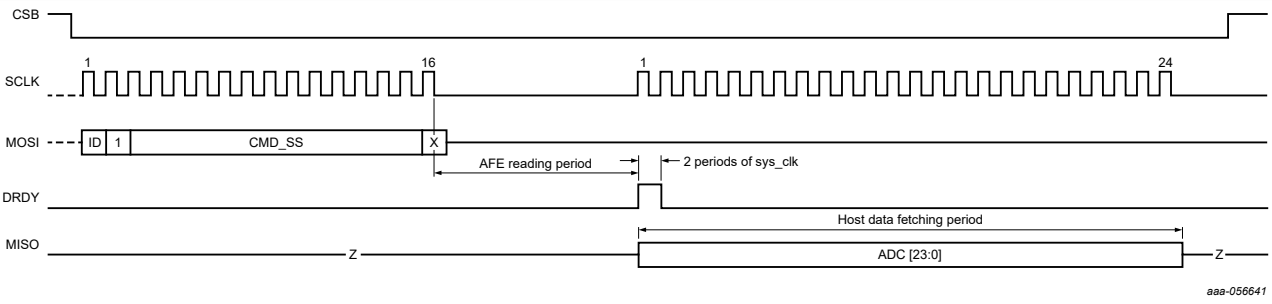


Figure 34. CMD_SS command timing with CSB low

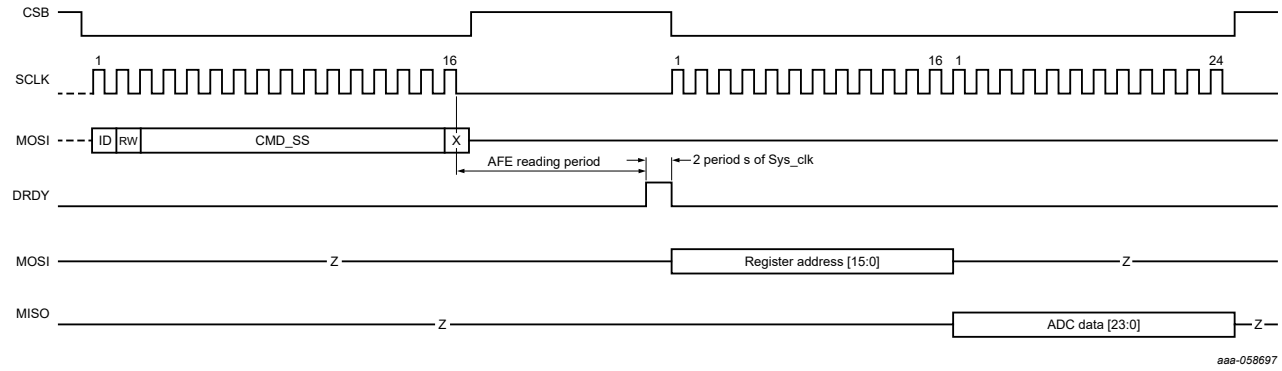


Figure 35. CMD_SS command timing with CSB high

7.18.1 SYNC signal

If bit ADC_SYNC = 1, a detection of the rising edge at the SYNC pin starts a new conversion. If there is an ongoing conversion and the rising edge of the SYNC is received, the ongoing conversion will be aborted and a new conversion will be restarted. ADC_SYNC is set to 1 in bit 5 of the SYS_CONFIG0 register.

If bit ADC_SYNC = 0, the SYNC pulse is ignored.

7.19 User register map

The user register maps are categorized into the following:

1. Input channel configuration, status, and data registers
2. Output channel configuration, status, and data registers
3. System configuration, status, and alarm registers
4. Calibration coefficients, PN, and SN

Table 19. Input channel configuration

16-bit user registers - input channel configuration					
Register address	**Bit order**	**Bit name**	**RW**	**Default value**	**Short description**
AI_CONFIG0 0x20\h	15:10	Reserved	R	0x0	Reserved
	9	PGA_PGAIN	RW	0x0	Select the positive PGA gain (V/V): 0\b = 1x, 1\b = 16x. If IN_SEL = 00001\b, PGA_PGAIN setting is used for the PGA differential gain.
	8	PGA_NGAIN	RW	0x0	Select the negative PGA gain (V/V): 0\b = 1x, 1\b = 16x. If IN_SEL = 00001\b, the PGA_NGAIN value is forced with PGA_PGAIN value.
	7:3	IN_SEL	RW	0x0	See Table 12. ***Note:*** *When select ADCP, reset GPIO_FUNCTION[11] = 0\b; When select ADCN, reset GPIO_FUNCTION[12] = 0\b.*
	2:1	AI_TCC	RW	0x0	Proprietary channel temperature coefficient compensation: 00\b = enable AI_TCC for VI mode 01\b = enable AI_TCC for CI mode wtih CSA + CISW. 1x\b = Disable ADC_TCC.
	0	Reserved	R	0x0	Reserved

Table 19. Input channel configuration*...continued*

16-bit user registers - input channel configuration					
Register address	**Bit order**	**Bit name**	**RW**	**Default value**	**Short description**
AI_CONFIG1 0x21\h	15	Reserved	R	0x0	Reserved
	14:12	ADC_CAL_COEFF	RW	0x0	Pointer to select 1 of 8 calibrated gain and offset coefficient pairs in the calibrated channel coefficient registers. See Table 39.
	11	Reserved	R	0x0	Reserved
	10:8	CH_THRS	RW	0x0	Pointer to select the channel over- and underrange threshold: 000\b corresponds to ch0, 001\b corresponds to ch1 and likewise 111/b corresponds to ch7. The threshold values are stored in registers addresses mentioned in Table 20.
	7:3	ADC_DATA_RATE	RW	0x00	ADC data rate: See Table 14.
	2:0	ADC_SINC	RW	0x0	Select ADC sinc filter. See TABLE_ADC_RATE for further details 0\h = SINC4, 1\h = SINC4+1, 2\h = SINC4+2, 3\h = SINC4+3, 4\h = SINC4+4, 5\h to 7\h = SINC4.
AI_CONFIG2 0x22\h	15:10	CH_DELAY	RW	0x0	Preset channel delay before ADC start conversion. See Table 17.
	9	ADC_NORMAL_SETTLING	RW	0x0	ADC single-cycle settling or normal settling: 0\h = single-cycle settling (SCS), 1\h = normal settling (NS).
	8	ADC_FILTER_RESET	RW	0x0	Reset ADC digital filters at the start of every ADC conversion when set. 0\h = hold digital filters data from previous conversion, 1\h = reset digital filters.
	7:6	AIO_CHOP	RW	0x0	Enable chopping mechanism for ultra-low offset (Precision mode): 0x\h = chopping disabled, 10\h = enable the ADC input path chopping with two ADC readings average (AI precision) 11\h = enable the DAC polarity chopping with two ADC readings average (AIO precision).
	5:0	Reserved	R	0x0	Reserved
AI_MULTI_CH_EN 0x23\h	15:8	MCH_EN	RW	0x00	Enable logical configurable channel for ADC conversion in Multichannel mode: 0 = disable, 1 = enable. CH7 is bit 15, CH0 is bit 8.
	7:0	Reserved	R	0x00	Reserved
AI_SYSCFG 0x24\h	15	ADCDRDY_PWDT	RW	0x0	DRDY pulse width duration (# of SYSCLK cycle): 0\h = 2, 1\h = 8.
	14	ADC_DATA_16BIT	RW	0x0	ADC data register readout: 0\h = 24 bit, 1\h = 16 bit
	13	STATUS_STICKY_AI	RW	0x0	Prepended status bits behaviour when bursting output data with STATUS_EN = 1. 0\h = live; 1\h = sticky.
	12	ADC_OFF	RW	0x0	0\h = ADC_ON, normal analog input operations. 1\h = ADC_OFF, turn-off digital filter and related ADC functional blocks in digital domain in addition to turning off. ADCBUF (adcbuf_pd_3v), ADCREF_BUF (adcref_pd_3v), and ADC core (mod_pd_3v) in analog domain.
	11	PGA_ON	RW	0x0	0\h = PGA OFF; 1\h = PGA ON. Used for RTD mode, and combo mode with two extra inputs. Should be blocked during OP.
	10	STATUS_EN	RW	0x0	Prepend 8-bit status bits to ADC data. Status bits (MSB to LSB) are: overload, underload, overrange, underrange, overtemperature, global_alarm, overvoltage, CRC error.
	9	SYNCADC_EN	RW	0x0	If (GPIO_FUNCTION[15] = 0\b) and (SYNCADC_EN = 0\b), the start conversion is triggered by the last SPI serial clock falling edge at SCK pin; If (GPIO_FUNCTION[15] = 0\b) and (SYNCADC_EN = 1\b), the start conversion is triggered by the rising edge of external pulse at SYNCADC pin; If (GPIO_FUNCTION[15] = 1\b), the PIN operates as a GPIO, and the start conversion is triggered by the last SPI serial clock falling edge at SCK pin;

Table 19. Input channel configuration*...continued*

16-bit user registers - input channel configuration					
Register address	**Bit order**	**Bit name**	**RW**	**Default value**	**Short description**
	8	ADCDRDY_PIN_EDGE	RW	0x0	Set the behavior of the DRDY pin for CMD_MS, CMD_MM, CMD_MC reading modes. 0\h = produce rising edge on every channel conversion done 1\h = produce rising edge only when the last enabled channel conversion is completed.
	7:0	Reserved	R	0x0	Reserved
AI_STATUS 0x25\h	15	SINGLE_CH_ACTIVE	R	0x00	Single-channel conversion mode indicator, which includes CH_DELAY. 0\h = idle, 1\h = active.
	14	MULTI_CH_ACTIVE	R	0x0	Multichannel conversion mode indicator, which includes CH_DELAY. 0\h = idle, 1\h = active.
	13:11	CONFIG_CH_PTR	R	0x0	The selected logical channel for R/W access to CH_CONFIG0,1,2 registers. (Result from the use of SPI CMD_Chx)
	10:8	ACT_CURR_CH	R		The current active logical channel.
	7:0	Reserved	R	0x00	Reserved
AI_STATUS_OVR 0x26\h	15:8	AI_OVR	R	0x00	Channel overrange.
	7:0	Reserved	R	0x00	Reserved
AI_STATUS_UDR 0x27\h	15:8	AI_UDR	R	0x00	Channel underrange.
	7:0	Reserved	R	0x00	Reserved

Table 20. 24-bit user registers - AI channel data

24-bit user registers - AI channel data					
AI_DATA0..7 0x30\h - 0x37\h	23:0	DATA0 … DATA7	R	0x000000	Channel output data. Each channel has a corresponding data register. DATA0[23:0] is converted data output of CH0...DATA7[23:0] is converted output of CH7.
AI_CH_OVR_THR 0x38\h - 0x3F\h	23:0	OVR_THRS0 ... OVR_THRS7	RW	0x000000	Overrange threshold setting for each logical data channel.
AI_CH_UDR_THR 0x40\h - 0x47\h	23:0	UDR_THRS0 ... UDR_THRS7	RW	0x000000	Underrange threshold setting for each logical data channel.

Table 21. 16-bit user registers - output channel configuration registers

16-bit user registers - output channel configuration registers					
AIO_CONFIG 0x20\h	15	Reserved	R	0x0	
	14	VSA ON	RW	0x0	VSA ON = 1 turn ON VSA. Exception: AO_MODE = 10\b Voltage output mode force VSA ON = 1, this bit cannot be overwritten.
	13	CSA ON	RW	0x0	CSA ON = 1 turn ON CSA. Exception: AO_mode = 11\b Current output mode force CSA ON = 1, this bit cannot be overwritten.
	12	CISW_ON	RW	0x0	CISW_ON = 1 turn ON the current input SW connected to ground. CISW is used in conjunction with external Rsense for Current input mode configuration. ***Note:*** *To avoid short-circuit, CSIW_ON should be 0\h when the PA_ON = 1, if the CISW pin is connected to AOP/AON path.*
	11:7	Reserved	R	0x0	Reserved
	6:5	AO_MODE	RW	0x0	AO_MODE Pre-configured AO modes. 00\b : Hi-Z mode, PA_ON = 0, VSA_ON = x, CSA_ON = x 10\b: Voltage output mode, PA_ON = 1, VSA_ON = 1, CSA_ON = x 11\b : Current output mode, PA_ON = 1, VSA_ON = x, CSA_ON = 1
	4	UNIPOLAR_AO_MODE	RW	0x0	Select AO mode: 0\h = Bipolar AO mode 1\h = Unipolar AO mode. See Section 7.28.2.
	3:2	Reserved	R	0x0	Reserved

Table 21. 16-bit user registers - output channel configuration registers...*continued*

16-bit user registers - output channel configuration registers					
	1:0	AO_TCC	RW	0x00	Proprietary AO temperature coefficient correction: 00\b = select AO_TCC for VO mode 01\b = select AO_TCC for CO mode 1x\b = Disable
AO_CAL_COEF 0x21\h	15	Reserved	R	0x0	Reserved
	14:12	DAC_CAL_COEF	RW	0x0	Pointer to select DAC gain and offset calibration coeffs [3-BITS]
	11:0	Reserved	R	0x0	Reserved
AIO_PROT_CFG 0x22\h	15:13	AO_CLIM_PER	RW	0x0	Select the output current limit duration at AOP, AON: 0\h = 1 ms, 1\h = 2 ms, 2\h = 5 ms, 3\h = 10 ms; 4\h = 20 ms; 5\h = 50 ms; 6\h = 20 ms; 7\h = infinite. When the timer expires, if the AO_CLIM_PER timer duration is finite, the AO mode will be changed back to VO mode. If the AO_CLIM_PER timer duration is infinite, it will remain in limited current mode.
	12:11	AO_OVRLOAD_CUR_THR	RW	0x0	Select the output overload current thresholds at AOP, AON pin: 0\h = ±25 mA; 1\h = ±20 mA; 2\h = ±10 mA; 3\h = ±5 mA.
	10:9	AO_OVRCUR_DEG	RW	0x0	Set the output overcurrent deglitch timer duration. AO_OVRCUR_DEG is re-armed whenever DAC code or AO mode change. Then, the timer will be triggered upon an AO_SHRT_L or AO_OVRLOAD_L alarm and last for a duration of 0\h = 10 µs; 1\h = 20 µs; 2\h = 50 µs; 3\h = 100 µs. When the timer expires, if AO_SHRT_L = 1 persists, the AO is put into High-Z mode and the AO_STATUS is set to 01\b if (AO_SHRT_L = 0) and (AO_OVRLOAD_L = 0) and (AO_OVRLAOD_PROT = 0), the AO is put into High-Z mode and the AO_STATUS is set to 01\b if (AO_SHRT_L = 0) and (AO_OVRLOAD_L = 1) and (AO_OVRLAOD_PROT = 1), the AO is put into limited current mode and the AO_STATUS is set to 11\h. Initial duration is controlled by A_CLIM_SD.
	8	AO_OVRLOAD_PROT	RW	0x0	Set the overload protection behavior, post AO_OVR_CUR_RT reaction timer: In the event of a programmable overload condition (set by AO_OVRLOAD_CUR_THR), if 0\h = configure AO in High-Z mode and set AO_STATUS = 3\h 1\h = configure AO in current limiter mode and set AO_STATUS = 2\h for the duration of AO_CLIM_SD.
	7:6	AO_CLIM_SD	RW	0x0	Configure the output current limiter settling delay timer to allow the current limiter to settle. 0\h = 25 µs; 1\h = 50 µs; 2\h = 100 µs; 3\h = 200 µs. When the timer expires, if (AO_SHRT_L = 1), the AO is put into High-Z mode, and AO_STATUS alarm is set to 01\b; if (AO_SHRT_L = 0) and (AO_OVRLOAD_L = 0), the AO stays in limited current mode for the duration of AO_CLIM_PER, and the AO_STATUS alarm is set to 11\b. During the AO_CLIM_PER period, if (AO_SHRT_L = 1) | (AO_OVRLOAD_L = 1) will put the AO into High-Z mode and AO_STATUS alarm is set to 01\b.
	5:4	CISW_OVRCUR_DEG	RW	0x0	CISW input overcurrent deglitch timer duration 0\h = 10 µs; 1\h = 20 µs; 2\h = 50 µs; 3\h = 100 µs; When the timer expires, if CISW_SHRT_L = 1, the CISW is turned OFF, and the CISW_STATUS bit is reset. If (CISW_SHRT_L = 0) and (CISW_OVRLOAD_L = 1), the CISW current limiter mode is activated, and the CISW_STATUS bit is set. If (CISW_SHRT_L = 0) and (CISW_OVRLOAD_L = 0), the CISW remains turned ON.
	3:2	CISW_CLIM_PER	RW	0x0	CISW input over current limit period: 0\h = 1 ms; 1\h = 2 ms; 2\h = 5 ms; 3\h = 10 ms
	1:0	CISW_CLIM_SD	RW	0x0	CISW input current limiter settling delay timer 0\h = 25 µs; 1\h = 50 µs; 2\h = 100 µs; 3\h = 200 µs; After the timer expires, if CISW_SHRT_L = 1 or CISW_OVRLOAD_L = 1 persists, the AO is set in High-Z mode, if AO_SHRT_L = 0 and AO_OVRLOAD = 0, the AO stays in current limiter mode for the duration of AO_CLIM_PER. During the CISW_CLIM_PER, if CISW_SHRT_L = 1 or CISW_OVRLOAD = 1, the CISW is opened.
AO_SLR_CTRL 0x23\h	15	SLREN	RW	0x0	Slew rate enabled = 1; default 0: disabled.
	14:12	SLR_STEP	RW	0x0	Slew rate step. See Table 8.
	11:9	SLR_CLOCK	RW	0x0	Slew rate update clock. See Table 7.
	8	Reserved	R	0x0	Reserved
	7:0	Reserved	R	0x0	Reserved

Table 21. 16-bit user registers - output channel configuration registers...*continued*

16-bit user registers - output channel configuration registers					
AWG_PER 0x24\h	15:13	STEP_AMP	RW	0x0	Programmable step size: eight step sizes, amplitude step. See Section 7.5.4.
	12:10	STEP_freq	RW	0x0	Programmable frequency update: eight freq. update. See Table 9.
	9:0	HILO_TIME	RW	0x000	Programmable high/low time in term of number of STEP_PERIOD(= 1 / STEP_FREQ). See Table 11.
AO_SYSCFG 0x25\h	15	SYNCDAC_EN	RW	0x0	If SYNCDAC_EN = 0\b, the DAC code is latched by the rising edge of CSB; If SYNCDAC_EN = 1\b, the DAC code is latched by the rising edge of External SYNCDAC pulse; ***Note:*** *The SYNCDAC pin serves as device address (ADR0) at POR. During POR, if the ADR0 is at logic level HIGH, the address is set to 1, otherwise it is set to 0. After POR the pin functions as SYNCDAC.*
	14	DAC_DATA_16BIT	RW	0x0	0\h = NUMBER OF SPI DAC DATA = 3 BYTE [24-BIT] 1\h= NUMBER OF SPI DAC DATA = 2 BYTE [16-BIT]
	13	STATUS_STICKY_AO	RW	0x0	Prepended status bits behaviour when reporting AO_OC or CI_OC status while STATUS_EN = 1. 1\h = sticky; 0\h = live.
	12	Reserved	R	0x0	Reserved
	11:10	DAC_SEL_REFBUF_ON	RW	0x0	(AO_ON[1:0]) / DAC_en / DACREFBUF_en 0 0 / 0 / 0 0 1 / 0 / 1 1 0 / 1 / 1 1 1 / 1 / 1 ***Note:*** *Need to set AO_ON = 11 along with AO_MODE = 10\b or 11\b if internal DAC is used for generating voltage and current output.*
	9:0	Reserved	R		Reserved
AIO_STATUS 0x26\h	15	CISW_STATUS	R	0x0	CISW live status. CISW status to compare against CISW_ON configuration.
	14	CSA_STATUS	R	0x0	CSA live status
	13	VSA_STATUS	R	0x0	VSA live status
	12:11	AO_STATUS	R	0x0	AO status to check against the AO configuration. The AO status can differ from the configuration since the protection circuits if triggered will put the AO into a Safe state. 00\b : High-Z mode, PA_ON = 0. 01\b : High-Z mode, set by the protection circuit. 10\b : Voltage output mode, PA_ON = 1, VSA_ON = 1. VFB mode 11\b : Current output mode, PA_ON = 1, CSA_ON = 1. CFB mode
	10:9	Reserved	R		Reserved
	8	Slew Rate_ON	R	0x0	Live detection 0\h : Slew rate control inactive 1\h : Slew rate control active
	7	AO_SHRT_L	R	0x0	Live detection 0\h : Current output short-circuit detection non-active 1\h : Current output short-circuit detection active
	6	AO_OVRLOAD_L	R	0x0	Live detection 0\h : Current output overload detection ON = 0 1\h : Current output overload detection ON = 1
	5	CISW_SHRT_L	R	0x0	Live detection 0\h : Current input short-circuit detection ON = 0 1\h : Current input short-circuit detection ON = 1
	4	CISW_OVRLOAD_L	R	0x0	Live detection 0\h : Current input overload detection ON = 0 1\h : Current input overload detection ON = 1
	3	CISW_SHRT_S	W1C	0x0	Sticky status bit. Write 1/Issue CMD_CISW_ABORT/CMS_CISW_ABORT_HIZ to clear 0\h : Current input short-circuit detection ON = 0

Table 21. 16-bit user registers - output channel configuration registers...*continued*

16-bit user registers - output channel configuration registers					
					1\h : Current input short-circuit detection ON = 1
	2	CISW_OVRLOAD_S	W1C	0x0	Sticky status bit. Write 1/Issue CMD_CISW_ABORT/CMS_CISW_ABORT_HIZ to clear 0\h : Current input overload detection ON = 0 1\h : Current input overload detection ON = 1
	1	AO_SHRT_S	W1C	0x0	Sticky status bit. Write 1/Issue CMD_AO_ABORT/CMS_AO_ABORT_HIZ to clear 0\h : Current output short-circuit detection ON = 0 1\h : Current output short-circuit detection ON = 0
	0	AO_OVRLOAD_S	W1C	0x0	Sticky status bit. Write 1/Issue CMD_AO_ABORT/CMS_AO_ABORT_HIZ to clear 0\h : Current output overload detection ON = 0 1\h : Current output overload detection ON = 1

Table 22. 24-bit user registers - AO channel data

24-bit user registers - AO channel data					
AO_DATA 0x28\h	23:0	DAC_DATA	RW	0x000000	[23:6] 18-bit DAC code: Analog_trim0[1:0] = 0; Range : -131072 to + 131071 [23:8] 16-bit DAC code: Analog_trim0[1:0] = 1; Range : -32768 to + 32767 [23:10] 14-bit DAC code: Analog_trim0[1:0] = 2; Range : -8192 to + 8191 [23:12] 12-bit DAC code: Analog_trim0[1:0] = 3; Range : -2048 to +2047
AO_OC_POS_LIMIT 0x29\h	23:0	OUT_OC_POS_LIMIT	RW	0x000000	Output overcurrent limit – positive [23:6] 18-bit - CSA
AO_OC_NEG_LIMIT 0x2A\h	23:0	OUT_OC_NEG_LIMIT	RW	0x000000	Output overcurrent limit – negative [23:6] 18-bit - CSA
AWG_AMP_MAX 0x2B \h	23:06	AMP_WMAX	RW	0x000000	[23:6] 18-bit MAX code range : -131072 to 131071. See Section 7.5.4.
	5:0	Reserved	R	0x0	Unused
AWG_AMP_MIN 0x2C\h	23:06	AMP_WMIN	RW	0x000000	[23:6] 18-bit MAX Code range : -131072 to 131071. See Section 7.5.4.
	5:0	Reserved	R	0x0	Unused

Table 23. 16-bit user registers - common system configuration and status

16-bit user registers - common system configuration and status					
CRC_CONF_REGS 0x20\h	15:0	CRC_CONF_REGS	R	0x0000	Calculated CRC result of all the current user's configuration registers (RW) except the status and data output register (R).
CRC_COEF_REGS 0x21\h	15:0	CRC_COEF_REGS	R	0x0000	Calculated CRC result of all the current user's 24-bit coefficient registers (RW).
CRC_TRIM_REGS 0x22\h	15:0	CRC_TRIM_REGS	R	0x0000	Calculated CRC output result of all the current internal trim registers (R internal)
CRC_TRIM_REF 0x3F\h	15:0	CRC_TRIM_REF	R	0x0	Stored reference result of precalculated CRC at production of internal trim registers, to be used for comparison against CRC_TRIM_REGS. (R internal)
GPI_DATA 0x23\h	15:11	GPI_DATA	R	0x00	GPI data detected: 0 = Logic 0 (DGND), 1 = Logic 1 (DVDD). GPIO4 is bit15, GPIO0 is bit11.
	10:0	Reserved	R	0x00	Reserved
GPO_ENABLE 0x24\h	15:11	GPO_ENABLE	RW	0x00	GPO driving enable:

Table 23. 16-bit user registers - common system configuration and status*...continued*

16-bit user registers - common system configuration and status					
					0 = disabled driving, 1 = enabled driving. GPIO4 is bit15, GPIO0 is bit11.
	10:0	Reserved	R	0x00	Reserved
GPIO_FUNCTION 0x25\h	15:11	PIN_FUNC	RW	0x00	0 = Normal pin function, 1= GPIO function. GPIO4 is mapped to bit15, GPIO0 is mapped to bit11.
	10:0	Reserved	R	0x0000	Reserved
GPI_ENABLE 0x26\h	15:11	GPI_ENABLE	RW	0x00	GPI read enable: 0 = disabled read, 1 = enabled read. GPIO4 is bit15, GPIO0 is bit11.
	10:0	Reserved	R	0X00	Reserved
GPI_EDGE_POS 0x27\h	15:11	GPI_EDGE_POS	R	0x00	GPI positive edge(s) data: 0\h = none, 1\h = positive edge detected. Cleared after readback or CMD_CLEAR_ALRM.
	10:0	Reserved	R	0x0000	Reserved
GPI_EDGE_NEG 0x28\h	15:11	GPI_EDGE_NEG	R	0x00	GPI negative edge(s) data: 0\h = none, 1\h = negative edge detected. Cleared after readback or CMD_CLEAR_ALRM.
	10:0	Reserved	R	0x0000	Reserved
GPO_DATA 0x29\h	15:11	GPO_DATA	RW	0x00	Set GPO output data: 0\h = output logic 0, 1\h = output logic 1. GPIO4 is bit15, GPIO0 is bit11.
	10:0	Reserved	R	0x0000	Reserved
SYS_CONFIG 0x2A\h	15:9	Reserved	R	0x0	Reserved
	8	REF_SEL	RW	0x0	Select internal or external 2.5 V voltage references for ADCREFBUF and DACREFBUF: 0\h = selects internal 2.5 V (REF_INT). 1\h = selects external 2.5 V (REF_EXT). ***Note:*** *Internal reference is always powered on.*
	7	GLOBAL_ALRM_STICKY	RW	0x0	Global alarm interrupt behavior is: 0\h= non-sticky, read to clear and it is live status. 1\h= sticky, write 1 to clear a specific bit.
	6	SPI_DOUT_DRIVE	RW	0x0	Increase DOUT output drive if high capacitance loading.
	5	INTB_DRIVER_TYPE	RW	0x0	INTB pin driver type: 0 = 100 kΩ pullup with open drain, 1 = CMOS push-pull.
	4	CRC_EN	RW	0x0	Enable CRC: 0\h = disable, 1\h = enable.
	3:0	Reserved	R	0x0	Reserved
SYS_STATUS 0x2B\h	15:14	Reserved	R	0x0	Reserved
	13	CHIP_READY	R	0x0	Chip status indicator. Upon power up, INTB pin will go LOW (active low) to indicate the chip is ready. The user must read this register to clear the INTB pin. This bit will stay HIGH when the chip is operational. 0\h = Chip is not yet ready, 1\h = Chip is ready.
	12	Reserved	R	0x0	Reserved
	11:10	CK_SRC_SEL_STAT	R	0x0	Status indicating the system clock in use: 0x\b : Internal clock in use.

Table 23. 16-bit user registers - common system configuration and status*...continued*

16-bit user registers - common system configuration and status					
					1x\b : External clock in use.
	9	CRC_ERROR_S	W1C	0x0	CRC error encountered on MOSI line before the last transmission. ***Note:*** *Write 1 to clear.*
	8	CRC_ERROR_L	R	0x0	CRC error encountered on MOSI line on last transmission.
	7:0	Reserved	R	0x0	Reserved
CK_SRC_SEL_CONFIG 0x30\h	15:12	Reserved	R	0x0	Reserved

	11:**10**	CK_SRC_SEL	RW	0x0	If (GPIO_FUNCTION[13] = 0\b) and (CK_SRC_SEL = 0x \b), select internal clock;
					If (GPIO_FUNCTION[13] = 0\b) and (CK_SRC_SEL = 1x \b), select the applied external clock at OSCIN/GPIO2;
					Note: *Switch time ~ 5 µs.*
					If (GPIO_FUNCTION[13] = 1\b), the OSCIN/GPIO2 pin operates as GPIO, and internal clock is selected;
					Note: *Only during POR, an internal auto-selection logic selects the external clock source at OSCIN/GPIO2 pin if a clock signal is detected.*
					Before CHIP_READY is set to logic 1, the internal or external clock has been already selected and the auto-selection logic is disabled.
					Note: *~ 2 ms*

	9:0	Reserved	R	0x0	Reserved

Table 24. 16-bit user registers - global alarm configuration and status

16-bit user registers - global alarm configuration and status					
GLOBAL ALARM ENABLE 0x2C\h	15	OVER_TEMP_ALRM	RW	0x0	Overtemperature warning at 145 ºC.
	14	HVDD_ALRM	RW	0x0	Enable alarm for HVDD supply detect below preset threshold.
	13	HVSS_ALRM	RW	0x0	Enable alarm for HVSS supply detect below preset threshold.
	12	DVDD_ALRM	RW	0x0	Enable alarm for DVDD supply detect below preset threshold.
	11	CRC_ALRM	RW	0x0	Enable alarm for CRC error detection on MOSI line.
	10	GPI_POS_ALRM	RW	0x0	Enable alarm for rising edge detected at any of GPI pins.
	9	GPI_NEG_ALRM	RW	0x0	Enable alarm for falling edge detected at any of GPI pins.
	8	CONFIG_ERROR_ALRM	RW	0x0	Enable alarm for register configuration error.
	7	AI_OVRRNG_ALRM	RW	0x0	Enable alarm for one or more data channel is overrange.
	6	AI_UNDRNG_ALRM	RW	0x0	Enable alarm for one or more data channel is underrange.
	5	AI_OVRLOAD_ALRM	RW	0x0	Enable alarm for one or more data channels is overloaded or underloaded.
	4	EXTCLK_FREQ_ALRM	RW	0x0	Enable alarm when EXTCLK frequency varies with internal CLK by XX.
	3	AO_OC_ALRM	RW	0x0	Enable alarm for analog output overcurrent.
	2	CI_OC_ALRM	RW	0x0	Enable alarm for analog input overcurrent.
	1	AO_SHRT_ALRM	RW	0x0	Enable short alarm.
	0	TEMP_ALRM	RW	0x0	Enable programmable temperature alarm. The threshold is set in THRS_ TEMP register bits.
GLOBAL ALARM INT 0x2D\h	15	OVER_TEMP_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	14	HVDD_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	13	HVSS_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	12	ADVDD_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	11	CRC_ERR_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	10	GPI_POS_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	9	GPI_NEG_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.

Table 24. 16-bit user registers - global alarm configuration and status*...continued*

16-bit user registers - global alarm configuration and status					
	8	CONFIG_ERROR_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	7	AI_OVRRNG_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	6	AI_UNDRNG_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	5	AI_OVRLOAD_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	4	EXTCLK_FREQ_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	3	AO_OC_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	2	CI_OC_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	1	AO_SHRT_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
	0	TEMP_INT	RW	0x0	Bit clear behavior controlled by GLOBAL_ALRM_STICKY.
DIE_TEMP 0x2E \h	15:0	DIE_TEMP	R	0x00	16-bit die temperature readout in 2's compliment. Temperature = DIE_TEMP value/64 ºC
TEMP_THRS 0x2F\h	15:0	TEMP_THRS	RW	0x00	Temperature threshold in 2's compliment for setting custom temperature warning alarm.

Table 25. 24-bit calibration coefficient registers - common

24-bit calibration coefficient registers - common					
GAIN_COEF0...7 0x50\h-0x57\h	23:0	GCC	RW	0x400000	Calibrated gain coefficients. The user may alter or update the values to fit their application. For each of the logical channel setup, these GAIN_COEF registers are indexed by addressable pointer set by register bits CH_CAL_GAIN_OFFSET[2:0]. Initially after CHIP_READY, the content of these registers are populated with factory-calibrated coefficients. See Table 33 if applicable.
OFFSET_COEF0...7 0x58\h-0x5F\h	23:0	OCC	RW	0x000000	Calibrated offset coefficients. The user may alter or update the values to fit their application. For each of the logical channel setup, these OFFSET_COEFF registers are indexed by addressable pointer set by register bits CH_CAL_GAIN_OFFSET[2:0]. Initially after CHIP_READY, the content of these registers are populated with factory-calibrated coefficients. See Table 33 if applicable.
EXTRA_CAL_COEF0...7 0x60\h -0x67\h	23:0	EXTCC	RW	0x00000000	Extra register for temporary storing coefficients, for example, it can be used as self-calibrated ADC values and internal VREF.

Table 26. 16-bit user registers - part number

16-bit user registers - part number					
PN2 0x40\h	15:0	PN2	R	0x00	Part number (MSB). Example, 9335 for NAFE93352B40BS part number
PN1 0x41\h	15:0	PN1	R	0x00	Part number (MidLSB). Example, 2B40 for NAFE93352B40BS
PN0_REV 0x42\h	15:8	PN0	R	0x00	Part number (LSB). Example, 00 for NAFE93352B40BS
	7:0	REVISION_ID	R	0xB0	Revision

Table 27. 24-bit user registers - serial number

24-bit user registers - serial number					
REGISTER(24-bit)	BIT ORDER	BIT NAME	RW	RESET	SHORT DESCRIPTION
SERIAL1 0x43\h	23:0	SN1	R	0x	[23:0] Unique serial number (MSB)
SERIAL0 0x44\h	23:0	SN0	R	0x	[23:0] Unique serial number (LSB)

7.20 SPI and controls

7.20.1 SPI signal pins

The SPI-compatible serial interface is used to read the conversion data and internal register content, and to configure the device and to control the DAC and ADC. The serial interface consists of four signals: CSB, SCLK, MOSI, and MISO. One external pin is used as a SPI address, such that the host can address two devices without using a separate CSB pin. In addition, the DRDY and SYNC signals allow handshaking and data synchronization between the host and the device. The conversion data are provided with an optional CRC code for improved data integrity. The DAC word can be written with and without an 8-bit CRC appended at the end of data.

CSB (active low) is an input pin that enables the communication between the host and the chip. CSB must remain low entire data transaction. When CSB is set to high, the serial interface is reset, SCLK input and command inputs are ignored.

SPI_ADDR is an additional SPI address pin, in addition to CSB.

SCLK is a serial interface clock that can operate up to 32 MHz. It is a noise-filtered, Schmitt-triggered input used to clock data in/out of the chip. Serial input data is latched in the falling edge of SCLK and serial data outputs from the chip are updated on the rising edge of SCLK.

MOSI is the serial data input to the chip. MOSI is used to input commands and register data to the chip.

MISO is the serial data output from the chip. MISO is contained in the internal registers data, ADC results, status byte, and/or 8-bit CRC if CRC_EN and/or STATUS_EN set to 1, respectively. When CSB is high, MISO is in high-impedance, 3-state mode. MISO is updated on the rising edge of the SCLK.

DRDY (active low to high) is an output pin that displays the conversion status. DRDY is driven from low-to-high when the conversion result is ready for reading. It stays high for a finite duration.

SYNC is an external pin used to synchronize the data conversion to external events. Start any conversion mode can be either (not both) used SPI command or asserting low-to-high transition on the SYNC pin given that the ADC_SYNC bit in the SYS_CONFIG0 register is set to 1. Upon the rising edge of the SYNC. The details of how to use this signal is described in a later section.

INTB (active low) is an output pin that notifies there is a global alarm interrupt has occurred.

7.20.2 SPI communication protocols

The SPI user communication protocol is described in the following section. The SPI host must always start with DEV_AD bit either 0 or 1 to match with the device ADDR0’s pin to initiate the communication with that device. The following bits are: RW bit (read or write transaction), SYS_L bit, 2-bit Dev_IO, 2-bit Ch, 8 RA bits (addressable up to 8192 location) and D is data from host to device or device to host depending on write or read operation, respectively. SYS_L and Dev_IO are used to access different sub-system registers of the chip, for example, ADC, DAC, and common.

Bit	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22		1	0
	DEV_AD	RW_L	SYS_L	DEV_IO1	DEV_IO0	CH1	CH0	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	X	D23	D22		D1	D0
	RA12	RA11	RA10	RA9	RA8																

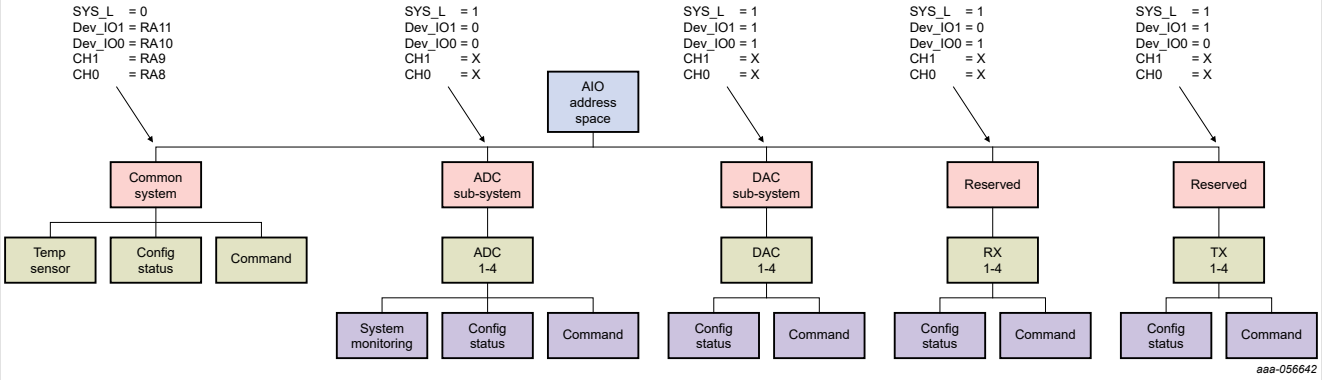


Figure 36. SPI framework

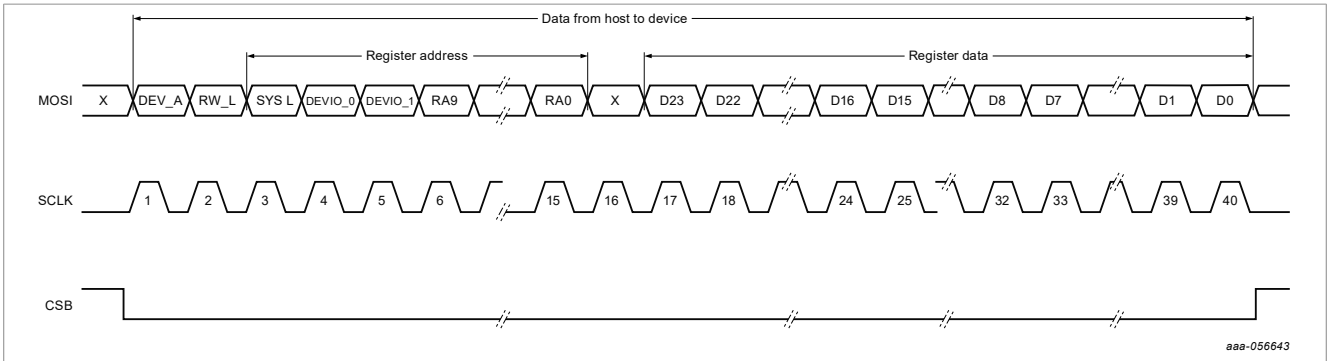


Figure 37. SPI register write timing diagram

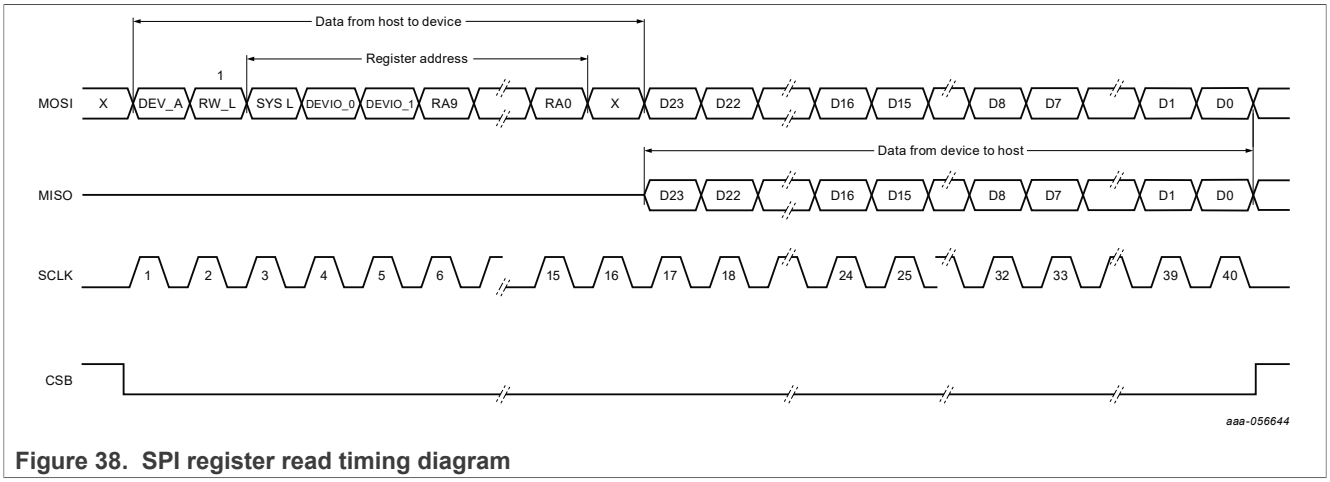


Figure 38. SPI register read timing diagram

7.20.3 SPI command

SPI commands are dedicated SPI address with predefined functions for reducing SPI transactions on frequent data accesses and controls.

CMD_RELOAD: only reloads OTP contents to shadow registers. OTP contents consist of NAFE93352 trims parameters and offset and gain calibration coefficients. This command does not reset user registers.

CMD_CLEAR_REG: only clear user-accessible registers except the clock source select,

CK_SRC_SEL[1:0] does not get clear even if they are part of user's registers and user can change this register after PORB while any conversion is in active. For instance, CK_SRC_SEL was held other value than 0 before the command was issued, it would stay the same after this command was issued.

Table 28. Common system commands

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Common system commands	*Mnemonic*
DEV_AD	RW_L	**SYS_L = 0**	Dev_IO1	DEV_IO0	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	X	Command description	
X	0	0	0	0	0	0	0	0	0	1	0	0	1	0	X	**CMD_CLEAR_ALRM**: Clear global alarm	***CMD_ CLEAR_ ALARM***
X	0	0	0	0	0	0	0	0	0	1	0	1	0	0	X	**CMD_RESET:** (HW reset, same as RSTB pulled low)	***CMD_RESET***
X	0	0	0	0	0	0	0	0	0	1	0	1	0	1	X	**CMD_CLEAR_REG**: (SW clears all user registers to default values except SYS_ CONFIG0 register).	***CMD_ CLEAR_REG***
X	0	0	0	0	0	0	0	0	0	1	0	1	1	0	X	***CMD_RELOAD:*** *Reload stored contents from on-chip non-volatile memory.*	***CMD_ RELOAD***
X	0	0	0	0	0	0	0	0	0	1	0	1	1	1	X	*Reserved*	***Reserved***
X	1	0	0	0	0	0	0	0	0	0	0	1	1	0	X	***CMD_CALC_CRC_CONFG:*** *Calculate CRC sum for all 16-bit user configuration registers and save result to CONF_ REGS_CRC register.*	***CMD_CALC_ CRC_CONFG***
X	1	0	0	0	0	0	0	0	0	0	0	1	1	1	X	***CMD_CALC_CRC_COEF:*** *Calculate CRC sum for all 24-bit CAL coefficient and threshold registers and save result to COEF_REGS_CRC register.*	***CMD_CALC_ CRC_COEF***
X	1	0	0	0	0	0	0	0	0	0	1	0	0	0	X	***CMD_CALC_CRC_FAC:*** *Calculate all factory OTP trim registers and save result to TRIM_REGS_CRC register (save factory sum in memory somewhere: OTP's PA : TDB).*	***CMD_CALC_ CRC_FAC***
X	X	0	0	0	0	0	0	0	0	X	X	X	X	X	X	***TBA***	
X	1	0	0x200-0xFFF												X	**Common system's register read via SPI**	
X	0	0	0x200-0xFFF												X	**Common system's register write via SPI**	

Table 29. ADC system command

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	**ADC0-3 (CH1 = 0, CH0 = 0) sub-system's commands : Dev_IO1 = 0, Dev_IO0 = 0 => ADC**	*Mnemonic*
DEV_AD	RW_L	**SYS_L=1**	**Dev_IO1**	**Dev_IO0**	**CH1**	**CH0**	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	X	Command description	
X	0	1	0	0	0	0	0	0	0	0	0	0	0	0	X	**CMD_CH0**: To select logical channel CH0	***CMD_CH0***
X	0	1	0	0	0	0	0	0	0	0	0	0	0	1	X	**CMD_CH1:** To select logical channel CH1	***CMD_CH1***
X	0	1	0	0	0	0	0	0	0	0	0	0	1	0	X	**CMD_CH2:** To select logical channel CH2	***CMD_CH2***
X	0	1	0	0	0	0	0	0	0	0	0	0	1	1	X	**CMD_CH3:** To select logical channel CH3	***CMD_CH3***
X	0	1	0	0	0	0	0	0	0	0	0	1	0	0	X	**CMD_CH4:** To select logical channel CH4	***CMD_CH4***
X	0	1	0	0	0	0	0	0	0	0	0	1	0	1	X	**CMD_CH5: To select logical channel CH5**	***CMD_CH5***
X	0	1	0	0	0	0	0	0	0	0	0	1	1	0	X	**CMD_CH6: To select logical channel CH6**	***CMD_CH6***
X	0	1	0	0	0	0	0	0	0	0	0	1	1	1	X	**CMD_CH7: To select logical channel CH7**	***CMD_CH7***
X	0	1	0	0	0	0	0	0	0	1	0	0	0	0	x	**CMD_ADC_ABORT:** Abort the current conversion immediately	***CMD_ADC_ ABORT***

Table 29. ADC system command*...continued*

X	0	1	0	0	0	0	0	0	0	1	0	0	1	0	x	**CMD_END:** Stop ADC at the end of the current conversion	***CMD_ADC_END***
X	0	1	0	0	0	0	0	0	0	1	0	0	1	1	X	**CMD_CLEAR_DATA:** Clear all ADC0 channel data	***CMD_CLEAR_DATA***
X	1	1	0	0	0	0	0	0	0	0	0	0	0	0	X	**CMD_SS:**One-shot conversion on the selected channel. When bit ADC_SYNC=1, the start conversion is triggered by SYNC pulse. If bit ADC_SYNC=0, the last edge of this SPI command is used to trigger the conversion start. (SS: Single-channel Single-reading)	***CMD_SS***
X	1	1	0	0	0	0	0	0	0	0	0	0	0	1	X	**CMD_SC:** Continuous conversion on the selected channel until CMD_ABORT or CMD_END. If bit ADC_SYNC = 1, SYNC pulse is used to start the conversion. Similar to all other conversion modes, the last edge of this SPI command is used to trigger the conversion start when bit ADC_SYNC = 0. (SC: Single-channel continuous-reading)	***CMD_SC***
X	1	1	0	0	0	0	0	0	0	0	0	0	1	0	X	**CMD_MM:**Multichannel conversions in Autonomous mode. The sequencer will start conversion by sequencing on the enabled channel set forth in MCH_EN[7:0] register, from CH0 to CH7. When bit ADC_SYNC = 1, SYNC pulse is used to start the first conversion only, the subsequent channel increment and conversion is autonomous. If SYNC pulse is issued before completion of the current conversion, ADC will abort the conversion immediately and move to the first enabled channel. Same behavior is expected with CMD_ABORT in this mode. (MM: multichannel multireading)	***CMD_MM***
X	1	1	0	0	0	0	0	0	0	0	0	0	1	1	X	**CMD_MC:** Similar to CMD_SSEQ with infinite looping until CMD_ABORT or CMD_END is issued. (MC: Multichannel continuous reading)	***CMD_MC***
X	1	1	0	0	0	0	0	0	0	0	0	1	0	0	X	**CMD_MS:** Multichannel conversions in Host-driven mode. If bit ADC_SYNC = 1, each conversion is started by the rising edge of SYNC pulse. If bit ADC_SYNC = 0, issue this SPI command repeatedly to trigger conversion start for each enabled channels. If bit ADC_SYNC = 1, each SYNC pulse edge is used as trigger for conversion start on the next enabled channel. Upon completion of each ADC conversion, the pointer is auto-incremented to the next enabled channel and awaits for the arrival of SYNC edge. The ADC will loop back to 1st enabled channel when the last enabled channel was completed. Issue CMD_END or CMD_ABORT will exit this mode. If SYNC pulse is issued before completion of the conversion on the current channel, ADC will abort the conversion immediately and stay at the current channel (this is contrary to channel pointer behavior in MM and	***CMD_MS***

Table 29. ADC system command*...continued*

																MC modes). (MS: Multichannel single-reading)	
X	1	1	0	0	0	0	0	0	0	0	0	1	0	1	X	**CMD_BURST_DATA:** Burst read the enabled data channels from CH_DATA from CH0 to CH7 sequentially (determined by MCH_EN[7:0] bits)	***CMD_BURST_DATA***
X	X	1	0	0	X	X	0	0	0			[1]				**TBA**	
X	1	1	0	0	X	X	0x20-0xFF									ADC0 sub-system's register read via SPI	
X	0	1	0	0	X	X	0x20-0xFF									ADC0 sub-system's register write via SPI	

[1] Command future expansion

Table 30. DAC system command

15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**DAC0-3 (CH1 = X, CH0 = X) sub-system's commands : Dev_IO1 = 1, Dev_IO0 = 1 => DAC**	***Mnemonic***
DEV_AD	RW_L	**SYS_L = 1**	**Dev_IO1**	**Dev_IO0**	**CH1**	**CH0**	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	X	Command description	
X	0	1	1	1	0	0	0	0	0	0	0	0	0	0	X	**CMD_WGEN_STOP:** Stop the auto_waveform generator	***CMD_WGEN_STOP***
X	0	1	1	1	0	0	0	0	0	0	0	0	0	1	X	**CMD_WGEN_START:** Command to start auto-generation DAC waveform output	***CMD_WGEN***
x	0	1	1	1	0	0	0	0	0	0	0	0	1	0	X	**CMD_CLEAR_DAC0 :** Command to set DAC output to mid-scale level similar at POR. It also resets the slew rate state machine when it is progress. While wave gen is in progress, this command will be ignored. Midscale level at user's 18-bit = 'h00000;	***CMD_CLR_DAC0***
x	0	1	1	1	0	0	0	0	0	0	0	0	1	1	X	**CMD_AO_ABORT:** Abort the running AO overcurrent protection FSM after a detected overcurrent in VO or CO mode. CMD_AO_ABORT: Exit the running AO overcurrent protection FSM after clearing the sticky status for AO overcurrent, AO_SHRT_S and AO_OVRLOAD_S and overwriting AO mode field of AO_config with the previous mode (VO or CO mode) and updating DAC value with user register DAC value. Then go to Idle state. CMD_AO_ABORT is ignored if the AO overcurrent protection FSM is in an Idle state.	***CMD_AO_ABORT***
x	0	1	1	1	0	0	0	0	0	0	0	1	0	0	X	**CMD_AO_ABORT_HIZ:** Abort the running AO overcurrent protection FSM after a detected overcurrent in VO or CO mode. CMD_AO_ABORT_HIZ Exit the AO overcurrent FSM after clearing the sticky status for AO overcurrent, AO_SHRT_S and AO_OVRLOAD_S and resetting user programmed AO_MODE to HIZ (overwrite the AO_MODE field of SPI register to HiZ). Then go to Idle state. CMD_AO_ABORT_HIZ is ignored if the AO overcurrent protection FSM is in an idle state.	***CMD_AO_ABORT_HIZ***
x	0	1	1	1	0	0	0	0	0	0	0	1	0	1	X	**CMD_CISW_ABORT:**Abort the running CISW input overcurrent protection FSM after a detected overcurrent on CISW input. CMD_CISW_ABORT Exit the CISW overcurrent protection	***CMD_CISW_ABORT***

Table 30. DAC system command*...continued*

																FSM after clearing the overcurrent sticky status bits CISW_SHRT_S and CISW_OVRLOAD_S, disengaging CISW current limiter and overwriting CISW_ON bit register to 1. Then go to Idle state. CMD_CISW_ABORT is ignored if the CISW overcurrent protection FSM is in an Idle state.	
x	0	1	1	1	0	0	0	0	0	0	0	1	1	0	X	**CMD_CISW_ABORT_HIZ:**Abort the CISW input overcurrent protection FSM after triggered by an overcurrent detection on CISW input. CMD_CISW_ABORT_HIZ exit the CISW overcurrent protection FSM after clearing the overcurrent sticky status CISW_SHRT_S and CISW_OVRLOAD_S,overwriting, and overwriting the user-programmed CISW switch control (AIO_CONFIG.CISW_ON) configuration to open the switch. Then go to Idle state. CMD_CISW_ABORT_HIZ is ignored if the CISW overcurrent protection FSM is in an idle state.	***CMD_CISW_ABORT_HIZ***
X	0	1	1	1	0	0	0	0	0		Command future expansion						
x	1	1	1	1	0	0	0x20-0xFF									DAC0 sub-system's register read via SPI	
x	0	1	1	1	0	0	0x20-0xFF									DAC0 sub-system's register write via SPI	

7.20.4 SPI byte-wise write command

The second bit after the first SPI bit frame RW_L is 0, which indicates this is a write transaction. A SPI write command is used to configure the internal registers of the chip. The register values are updated every eighth clock cycle with a byte of data starting from the MSB. A minimum of eight SCLKs are needed to write the first byte of data in a multibyte register. For example, if the user needs to update the first MSB-byte (bit 23:16) of the register that has 24-bit data width and bits 15 to 0 retain the old value of the register, then eight SCLKs are needed. The example below shows the host partial write value 0xA5 to bit 23 to bit 16 of register 0x0010.

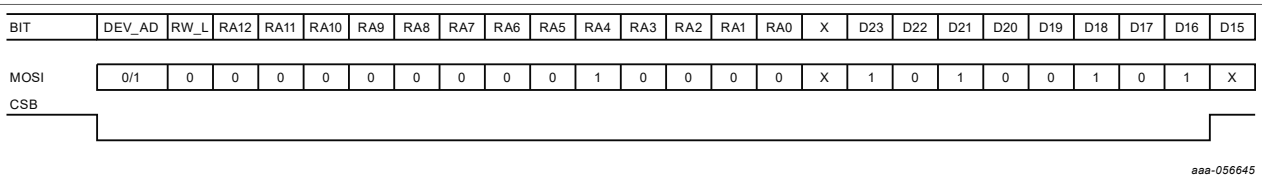


Figure 39. SPI register byte-wise write timing diagram

7.20.5 Register write with CRC enabled

Figure 40 and Figure 41 show host writes 16-bit and 24-bit internal register respectively. There are two CRC bytes sent from host named CRC-2. The first CRC byte is calculated by the host from the first 16-bit data word which includes device ID bit, RWL bit, RA bits, and don't care bit (0). The second CRC byte is calculated from the 16-bit WDATA[15:0] or WDATA[23:0] if the host writes to the 16-bit register or 24-bit register, respectively. There is always an extra empty byte (eight extra SCLKs) required host send after the second CRC byte. The device needs extra clocks to check/verify with the on-chip CRC logic if the data sent by the host is not corrupted. After the CRC byte is received and a match is found with the device-calculated CRC, then the register update will take place. The controller can decide to drive an extra seven more clock cycles to receive

the calculated CRC data from the device or it can terminate the SPI frame by deassert the CSB to high without affecting the register being updated.

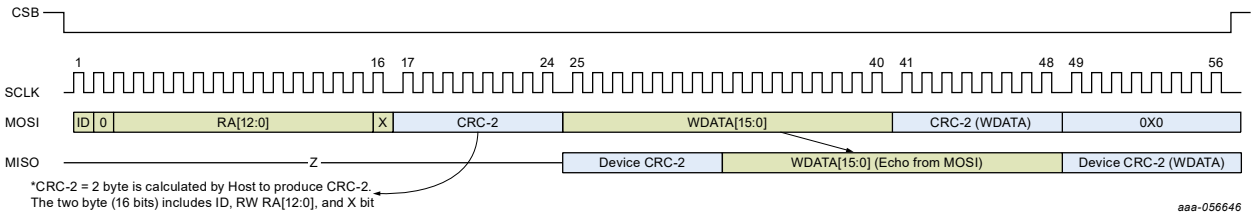


Figure 40. Host writes to register 16-bit with CRC enabled

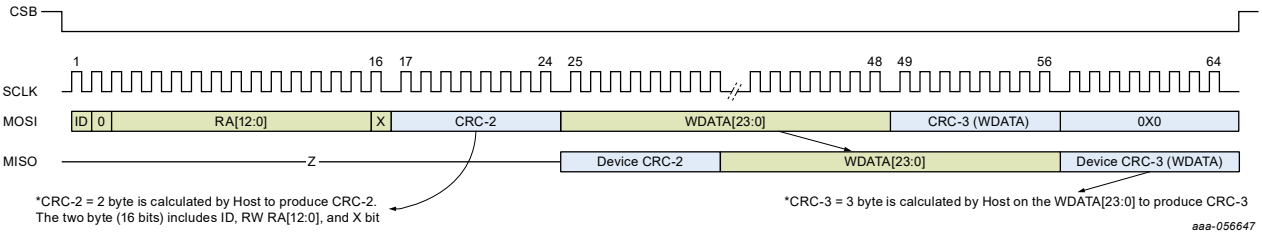


Figure 41. Host writes to register 24-bit with CRC enabled

7.20.6 DAC conversion timing

The DAC needs min 18 system clocks of wait time between last SCLK edge and CSB/SYNDAC (depending on which one is being used) going high at the end of the SPI frame. This time is specified as TDAC_wait in EC table and violation of it will lead to erroneous output (voltage or current) at pin AO.

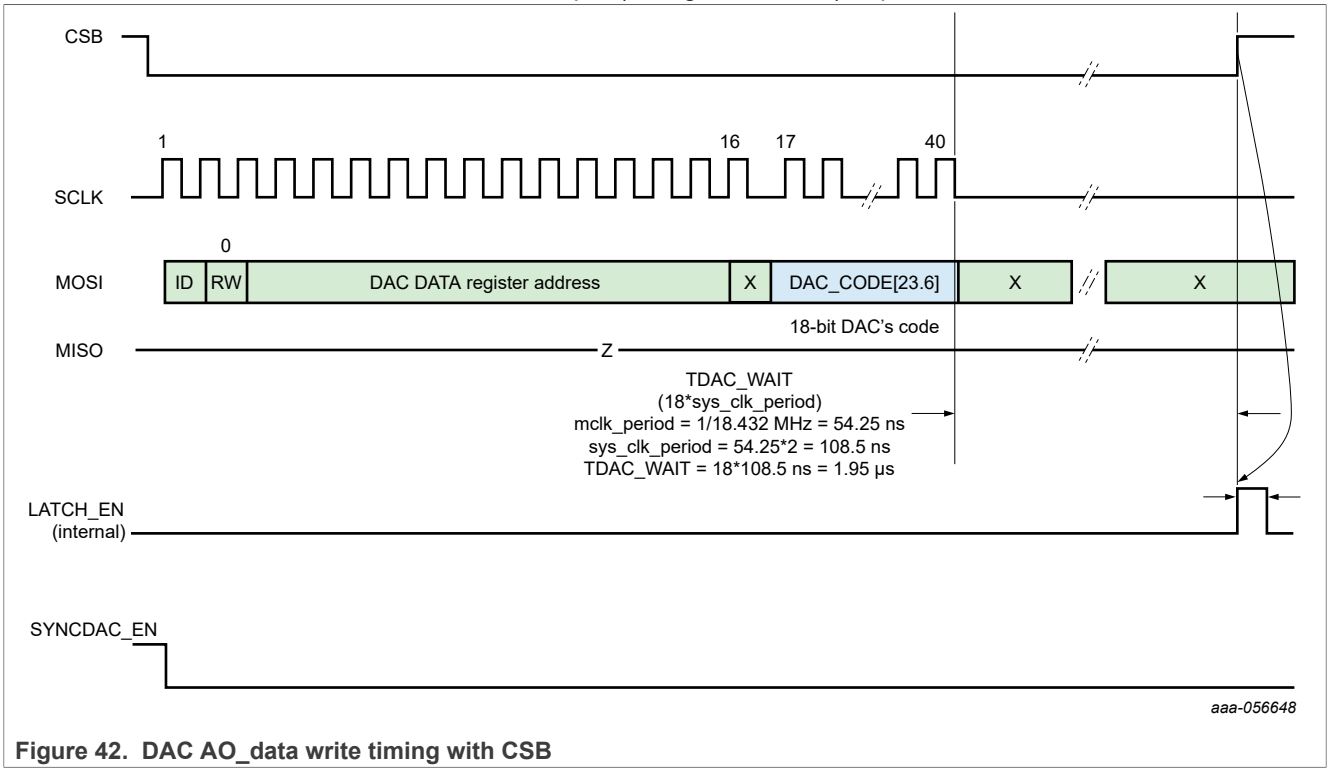


Figure 42. DAC AO_data write timing with CSB

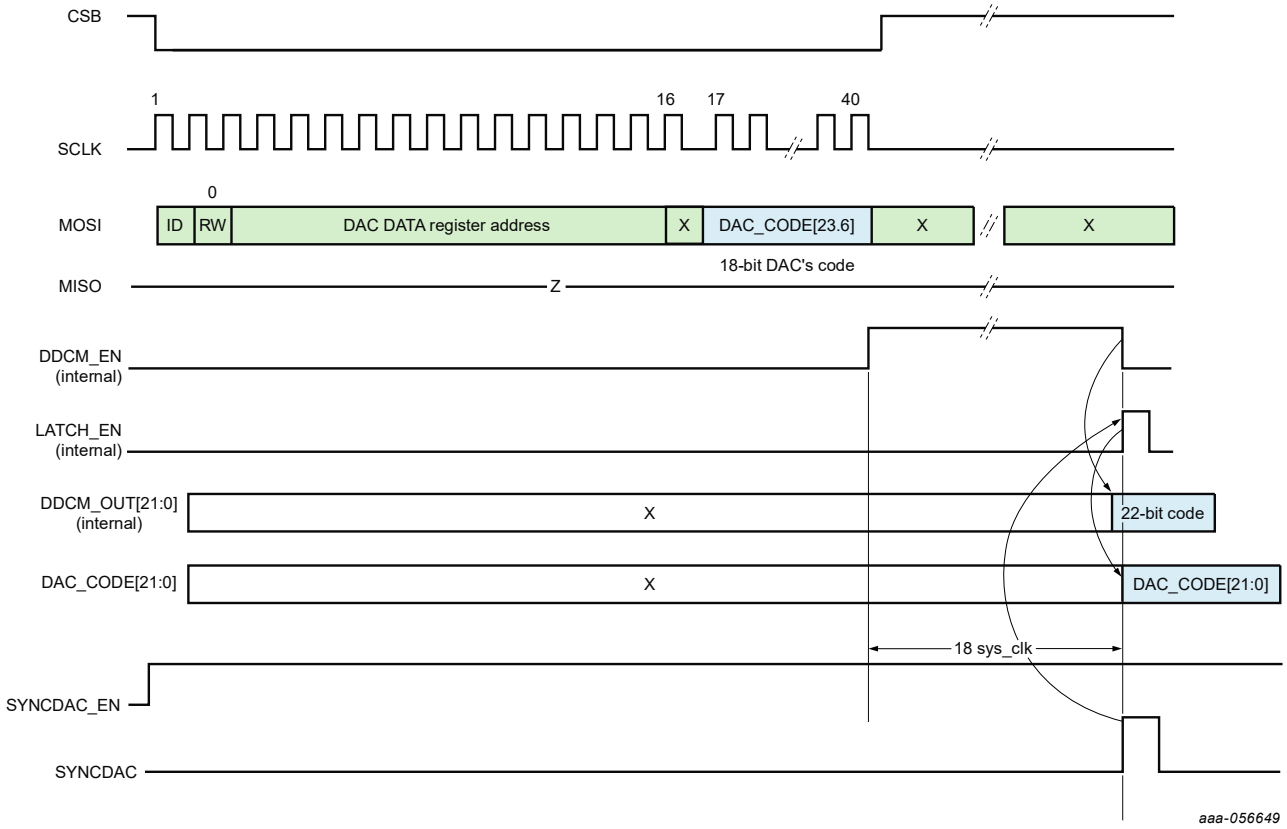


Figure 43. DAC AO_data write timing with SYNCDAC

7.20.7 CRC

CRC-8 generator

The NAFE93352 provides assurance of the integrity of the data communication, it has an option to have 8-bit CRC data appended after the data transfers or revives. The CRC_EN is bit 7 in the SYS_CONFIG0 register, and its default 0 means CRC_EN is off. The following polynomial is always used in this chip:

$y = x^8 + x^2 + x + 1$ equivalent to binary number is 100000111.

The CRC byte is an error detection byte that detects communication errors to and from the host and device. The CRC byte is the division remainder of the payload data of the CRC polynomial in which the polynomial function is $X^8 + X^2 + X + 1$. The 9-bit binary coefficients are: 100000111b. The payload data are either 2 or 3 bytes depending on the data transfer operation.

When CRC is enabled, the CRC byte only appends after the 16-bit command (2 bytes) and after the ADC data.

16-bit command byte: The host computes the CRC over the 16-bit command byte and appends the CRC to the command the third byte. The device performs the CRC calculation and compares the result to the CRC byte transmitted by the host. If the host and the device CRC values match, the command executes. Otherwise, the command does not execute, and the device asserts a CRC interrupt by pulling INTB pin to ground.

To generate the checksum, the data is left shifted by eight bits to create a number ending in eight Logic 0s. The polynomial is aligned such that its MSB is adjacent to the leftmost Logic 1 of the data. An exclusive OR (XOR) function is applied to the data to produce a new, shorter number. The polynomial is again aligned so that its MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated until the new result is less than the polynomial.

7.21 Diagnostic features

The AIO-AFE includes a robust protection circuit and advanced diagnostic feature for self-condition monitoring, as well as system-level condition monitoring.

7.21.1 Input diagnostics

In addition to typical open and short detection, the programmable output can also be used for various types of input impedance measurement. Moreover, by switching the polarity of the output voltage or current source, the Input common mode voltage could be removed.

7.21.2 Input underrange and overrange

Every configured logical channel has the feature to detect ADC under- or overrange condition with user-programmable thresholds. In addition to the status registers, an OR'ed of overrange/underrange could also be set as interrupt (INTB) for flexibility.

7.21.3 Voltage supplies rails monitoring

The AIO-AFE on-demand can read and monitor the following values: HVDD, HVSS, and VDD, VLDO.

When these values are read, a global alarm is issued if the read value is out of the programmed window threshold.

The HVDD, HVSS, and VDD also have a dedicated UVLO detect circuit for the purpose of POR.

7.21.4 Thermal shutdown

The AIO-AFE includes a thermal shutdown circuit to protect the device for overtemperature. The thermal shutdown circuit asserts the global alarm for warning purposes if the temperature exceeds 145 °C. The thermal shutdown turns off the chip for protection purposes if the temperature exceeds 165 °C.

The AIO-AFE integrates a temperature sensor that allows continuous monitoring of the die temperature by reading the DIE_TEMP register. In addition, a user-programmable alarm threshold can provide early overtemperature warning.

7.21.5 Monitoring with global alarm

The AIO-AFE provides a flexible and configurable global alarm to allow the user to configure it based on the specific application and need.

For device and input monitoring, various alarms and interrupts are available including programmable alarm thresholds for (1) temperature alarm, (2) channel-based overrange, and underrange alarms.

The alarm-clearing behavior is determined by GLOBAL_ALRM_STICKY.

Table 31. Alarm and interrupt

GLOBAL ALARM ENABLE 0x32\h	15	OVER_TEMP_ALRM	RW	0x0	Overtemperature warning at 145 °C.
	14	HVDD_ALRM	RW	0x0	Enable alarm for HVDD supply detect below preset threshold.
	13	HVSS_ALRM	RW	0x0	Enable alarm for HVSS supply detect below preset threshold.
	12	DVDD_ALRM	RW	0x0	Enable alarm for DVDD supply detect below preset threshold.
	11	Reserved	RW	0x0	Unused
	10	GPI_POS_ALRM	RW	0x0	Enable alarm for rising edge detected at any of the GPI pins.
	9	GPI_NEG_ALRM	RW	0x0	Enable alarm for falling edge detected at any of the GPI pins.
	8	CONFIG_ERROR_ALRM	RW	0x0	Enable alarm for register configuration error.
	7	OVRRNG_ALRM	RW	0x0	Enable alarm when one or more data channels are overrange.
	6	UNDRNG_ALRM	RW	0x0	Enable alarm when one or more data channels are underrange.
	5	OVRLOAD_ALRM	RW	0x0	Enable alarm when one or more data channels are overloaded or underloaded.
	4	EXTCLK_FREQ_ALRM	RW	0x0	Enable alarm when XTAL or EXTCLK frequency varies with internal CLK by XX.
	3	PGA_OV_ALRM	RW	0x0	Enable alarm when one or more data channels are overvoltage stressing the PGA.
	2	VIEX_OV_ALRM	RW	0x0	Enable alarm when excitation voltage source is overloaded.
	1	VIEX_OI_ALRM	RW	0x0	Enable alarm when excitation current source is overloaded.
	0	TEMP_ALRM	RW	0x0	Enable programmable temperature alarm, the triggering threshold is set in THRS_TEMP register bits.
GLOBAL ALARM INTERRUPT 0x33\h	15	OVER_TEMP_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	14	HVDD_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	13	HVSS_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	12	DVDD_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	11	Reserved	RW	0x0	Unused
	10	GPI_POS_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	9	GPI_NEG_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	8	CONFIG_ERROR_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	7	OVRRNG_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	6	UNDRNG_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	5	OVRLOAD_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	4	EXTCLK_FREQ_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	3	PGA_OV_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	2	VIEX_OV_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	1	VIEX_OI_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.
	0	TEMP_INT	RW	0x0	Bit clear behavior is controlled by GLOBAL_ALRM_STICKY.

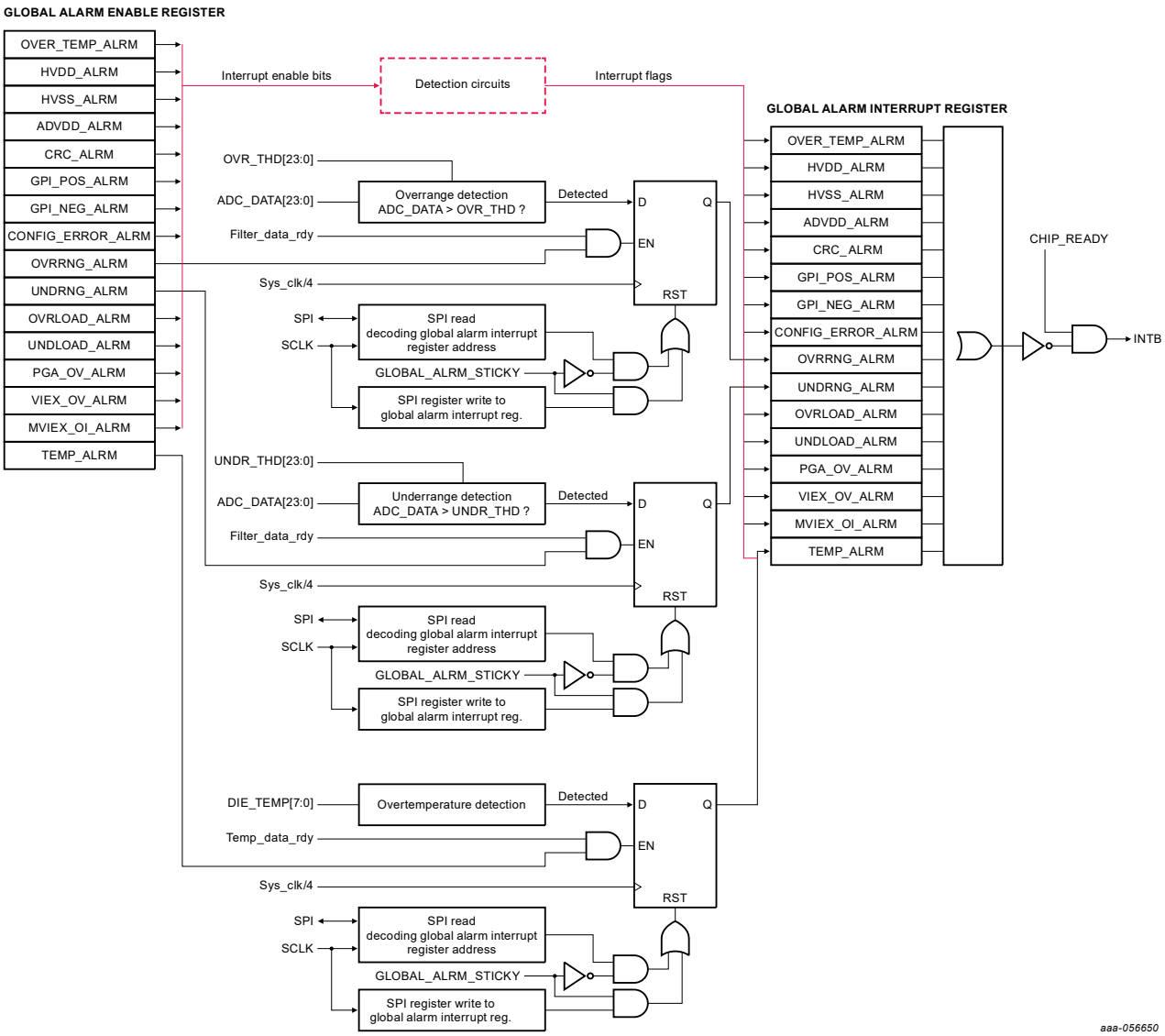


Figure 44. Alarm

7.21.5.1 Interrupts

The INTB pin of the chip is a NOR function of the internal 15-bit of global alarm interrupt registers. Each of these global alarm interrupt register bits can be written 1 or 0, respectively, to enable or disable the SPI's register write command to global alarm enable register (Address = 0x2E\h).

Note: *Using SPI write to enable all the CH_DATA readback could be prepended with a channel-specific status byte by enabling STATUS_EN, each of the status bits is OR's of all 15 channels.*

The logic equivalence is shown in Figure 45.

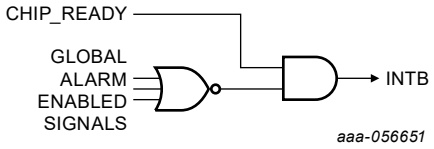


Figure 45. Interrupt

Note: *The status byte is only prepended when reading out the ADC data with the SYS_CONFIG0 bit 6th set to 1.*

Each individual status bit is concatenated in a single byte listed in Table 32.

Table 32. Status byte description

Status bit function	Representation base		Bit index
	channel	global	
ADC underloaded or overloaded	X		7
ADC over user set threshold	X		6
ADC under user set threshold	X		5
VIEX_OV_ALRM or VIEX_OI_ALRM	X		4
PGA is overloaded	X		3
Current die temperature over user set threshold		X	2
Clock alarm error		X	1
Result of 3-bit logical OR of HVDD_ALRM, HVSS_ALRM, and HVDD_ALRM signals		X	0

These status bits behave independently of the SYS_CONFIG.3 state. They behave depending on what CMD_xy was issued:

Command CMD_SS: Status becomes sticky until the host initiates another conversion, then the status will update accordingly. The host can clear this channel base status by issuing CMD_CLEAR_DATA or CMD_CLEAR_REG.

Commands CMD_MM, CMD_MC, and CMD_SC: During multichannel or continuous conversions, these status bits will be updated accordingly per/channel based on its live status. Therefore, the last conversion channel base status bits will not be clear until the host wants to clear them by issuing CMD_CLEAR_DATA or CMD_CLEAR_REG.

This behavior applies for channel-base status during active conversion. The 5-MSB status bits are ADC underload, ADC overload, ADC underrange, ADC overrange, VIEX over-/under-, and PGA overload.

Global alarm interrupt register (Address 0x2F\h) can be configured as non-sticky or sticky behavior via programing SYS_CONFIG0.3 (bit 3). Programming SYS_CONFIG0.3 = 0, non-sticky, and SYS_CONFIG0.3 = 1, sticky behavior to all 15-bit of global alarm interrupt register (GAI). When the sticky option is selected, each GAI register bit will be set by hardware if there is an interrupt event occurs respect to each functional bit that described in global alarm interrupt register. The host needs to clear whatever bit is set by writing 1, if the host again needs to see the next interrupt event.

Note: *Writing 1 to the bit that is 0, will not alter it to 1.*

7.21.5.2 Latched and not-latched alarm

When the non-sticky option is selected, the content of the GAI register will reflect whatever the current chip or channel conversion status at the time the host reads this register. The functionality of the INTB pin depends on how the host programs the SYS_CONFIG0.3 bit. For example, SYS_CONFIG0.3 = 1, sticky, INTB will be deasserted low until all interrupts are clear, whereas SYS_CONFIG0.3 = 0, non-sticky, INTB will be low

whenever there is an interrupt occurring, and high whenever there is no interrupt at all. INTB might be toggling, meaning interrupt comes and goes regardless if host keeps reading the GAI register.

The interrupt logic equation is shown below:

$$INTB = \sim (glb\_alarm\_intr\_flags \,||\, reset\_int\_flag\_r);$$

Note: *The reset_int_flag_r is set after the POR. It might also be set if a POR glitch has occurred. Then INTB will be asserted low.*

It is recommended that the host reads SYS_STATUS0 register to see if the CHIP_READY is set before communication to the chip. Upon reading this register, INTB will be clear and deasserted high, waiting for the next interrupt event.

- CRC_ERROR status can now be read via SPI through SYS_STATUS0 register (bit 12) and it is clear on read. The CRC_ERROR flag can also be routed out to GPIO2 when SYS_CONFIG0 bit 0 is set to 1. GPIO2 now has dual function: when SYS_CONFIG0.0 = 0: general-purpose I/O and 1: CRC_ERROR flag output.

7.21.6 Configuration or loading error

When a user-configuration error or chip error is detected, CONFIG_ERROR_INT will be asserted. A chip-configuration error could be triggered by command CMD_RELOAD during readback of the on-chip NVM module, the readback data was found inconsistent between two reads.

7.22 Channel-based configuration

The AIO-AFE has:

- Configurable analog output
- Configurable analog input
- Digital GPIOs (two can take analog inputs)
- On-chip scaled reference voltages for built-in self-test (BIST) functions

The eight logical channels are used to configure the main parameters of the input channels, such as PGA gain, mux selection, calibration coefficients, data rate, and digital filters. With the channel-based configurations, the user may switch among the configured channels without the need to perform multiple SPI transactions to set up various configurations before each ADC conversion.

7.23 Use of factory-calibrated coefficients

The AIO-AFE part is supplemented with factory-calibrated coefficients (CAL). The coefficients will be calibrated at the NXP factory and stored in the non-volatile memory. Each gain and offset coefficient is full 20-bit.

To use the factory coefficients, the user will need to pick the appropriate coefficient pointer in the CH_CONFIG registers.

Table 33. Factory calibration

Pointer	Gain register	ADDR\h	Offset register	ADDR\h	NVM stored coefficient and setting
0	GAIN_COEF0[23:0]	50	OFFSET_ COEF0[23:0]	58	VOUT, single-ended, measured at AIO-GND
1	GAIN_COEF1[23:0]	51	OFFSET_ COEF1[23:0]	59	COUT, Rs = 50 Ω, singled-ended, measured at AIO-GND
2	GAIN_COEF2[23:0]	52	OFFSET_ COEF2[23:0]	5A	VIN, via VSA, sourced from calibrated AIO-GND
3	GAIN_COEF3[23:0]	53	OFFSET_ COEF3[23:0]	5B	CIN, Rs = 50 Ω, via CSA, CISW, sourced at AIO-GND

Table 33. Factory calibration*...continued*

Pointer	Gain register	ADDR\h	Offset register	ADDR\h	NVM stored coefficient and setting
4	GAIN_COEF4[23:0]	54	OFFSET_ COEF4[23:0]	5C	ADCP-ADCN (GPIO0-GPIO1) differential
5	GAIN_COEF5[23:0]	55	OFFSET_ COEF5[23:0]	5D	VIN, via AI1P, PGA = 1
6	GAIN_COEF6[23:0]	56	OFFSET_ COEF6[23:0]	5E	VIN, via AI1N, PGA = 1
7	GAIN_COEF7[23:0]	57	OFFSET_ COEF7[23:0]	5F	VIN, via AI1P-AI1N, PGA = 16

7.24 Input-pin termination and protection diodes

An external 3 kΩ or higher series resistor is recommended for every analog input pin (AIxx).

Note: *The protection diodes, at each analog input, with the external series 5 kΩ resistor serves as surge protection and fast-transient immunity. A low-leakage architecture is used to minimize the diode leakage to be less than 1 nA at room.*

7.25 Current output source

The programmable current source could also be used as an excitation source for input impedance measurement, biasing of RTD, or built-in self-test (BIST) for channel readback.

As the excitation V/I source is generated from VREF, the measurement associated with it is ratiometric. This is desirable as the drift of VREF is less of a concern.

7.26 GPIOs

The GPIO control and data registers are organized by 4x10 bits register.

GPI_DATA (0x23\h): Read(R) only register and it detects a level logic from the pad.

GPIO_CONFIG0 (0x24\h): Read/Write(R/W) GPO_EN register. It enables an output path.

GPIO_ CONFIG1(0x25\h): R/W GPIO_CON register. It connects the internal I/O to the pad.

GPIO_CONFIG2 (0x26\h): R/W GPI_ENABLE. It enables the input path to allow reading data from the pad, looping back from GPO_DATA register and, or GPIO edges detection.

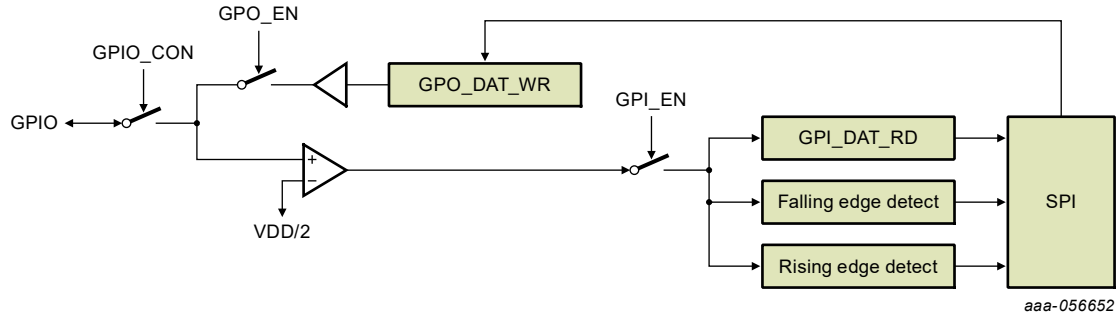


Figure 46. GPIO structure

While GPI_EN = 1 and GPIO_CON = 1, any transition from 0 ≥ 1 (positive edge) or 1 ≥ 0 (negative edge) the edge-detection register (GPI_EDGE_POS at 0x27 and GPI_EDGE_NEG at 0x28) will be set to 1. This edge-detection register is defined as sticky by nature and requires the host to clear it by writing 1 to the bit that is set to 1.

7.27 Chip reset

The AIO-AFE has two types of reset mode: Chip POR, and Command RESET.

When in reset, all HV-input pins, GPIO pins are in High-Z input mode, internal voltage reference is used, ADC digital filters are cleared, all user registers are set to their default values, and all OTP shadow register content will be reloaded. The input clock source will default back to internal RC oscillator.

Command CMD_RESET is the same as a hardware reset.

Command CMD_CLEAR_REG operates similarly to software reset. It clears all user-accessible registers to default values except SYS_CONFIG0.9:8, CK_SRC_SEL[1:0].

Command CMD_RELOAD will reload the stored content from the on-chip non-volatile memory to the shadow register.

7.28 Analog input and output ranges

7.28.1 Input types and ranges

The AIO-AFE covers any combination of the input type signals and multiple ranges. The input types combination includes bipolar and unipolar signals, as well as single-ended and differential signals.

The input ranges are a function of the channel gain (CH_GAIN) and are determined by the following equation:

$$Input\ \ range = \pm 10\ \ V \big/ CH\_GAIN$$

All the analog input ranges and types have the full range or overload range 1.25 times the nominal or linear range.

The max overload differential range is ±25 V for CH_GAIN = 1 and the correspondent max linear range is ±20 V.

Linear differential voltage input ranges:

- ±20 V; ±0.25 V

The max overload single-ended range is ±12.5 V for CH_GAIN = 1 and the correspondent max linear range is ±10 V.

Linear single-ended voltage input ranges:

- ±10 V; ±0.125 V

In addition, the AFE fits exactly the input current ranges with the most common external resistors value.

- ±20 mA; 0 mA to 20 mA; 4 mA-20 mA
- 25 Ω; 50 Ω; 100 Ω; 200 Ω; 250 Ω; 500 Ω;

The AIO-AFE provides a high-input impedance of 1 GOhm and low-input leakage current. In combination with its low noise and low offset drift PGA allows accurate measurement of RTD and TC. The NAFE93352 provides a precise programmable current excitation source to enable the measurement of resistance and RTD sensor.

Table 34 reports the nominal ranges, the max and min values, full-scale range, and resolution for the different input type signals and PGA gain setting.

Table 34. HV input ranges and resolutions

Nominal range values (V)		
Type	PGA gain setting	
	1	16
Bipolar DIFF	±20.00000	±1.25
BipolarSE	±10.00000	±0.625
Unipolar DIFF	±10.00000	±0.625
Unipolar SE	±10.00000	±0.625
Min and max values (V)		
Type	PGA gain setting	
	1	16
Bipolar DIFF	±25.00000	±1.5625
BipolarSE	±12.50000	±0.7812
Unipolar DIFF	±12.50000	±0.7812
Unipolar SE	±12.50000	±0.7812
Full range scale (V)		
Type	PGA gain setting	
	1	16
Bipolar DIFF	50	±1.5625
BipolarSE	25	±0.7812
Unipolar DIFF	25	±0.7812
Unipolar SE	12.5	±0.7812
Resolution (V)		
Type	PGA gain setting	
	1	16
Bipolar DIFF	3.0e-6	186.3e-9
BipolarSE	3.0E-6	186.3E-9
Unipolar DIFF	3.0E-6	186.3E-9
Unipolar SE	3.0E-6	186.3E-9

7.28.2 Analog output ranges

Analog output to ADC code output transfer function.

$$DAC_{code} = -AO_v * \frac{2^N}{5*VREF}$$

$$AO_V = -Code * \frac{5*VREF}{2^N}$$

N is the DAC resolution. Up to 18-bit.

DAC codes span from -2^(N-1) to 2^(N-1)-1.

Table 35 reports the case for 18-bit resolution.

Vref = 2.5 V; DAC resolution = 18 bit;

Voltage AO FSR = 25 V; AOV resolution ±10 V = 95.36 µV

Current AO FSR = 50 mA; AIV resolution ±20 mA = 19.07 nA

Table 36 reports the case for 16-bit resolution.

Vref = 2.5 V; DAC resolution = 16 bit;

Voltage AO FSR = 25 V; AOV resolution ±10 V = 381.5 µV

Current AO FSR = 50 mA; AIV resolution ±20 mA = 762.9 nA

Table 35. 18-bit bipolar range

Voltage target output	Digital code (18-bit)	Voltage output (V)
12.5	131071	-12.499905
10	104858	-10.000038
5	52429	-5.000019
1 VLSB	1	-0.000095
0	0	0.000000
-1 VLSB	-1	0.000095
-5	-52429	5.000019
-10	-104858	10.000038
-12.5	-131072	12.500000
Current target output	Digital code	Current output (A)
0.025	131071	-0.025000
0.02	104858	-0.020000
0.004	20972	-0.004000
1	1	0.000000
0	0	0.000000
1	1	0.000000
-0.004	-20972	0.004000
-0.02	-104858	0.020000
-0.025	-131072	0.025000

Table 36. 16-bit bipolar range

Voltage target output	Digital code (16-bit)	Voltage output (V)
12.5 V	32767	-12.499619
10 V	26214	-9.999847
5 V	13107	-4.999924
1 VLSB	1	-0.000381
0 V	0	0.000000
-1 VLSB	-1	0.000381
-5 V	-13107	4.999924
-10 V	-26214	9.999847
-12.5 V	-32768	12.500000

Table 36. 16-bit bipolar range*...continued*

Current target output	Digital code	Current output (A)
25 mA	32767	-24.999E-3
20 mA	26214	-20.000E-3
4 mA	5243	-4.000E-3
1 ILSB	1	-762.939E-3
0 mA	0	000.000E+0
-1 ILSB	-1	762.939E-9
-4 mA	-5243	4.000E-3
-20 mA	-26214	20.000E-3
-25 mA	-32768	25.000E-3

The user can set the analog output to unipolar range by setting AIO_CONFIG.UNIPOLAR_AO_MODE = 1\b. The following are the transfer function and ranges:

LSBV = 25 V/(2^N)

AOV = 18.75 - DAC_CODE * LSBV

LSBI = 0.05 A/(2^N)

AOI = 0.0375 - DAC_CODE * LSBI

Table 37. 18-bit unipolar voltage output range

DI decimal	DI HEX 2C	Voltage output (V)
131071	01FFFF	6.250095
117965	01CCCD	7.499981
96993	017AE1	9.500027
55050	00D70A	13.500023
0	000000	18.750000
-39322	036666	22.500038
-70779	02EB85	25.500011
-112722	0247AE	29.500008
-131072	020000	31.250000

Table 38. 18-bit unipolar current output range

DI Decimal	DI HEX 2C	Current Output (A)
131071	01FFFF	0.012500
117965	01CCCD	0.015000
91750	016666	0.020000
13107	003333	0.035000
0	040000	0.037500
-65536	030000	0.050000
-91750	02999A	0.055000
-117965	023333	0.060000
-131072	020000	0.062500

7.29 Device calibration

The AIO-AFE products include 32 user-accessible calibration coefficient registers divided into three groups:

- Gain: GAIN_COEF0[23:0] to GAIN_COEF7[23:0]
- Offset: OFFSET_COEF0[23:0] to OFFSET_COEF7[23:0]
- Extra-CAL COEFF: EXTAR_COEF0[23:0] to EXTRA_COEF7[23:0]

To reduce the calibration error, the bit-width of gain, offset, and self-calibration coefficient registers are 24-bit wide, the same as the main ADC. The DAC will use the 18 MSB of this coefficient.

The above user-calibration coefficients can be read and written by the user. During device power-up or reset, the factory-calibrated coefficients that were stored in non-volatile memory (NVM) are loaded into these registers, if available.

In general, there are three categories of calibration coefficients:

- System offset and gain calibration coefficients for voltage or current input
- System offset and gain calibration coefficients for resistance and RTD input
- Self-calibration values

Table 39 describes the calibration coefficients registers.

Table 39. Calibration coefficients registers

Pointer	Gain register	ADDR\h	Offset register	ADDR\h	NVM stored coefficient and setting
0	GAIN_COEF0[23:0]	80	OFFSET_COEF0[23:0]	90	VOUT, single-ended, measured at AIO-GND
1	GAIN_COEF1[23:0]	81	OFFSET_COEF1[23:0]	91	COUT, Rs = 50 Ω, single-ended, measured at AIO-GND
2	GAIN_COEF2[23:0]	82	OFFSET_COEF2[23:0]	92	VIN, via VSA, sourced at AIO-GND
3	GAIN_COEF3[23:0]	83	OFFSET_COEF3[23:0]	93	CIN, Rs = 50 Ω, via CSA, CISW, sourced at AIO-GND
4	GAIN_COEF4[23:0]	84	OFFSET_COEF4[23:0]	94	CIN, Rs = 25 Ω, via AI1P-AI1N, CISW, PGA = 16
5	GAIN_COEF5[23:0]	85	OFFSET_COEF5[23:0]	95	VIN, via AI1P, PGA = 1
6	GAIN_COEF6[23:0]	86	OFFSET_COEF6[23:0]	96	VIN, via AI1N, PGA = 1
7	GAIN_COEF7[23:0]	87	OFFSET_COEF7[23:0]	97	VIN, via AI1P-AI1N, PGA = 16

Table 40. Optional coefficient registers

SELF-CAL REGISTER	NVM stored parameter	Nominal value	Stored format	Setting description
OPT_COEF0[23:0]	VREFPADC	2.5	(VREF/5)*2^24	REFP_ADC-REFN_ADC pin voltage
OPT_COEF1[23:0]	ADCP-VCM GAIN	—	—	—
OPT_COEF2[23:0]	ADCP-VCM OFFSET	—	—	—
OPT_COEF3[23:0]	ADCN-VCM GAIN	—	—	—
OPT_COEF4[23:0]	ADCN-VCM OFFSET	—	—	—
OPT_COEF5[23:0]		—	—	—
OPT_COEF6[23:0]	RTD_OFFSET1	0	(OFFSET/FSR)*2^24	250 uA, PGA = 16 V/V
OPT_COEF7[23:0]	RTD_GAIN1	1	Ga*2^24/4	250 uA, PGA = 16 V/V

7.29.1 Offset and gain calibration

The ideal transfer characteristic is

$$y = x$$

The actual transfer characteristic is

$$\boldsymbol{y} = G_a \cdot x + O_a$$

Where Ga and Oa are the actual gain and actual offset respectively.

The calibrated transfer characteristic is

$$\boldsymbol{y} = G_a \cdot G_c \cdot x + G_c \cdot (O_a - O_c)$$

Where Gc and Oc are the correction gain and offset coefficients, respectively.

$$\begin{cases} G_c = \frac{1}{G_a} \\ O_c = O_a \end{cases}$$

7.29.2 Voltage and current input gain and offset calibration procedures

This section describes the steps for performing offset and gain digital calibration for voltage or current input.

7.29.2.1 Steps for gain CAL

1. Set $O_c = 0$
2. Set $G_c = 1$
3. Put a voltage source equals to x1, about +100 % of full-scale.
4. Read $y_1 = G_a \cdot 1 \cdot x_1 + 1 \cdot \left(O_a + 0\right)$
5. Put a voltage source equals to x2, about -100 % of full-scale.
6. Read $y_2 = G_a \cdot 1 \cdot x_2 + 1 \cdot \left(O_a + 0\right)$
7. Calculate $G_a = \frac{y_2 - y_1}{(x_2 - x_1)}$
8. Set $\boldsymbol{G_c} = \frac{1}{\boldsymbol{G_a}}$

7.29.2.2 Steps for offset CAL

1. Plug $y_1 = G_a \cdot x_1 + O_a$
2. Calculate $O_a = \left(y_1 - G_a \cdot x_1\right)$
3. Set $\boldsymbol{O_c} = O_a$

7.29.3 Resistance and RTD input gain and offset calibration procedures

This section describes the steps in performing offset and gain digital calibration for resistance and RTD input.

7.29.3.1 Steps for resistance gain CAL

1. Set $O_c = 0$
2. Set $G_c = 1$
3. Put a resistance value equal to x1, about +80 % of full-scale range.
4. Read $y_1 = G_a \cdot 1 \cdot x_1 + 1 \cdot \left(O_a + 0\right)$
5. Put a resistance value equal to x2, about 0 % of full-scale range (for example, short-circuit the input).
6. Read $y_2 = G_a \cdot 1 \cdot x_2 + 1 \cdot \left(O_a + 0\right)$
7. Calculate $G_a = y_2 - y_1 \left(x_2 - x_1\right)$
8. Set $G_c = 1 G_a$

7.29.3.2 Steps for resistance offset CAL

1. Plug $y_1 = G_a \cdot x_1 + O_a$
2. Calculate $O_a = \left(y_1 - G_a \cdot x_1\right)$
3. Set $O_c = O_a$

7.29.4 ADC digital gain and offset calibration coefficients

Offset calibration registers are 24-bit wide and their values are in twos complement format with a minimum negative value equal to 80_0000\h and a maximum positive value equal to 7F_FFFF\h . A register value equal to 000000h has no offset correction.

$$Offset = 10 / 2^{24} \cdot 1 / GAIN \cdot \left(mod\left(hex2dec\left(COEF \right) + 2^{23},\ 2^{24} \right) - 2^{23} \right)$$

Gain Calibration registers are 24-bit wide and their values are straight binary format and map a gain range from 0 to 3.99999976158142. The unity gain value is 40_0000\h. Table 41 shows full range of gain factor correction.

$$Gain = COEF / 2^{22}$$

The AFE output equation with internal digital calibration is:

$$AFE_{OUT} = \left(ADCOUT + CAL\_OFFSET \right) \cdot CAL\_GAIN$$

Table 41. Analog input

ANALOG INPUT - OFFSET VOLTAGE		
Offset calibration coefficient (hexadecimal)	Offset calibration coefficient (decimal)	Offset calibration PGA = 1 (V)
7FFFFF	8388607	24.9999970
40000	4194304	12.5000000
000001	1	0.0000030
000000	0	0.0000000
FFFFFF	–1	–0.0000030
C00000	–4194304	–12.5000000
800000	–8388608	–25.0000000
ANALOG INPUT - OFFSET CURRENT		
7FFFFF	8388607	49.9999940
400000	4194304	25.0000000
000001	1	0.0000060
000000	0	0.0000000
FFFFFF	–1	–0.0000060
C00000	–4194304	–25.0000000
800000	–8388608	–50.0000000

7.29.5 DAC digital gain and offset calibration coefficients

Offset calibration registers are 18-bit registers and their values are in twos complement format.

Table 42. Gain and offset coefficients

ANALOG OUTPUT - GAIN COEFFICIENTS		
Gain calibration coefficient (hexadecimal)	Gain calibration coefficient (decimal)	Gain calibration factor = Gain_coeff./(2^16)
03FFFF	262143	3.9999847
020000	131072	2.0000000
010001	65537	1.0000153
010000	65536	1.0000000
00FFFF	65535	0.9999847
008000	32768	0.5000000
000000	0	0.0000000

Table 42. Gain and offset coefficients*...continued*

ANALOG OUTPUT - OFFSET VOLTAGE		
Offset calibration coefficient (hexadecimal)	Offset calibration coefficient (decimal)	Offset calibration voltage out (V)
01FFFF	131071	12.4999046
010000	65536	6.2500000
000001	1	0.0000954
000000	0	0.0000000
03FFFF	–1	–0.0000954
030000	–65536	–6.2500000
020000	–131072	–12.5000000
ANALOG OUTPUT - OFFSET VOLTAGE		
Offset calibration coefficient (hexadecimal)	Offset calibration coefficient (decimal)	Offset calibration voltage out (V)
01FFFF	65536	24.9998093
010000	1	12.5000000
000001	0	0.0001907
000000	–1	0.0000000
03FFFF	–65536	–0.00019107
030000	–131072	–12.5000000
020000	65536	–25.0000000

7.30 Noise performance

The AIO-AFE noise performance of the analog input depends on the device configuration: data rate, PGA gain, digital filter order, and Settling mode configuration. Two significant factors that affect noise performance are data rate and PGA gain. Decreasing the data rate results in a proportional decrease of total noise because the equivalent noise bandwidth of the digital filter is reduced proportionally with the data rate. Increasing the gain reduces input referred noise because the noise of the PGA is lower than the noise of the ADC. Noise performance also depends on the shape digital filter because the order of the digital filter decreases the equivalent noise bandwidth, which results in lower noise.

Table 43 lists the noise performance of gain equals 1 and 16 (corresponding input full-scale ranges of ±25 V and ±1.563 V) as input-referred values.

The noise performance data are in units of µVRMS (RMS = root mean square) under the conditions listed.

The data shown in the noise performance tables represent typical AFE performance in normal settling at Ta = 25 °C and internal 2.5 V reference voltage. The noise data is acquired with inputs shorted and consecutive ADC readings for a period of 10 seconds or 1024 data points, whichever occurs first. Repeated noise measurements may yield higher or lower noise performance results because of the statistical nature of noise.

Table 43 reports the noise performance versus data rate and PGA gain setting.

ENOB is calculated from the RMS noise applying the following formula:

$$ENOB = MIN\left(LOG\left(Full\text{-}scale\ \ range \middle/ Noise\_RMS,\ \ 2\right),\ \ 24\right)$$

$$Full\text{-}scale\ \ range = 10 \middle/ PGA$$

Table 43. Noise µVrms (24-bit option)

Code	Data rate	4,608,000	Estimate noise (µVrms) vs PGA gain setting	
		OSR	1	16
0	**576000**	8	**27947.4**	**1746.7**
1	**384000**	12	**7547.4**	**471.8**
2	**288000**	16	**2987.0**	**186.8**
3	**192000**	24	**824.9**	**51.9**
4	**144000**	32	**355.5**	**22.9**
5	**96000**	48	**156.3**	**10.7**
6	**72000**	64	**118.1**	**8.3**
7	**48000**	96	**92.9**	**6.6**
8	**36000**	128	**80.1**	**5.7**
9	**24000**	192	**65.4**	**4.6**
10	**18000**	256	**56.6**	**4.0**
11	**12000**	384	**46.2**	**3.3**
12	**9000**	512	**40.0**	**2.8**
13	**6000**	768	**32.7**	**2.3**
14	**4500**	1024	**28.3**	**2.0**
15	**2250**	2048	**20.0**	**1.4**
16	**1125**	4096	**14.2**	**1.0**
17	**800**	5760	**12.0**	**0.8**
18	**600**	7680	**10.4**	**0.7**
19	**400**	11520	**8.5**	**0.6**
20	**300**	15360	**7.4**	**0.5**
21	**200**	23040	**6.1**	**0.4**
22	**100**	46080	**4.4**	**0.3**
23	**60**	76800	**3.4**	**0.2**
24	**50**	92160	**3.2**	**0.2**
25	**40**	115200	**2.9**	**0.2**
26	**30**	153600	**2.5**	**0.2**
27	**20**	230400	**2.2**	**0.1**
28	**15**	307200	**2.0**	**0.1**

Table 44. ENOB (24-bit option)

Code	Data rate	4,608,000	Estimate ENOB vs PGA gain setting	
		OSR	1	16
0	**576000**	8	**10.8**	**10.8**
1	**384000**	12	**12.7**	**12.7**
2	**288000**	16	**14.0**	**14.0**
3	**192000**	24	**15.9**	**15.9**
4	**144000**	32	**17.1**	**17.1**

Table 44. ENOB (24-bit option)*...continued*

Code	Data rate	4,608,000	Estimate ENOB vs PGA gain setting	
		OSR	1	16
5	**96000**	48	**18.3**	**18.2**
6	**72000**	64	**18.7**	**18.5**
7	**48000**	96	**19.0**	**18.9**
8	**36000**	128	**19.3**	**19.1**
9	**24000**	192	**19.5**	**19.4**
10	**18000**	256	**19.8**	**19.6**
11	**12000**	384	**20.0**	**19.9**
12	**9000**	512	**20.3**	**20.1**
13	**6000**	768	**20.5**	**20.4**
14	**4500**	1024	**20.8**	**20.6**
15	**2250**	2048	**21.3**	**21.1**
16	**1125**	4096	**21.7**	**21.6**
17	**800**	5760	**22.0**	**21.8**
18	**600**	7680	**22.2**	**22.0**
19	**400**	11520	**22.5**	**22.3**
20	**300**	15360	**22.7**	**22.5**
21	**200**	23040	**23.0**	**22.8**
22	**100**	46080	**23.5**	**23.3**
23	**60**	76800	**23.8**	**23.6**
24	**50**	92160	**23.9**	**23.7**
25	**40**	115200	**24.0**	**23.9**
26	**30**	153600	**24.0**	**24.0**
27	**20**	230400	**24.0**	**24.0**
28	**15**	307200	**24.0**	**24.0**

Table 45. Noise-free resolution (24-bit option)

Code	Date rate	4,608,000	Estimate noise-free resolution vs PGA gain setting	
		OSR	1	16
0	**576000**	8	**8.5**	**8.5**
1	**384000**	12	**10.4**	**10.4**
2	**288000**	16	**11.7**	**11.7**
3	**192000**	24	**13.6**	**13.6**
4	**144000**	32	**14.8**	**14.7**
5	**96000**	48	**16.0**	**15.8**
6	**72000**	64	**16.4**	**16.2**
7	**48000**	96	**16.7**	**16.5**
8	**36000**	128	**16.9**	**16.7**
9	**24000**	192	**17.2**	**17.0**

Table 45. Noise-free resolution (24-bit option)*...continued*

Code	Date rate	4,608,000	Estimate noise-free resolution vs PGA gain setting	
		OSR	1	16
10	**18000**	256	**17.4**	**17.2**
11	**12000**	384	**17.7**	**17.5**
12	**9000**	512	**17.9**	**17.7**
13	**6000**	768	**18.2**	**18.0**
14	**4500**	1024	**18.4**	**18.2**
15	**2250**	2048	**18.9**	**18.7**
16	**1125**	4096	**19.4**	**19.2**
17	**800**	5760	**19.7**	**19.5**
18	**600**	7680	**19.9**	**19.7**
19	**400**	11520	**20.2**	**20.0**
20	**300**	15360	**20.4**	**20.2**
21	**200**	23040	**20.7**	**20.5**
22	**100**	46080	**21.1**	**21.0**
23	**60**	76800	**21.5**	**21.3**
24	**50**	92160	**21.6**	**21.4**
25	**40**	115200	**21.7**	**21.6**
26	**30**	153600	**21.9**	**21.8**
27	**20**	230400	**22.1**	**22.0**
28	**15**	307200	**22.3**	**22.2**

Table 46. Noise µVrms (16-bit option)

Code	Data rate	4,608,000	Estimate noise (µVrms) vs PGA gain setting	
		OSR	1	16
0	**576000**	8	**27948.8**	**1746.8**
1	**384000**	12	**7552.5**	**472.1**
2	**288000**	16	**2999.7**	**187.6**
3	**192000**	24	**869.6**	**54.7**
4	**144000**	32	**449.6**	**28.6**
5	**96000**	48	**316.6**	**20.3**
6	**72000**	64	**299.6**	**19.1**
7	**48000**	96	**290.5**	**18.4**
8	**36000**	128	**286.7**	**18.1**
9	**24000**	192	**283.0**	**17.8**
10	**18000**	256	**281.1**	**17.7**
11	**12000**	384	**279.2**	**17.5**
12	**9000**	512	**278.2**	**17.4**
13	**4500**	1024	**276.8**	**17.3**
14	**2250**	2048	**276.0**	**17.3**

Table 46. Noise µVrms (16-bit option)*...continued*

Code	Data rate	4,608,000	Estimate noise (µVrms) vs PGA gain setting	
		OSR	1	16
15	**1125**	4096	**275.7**	**17.2**
16	**600**	7680	**275.5**	**17.2**
17	**450**	10240	**275.4**	**17.2**
18	**300**	15360	**275.4**	**17.2**
19	**200**	23040	**275.4**	**17.2**
20	**100**	46080	**275.3**	**17.2**
21	**60**	76800	**275.3**	**17.2**
22	**50**	92160	**275.3**	**17.2**
23	**30**	153600	**275.3**	**17.2**
24	**25**	184320	**275.3**	**17.2**
25	**20**	230400	**275.3**	**17.2**
26	**10**	460800	**275.3**	**17.2**
27	**5**	921600	**275.3**	**17.2**
28	**2.5**	1843200	**275.3**	**17.2**

Table 47. ENOB (16-bit option)

Code	Data rate	4,608,000	Estimate ENOB vs PGA gain setting	
		OSR	1	16
0	**576000**	8	**10.8**	**10.8**
1	**384000**	12	**12.7**	**12.7**
2	**288000**	16	**14.0**	**14.0**
3	**192000**	24	**15.8**	**15.8**
4	**144000**	32	**16.0**	**16.0**
5	**96000**	48	**16.0**	**16.0**
6	**72000**	64	**16.0**	**16.0**
7	**48000**	96	**16.0**	**16.0**
8	**36000**	128	**16.0**	**16.0**
9	**24000**	192	**16.0**	**16.0**
10	**18000**	256	**16.0**	**16.0**
11	**12000**	384	**16.0**	**16.0**
12	**9000**	512	**16.0**	**16.0**
13	**4500**	1024	**16.0**	**16.0**
14	**2250**	2048	**16.0**	**16.0**
15	**1125**	4096	**16.0**	**16.0**
16	**600**	7680	**16.0**	**16.0**
17	**450**	10240	**16.0**	**16.0**
18	**300**	15360	**16.0**	**16.0**
19	**200**	23040	**16.0**	**16.0**

Table 47. ENOB (16-bit option)*...continued*

Code	Data rate	4,608,000	Estimate ENOB vs PGA gain setting	
		OSR	1	16
20	**100**	46080	**16.0**	**16.0**
21	**60**	76800	**16.0**	**16.0**
22	**50**	92160	**16.0**	**16.0**
23	**30**	153600	**16.0**	**16.0**
24	**25**	184320	**16.0**	**16.0**
25	**20**	230400	**16.0**	**16.0**
26	**10**	460800	**16.0**	**16.0**
27	**5**	921600	**16.0**	**16.0**
28	**2.5**	1843200	**16.0**	**16.0**

Table 48. Noise-free resolution (16-bit option)

Code	Data rate	4,608,000	Estimate noise-free resolution vs PGA gain setting	
		OSR	1	16
0	**576000**	8	**8.5**	**8.5**
1	**384000**	12	**10.4**	**10.4**
2	**288000**	16	**11.7**	**11.7**
3	**192000**	24	**13.5**	**13.5**
4	**144000**	32	**14.4**	**14.4**
5	**96000**	48	**14.9**	**14.9**
6	**72000**	64	**15.0**	**15.0**
7	**48000**	96	**15.1**	**15.1**
8	**36000**	128	**15.1**	**15.1**
9	**24000**	192	**15.1**	**15.1**
10	**18000**	256	**15.1**	**15.1**
11	**12000**	384	**15.1**	**15.1**
12	**9000**	512	**15.1**	**15.1**
13	**4500**	1024	**15.1**	**15.1**
14	**2250**	2048	**15.1**	**15.1**
15	**1125**	4096	**15.1**	**15.1**
16	**600**	7680	**15.1**	**15.1**
17	**450**	10240	**15.1**	**15.1**
18	**300**	15360	**15.1**	**15.1**
19	**200**	23040	**15.1**	**15.1**
20	**100**	46080	**15.1**	**15.1**
21	**60**	76800	**15.1**	**15.1**
22	**50**	92160	**15.1**	**15.1**
23	**30**	153600	**15.1**	**15.1**
24	**25**	184320	**15.1**	**15.1**

Table 48. Noise-free resolution (16-bit option)*...continued*

Code	Data rate	4,608,000	Estimate noise-free resolution vs PGA gain setting	
		OSR	1	16
25	**20**	230400	**15.1**	**15.1**
26	**10**	460800	**15.1**	**15.1**
27	**5**	921600	**15.1**	**15.1**
28	**2.5**	1843200	**15.1**	**15.1**

8 Limiting values

8.1 Absolute maximum rating

Table 49. Absolute maximum rating

ABSOLUTE MAXIMUM RATING			
Description	**MIN**	**MAX**	**UNITS**
HVDD to AGND	-0.3	33	V
AGND to HVSS	-0.3	33	V
HVDD to HVSS	-0.3	55	V
AVDD to AGND	-0.3	5.5	V
DVDD to DGND	-0.3	5.5	V
AGND to DGND	-0.3	0.3	V
Screw terminal AIO to HVDD (include in series external diodes and sense resistor)	-70	36	V
Screw terminal AIO to HVSS, with external diode and series 50 Ω sense resistor	-36	65	V
AI1P, AI1N, Vsense, IsenseP, IsenseN to HVDD include 5 kΩ external current limiting resistor	-70	36	V
AI1P, AI1N, Vsense, IsenseP, IsenseN to HVSS, with external 5 kΩ resistor in series for current limit with a duration of less than one hour	-36	65	V
CISW to HVSS, or CISW to HVDD if internal the CISW switch is off	-60	60	V
CISW to GND, when CISW ON and AFE is functionally operating	-36	36	V
GPIO0.. GPIO4 to DGND	-0.3	VDVDD+0.3	V
OSCIN to DGND	-0.3	VDVDD+0.3	V
SCLK, DIN, DOUT, CSB, ADCDRDY, SYNCDAC, SYNCADC, INTB to DGND	-0.3	VDVDD+0.3	V
LDOCAP to DGND	-0.3	2.1	V
REFEXT/REFNR, REFDACBUF, REFADCBUF to AGND	-0.3	VAVDD+0.3	V
AGNDADCREF, AGNDDACREF to AGND	-0.3	0.3	V
COMPIN, HARTIN to HVVD	—	0.3	V
HVSS to COMPIN, HARTIN	—	0.3	V

8.2 Safe operating area

The safe operating area of the NAFE93352 represents the max power dissipation and maximum ambient temperature allowable to meet the maximum operating junction temperature, Tjmax = 150 °C.

The system designers should design their system in order to not exceeed maximum operating junction temperature, Tjmax = 150 °C.

The junction temperature is a function of ambient temperature, thermal resistance and power dissipation and is given by the following equation:

$$Tj = Tamb + Rth*Pdis$$

So given the package thermal resistance, the Tamb and Pdis should fit in the safe operating area, as reported in Figure 47.

Example: Tjmax = 150 °C, Rth = 35 °C/W, Pdismax = 1W

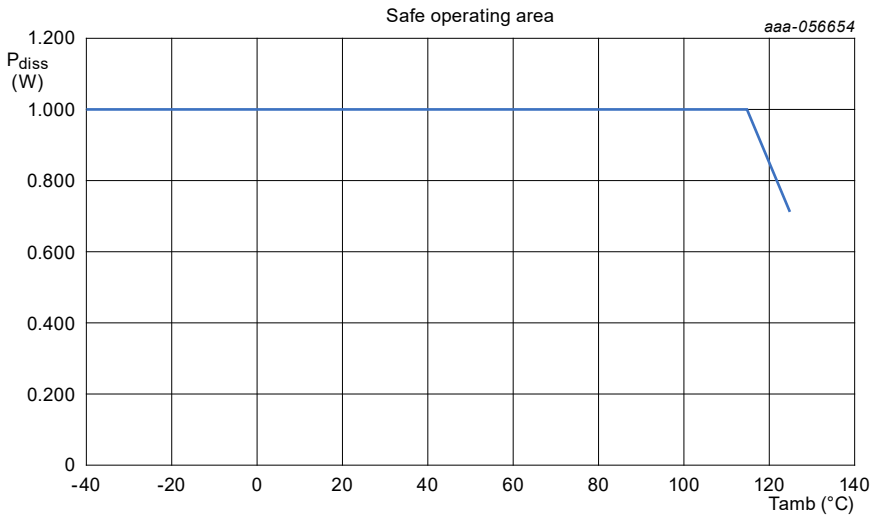


Figure 47. Safe operating area

To increase the safety, the NAFE93352 monitors the temperature junction with an integrated temperature sensor and provides an automatic warning alarm in case the Tj is over 145 °C.

9 Thermal characteristics

Table 50. Thermal characteristics

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Thermal characteristics					
Description		**Symbol**	**MIN**	**MAX**	**UNITS**
Operating temperature	—	—	—	—	°C
Ambient	—	Ta	-40	125	
Junction	—	Tj	-40	150	
Storage temperature	—	TSTO	-55	150	°C
Peak package reflow temperature	[1] [2]	TPPRT	—	260	°C
Junction to board (bottom exposed pad soldered to board)	[3]	RθJB	—	20	°C/W
Junction to ambient with four-layer board	[4] [5]	RθJA	—	35	°C/W

[1] Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.

[2] NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes) and enter the core ID to view all orderable parts and parametric.

[3] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

[4] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

[5] Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.

10 Electrical specifications

10.1 Analog output

Table 51. Analog output electrical characteristics

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, typical values are at Ta = 40 ºC, DAC at 100 ksps, analog output (AO) is connected to an external 1 kΩ load resistor connected to ground. The parameters are characterized to their linear ranges, unless otherwise stated.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE OUTPUT RANGE						
Voltage full-scale range	VOUT	±12.5 V full range	—	±12.5	—	V
Voltage linear range	VOUT		-10	—	10	V
VOLTAGE OUTPUT INITIAL ACCURACY WITHOUT CALIBRATION						
Total unadjusted error	VTUE	TUE [V/V] = (GEv+OE+INL)/FS				
Total unadjusted error at room temperature	VTUE_Ai	Initial accuracy without CAL coefficients. Internal reference. Ta = 40 °C. AO_TCC = 00\b	—	1.1	1.6	%FS
Total unadjusted error over temperature	VTUE_OTi	Initial accuracy without CAL coefficients. Internal reference. Ta = -25 °C to 105 °C. AO_TCC = 00\b	—	1.2	1.7	%FS
Offset error	VOFF_Ai	Initial offset error without factory CAL coefficients. Internal reference. Ta = 40 °C. AO_TCC = 00\b	-30	-15	0	mV
Gain error	VGE_Ai	Initial gain error without factory CAL coefficients. Internal reference. Ta = 40 °C. AO_TCC = 00\b	0.5	1.0	1.5	%FS
INL error	VINL_Ai	Initial offset error without factory CAL coefficients. External voltage reference. Ta = 40 °C. AO_TCC = 00\b	-0.3	0.2	0.3	mV
VOLTAGE OUTPUT INITIAL ACCURACY WITH USER CALIBRATION COEFFICIENTS						
Total unadjusted error		TUE [V/V] = (GEv+OE+INL)/FS				
Total unadjusted error	VTUE_Auc	Initial accuracy with user calibration. Internal voltage reference, AO_TCC = 00\b. Ta = 40 °C.	—	0.0035	0.01	%FS
Total unadjusted error over temperature	VTUE_OTuc	Initial accuracy with user calibration. Internal voltage reference, AO_TCC = 00\b. Ta = -25 °C to 105 °C	—	0.02	0.08	%FS
		Initial accuracy with user calibration at 40 °C, Internal voltage reference, AO_TCC = 00\b. Ta = -40 °C to 125 °C	—	0.025	0.1	
Calibrated offset error	VOFF_Auc	Initial calibrated offset error with user CAL coefficients. Internal reference, Ta = 40 °C	-0.1	0.025	0.1	mV
Calibrated gain error	VGE_Auc	Initial accuracy with user calibration. Internal voltage reference, AO_TCC = 00\b. Ta = 40 °C.	—	0.0013	0.005	%FS
	VGE_OTuc	Initial accuracy with user calibration. Internal voltage reference, AO_TCC = 00\b. Ta = -25 °C to 105 °C	—	0.0175	0.07	
		Initial accuracy with user calibration at 40 °C, Internal voltage reference, AO_TCC = 00\b. Ta = -40 °C to 125 °C	—	0.02	0.08	
INL error	VINLuc	Initial calibrated INL error with user CAL coefficients. External voltage reference, Ta = 40 °C	-0.3	0.2	0.3	mV
VOLTAGE OUTPUT INITIAL ACCURACY WITH FACTORY CALIBRATION COEFFICIENTS						
Total unadjusted error		TUE [V/V] = (GEv+OE+INL)/FS				
Total unadjusted error	VTUE_Afc	Initial accuracy with factory calibration. Internal voltage reference, AO_TCC = 00\b. Ta = 40 °C.	—	0.0375	0.15	%FS
Total unadjusted error over temperature	VTUE_OTfc	Initial accuracy with factory calibration. Internal voltage reference, AO_TCC = 00\b. Ta = -25 °C to 105 °C	—	0.05	0.2	%FS
		Initial accuracy with factory calibration at 40 °C, Internal voltage reference, AO_TCC = 00\b. Ta = -40 °C to 125 °C	—	0.055	0.22	
Calibrated offset error	VOFF_Afc	Initial calibrated offset error with applied factory CAL coefficients. Internal reference, Ta = 40 °C	-0.2	0.05	0.2	mV
Calibrated gain error	VGE_Afc	Initial accuracy with factory calibration. Internal voltage reference, AO_TCC = 00\b. Ta = 40 °C.	—	0.035	0.14	%FS
	VGE_OTfc	Initial accuracy with factory calibration. Internal voltage reference, AO_TCC = 00\b. Ta = -25 °C to 105 °C	—	0.0475	0.19	
		Initial accuracy with factory calibration at 40 °C, Internal voltage reference, AO_TCC = 00\b. Ta = -40 °C to 125 °C	—	0.0525	0.21	
Calibrated INL error	VINL_Afc	Initial calibrated INL error with factory CAL coefficients. External voltage reference, Ta = 40 °C	-0.3	0.2	0.3	mV
VOLTAGE OUTPUT DRIFT OVER TEMPERATURE						
Total drift error	VTDE	VTDE [V/V] = (GEv+OE+INL)/FS/(DeltaTemperature)				

Table 51. Analog output electrical characteristics...*continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, typical values are at Ta = 40 ºC, DAC at 100 ksps, analog output (AO) is connected to an external 1 kΩ load resistor connected to ground. The parameters are characterized to their linear ranges, unless otherwise stated.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Total drift error	VTDE	Internal voltage reference, AO_TCC = 00\b. Ta = -25 °C to 105 °C.	—	2.5	10	ppm/ °C
		Internal voltage reference, AO_TCC = 00\b. Ta = -40 °C to 125 °C.	—	2.5	10	
Offset drift	VOFFd	Internal voltage reference, AO_TCC = 00\b. Ta = -40 °C to 125 °C.	-2	0.5	2	µV/°C
Gain drift	VGEd	Internal voltage reference, AO_TCC = 00\b. Ta = -40 °C to 125 °C.	-8	2	8	ppm/ °C
Gain drift	VGEd	External voltage reference, AO_TCC = 1x\b. Ta = -40 °C to 125 °C.	-2	0.5	2	ppm/ °C
Gain drift over time(2)	VGEd1khr	External voltage reference, AI_TCC = 1x\b. Ta = 125 °C.	—	50	—	ppm/ 1000h
		Internal voltage reference, AI_TCC = 00\b. Ta = 125 °C.	—	1000	—	ppm/ 1000h
INL drift	VINLd	External voltage reference, AO_TCC = 00\b. Ta = -40 °C to 125 °C.	-0.5	0.125	0.5	µV/°C
VOLTAGE OUTPUT						
Voltage headroom		HVDD-AOx	2	—	—	V
Voltage footroom		AOx-HVSS	2	—	—	V
Short-circuit current threshold		Detection time < 5 µs	—	±60	—	mA
Short-circuit current limiter		Programmable timer = 10 µs to 100 µs	±65	—	±80	mA
Overload-circuit current threshold		Detection time < 5 µs	±25	—	—	mA
Overload-circuit current threshold		Detection time < 5 µs (default)	±5	—	—	mA
Overload-circuit current limiter		Timer = 1 ms to 10 ms/ ∞. Programmable within the operating current range	-25	±5	25	mA
Load resistor		delta Vout criteria	1	100	—	kΩ
Capacitive load stability		RL = 1 MΩ with external compensation capacitor 15 pF. Settling time (HS 10 µs, 0.1 %)	—	—	20	nF
		RL = 1 kΩ with external compensation capacitor 15 pF. Settling time (HS 10 µs, 0.1 %)	—	—	20	nF
		RL = 1 kΩ with external compensation capacitor 100 pF. Settling time (HS 1 ms, 0.1 %)	—	—	2	µF
DC output impedance		Voltage output enabled, VOUT = ±10 V, IOUT = 0-20 10 mA	—	0.01	—	Ω
		Output disabled DIS1 (AOMODE = 0, VSA ON)	—	10	—	MΩ
		Voltage output disabled DIS2 (AOMODE = 0, VSA OFF and AIO connected to VSA)	—	150	—	kΩ
ILEAK		Voltage output disabled. High-Z	—	1	—	nA
DC PSRR_HV		Vout 0 V, HVDD/HVSS = ±7 V to ±24 V, AVDD = 3.3 V	—	10	—	µV/V
DC PSRR_LV		Vout 0 V, HVDD/HVSS = ±15 V, AVDD = 3 to 3.6 V	—	10	—	µV/V
Input impedance VSENSE		No Output load, VSA = ON, ±10 V	—	1000	—	MΩ
CURRENT OUTPUT RANGE						
Output current full-scale range	IOUT	±25.0 mA full range	—	±25.0	—	mA
Output current linear range	IOUT	±25.0 mA full range	-20	—	20	mA
CURRENT OUTPUT INITIAL ACCURACY WITHOUT CALIBRATION						
Total unadjusted error		ITUE [A/A] = (GEa+OE+INL)/FS				
Total unadjusted error at room temeperature	ITUE_Ai	Initial accuracy without CAL coefficients. Internal reference. AO_TCC = 01\b. External Rsense = 50 Ω. Ta = 40 °C.	—	0.5	1.00	%FS
Total unadjusted error over temperature	ITUE_OTi	Initial accuracy without CAL coefficients. Internal reference. AO_TCC= 01\b. External Rsense = 50 Ω. Ta = -25 °C to 105 °C.	—	0.6	1.10	%FS
Offset error	IOFF_Ai	Initial offset error without factory CAL coefficients. Internal reference, Ta = 25°C. External Rsense = 50 Ω.	-70	-30	10	µA
Gain error	IGE_Ai	Initial gain error without factory CAL coefficients. Internal reference, Ta = 25°C. External Rsense = 50 Ω	0.0	1.0	2.0	%FS
INL error	IINL_Ai	Initial INL error without factory CAL coefficients. External reference, Ta = 40 °C. AO_TCC = 01\b. External Rsense = 50 Ω.	-0.6	0.4	0.6	µA
CURRENT OUTPUT INITIAL ACCURACY WITH USER CALIBRATION COEFFICIENTS						
Total unadjusted error	ITUE	ITUE [A/A] = (GEa+OE+INL)/FS				
Total unadjusted error	ITUE_Auc	Initial accuracy with user calibration. AO_TCC = 01\b, External Rsense = 50 Ω. Ta = 40 °C.	—	0.0025	0.01	%FS

Table 51. Analog output electrical characteristics...*continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, typical values are at Ta = 40 ºC, DAC at 100 ksps, analog output (AO) is connected to an external 1 kΩ load resistor connected to ground. The parameters are characterized to their linear ranges, unless otherwise stated.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Total unadjusted error over temperature	ITUE_OTuc	Initial accuracy with user calibration, Internal voltage reference, AO_TCC = 01\b. External Rsense = 50 Ω. Ta = -25 °C to 105 °C.	—	0.02	0.08	%FS
		Initial accuracy with user calibration, Internal voltage reference, AO_TCC = 01\b. External Rsense = 50 Ω. Ta = -40 °C to 125 °C.	—	0.025	0.1	
Calibrated offset error	IOFF_Auc	Initial calibrated offset error with user CAL coefficients. Internal reference, external Rsense = 50 Ω. Ta = 40 °C.	-0.5	0	0.5	µA
Calibrated gain error	IGE_Auc	Initial calibrated gain error with user calibration coefficients. AO_TCC = 01\b, external Rsense = 50 Ω. Ta = 40 °C.	-0.0035	-0.0015	0.0005	%FS
	IGE_OTuc	Initial calibrated gain error with user calibration coefficients at 40 °C, Internal voltage reference, AO_TCC = 01\b. External Rsense = 50 Ω. Ta = -25 °C to 105 °C.	—	0.0175	0.07	
		Initial calibrated gain error with user calibration at 40 °C, Internal voltage reference, AO_TCC = 01\b. External Rsense = 50 Ω. Ta = -40 °C to 125 °C.	—	0.02	0.08	
INL error	IINL_Auc	Initial calibrated INL error with user CAL coefficients. External voltage reference, Ta = 40 °C. External Rsense = 50 Ω	-0.6	0.4	0.6	µA
CURRENT OUTPUT INITIAL ACCURACY WITH FACTORY CALIBRATION COEFFICIENTS						
Total unadjusted error	ITUE	ITUE [A/A] = (GEa+OE+INL)/FS				
Total unadjusted error	ITUE_Afc	Initial accuracy with factory calibration. Internal voltage reference, AO_TCC = 01\b, external Rsense = 50 Ω. Ta = 40 °C.	—	0.0375	0.15	%FS
Total unadjusted error over temperature	ITUE_OTfc	Initial accuracy with factory calibration, Internal voltage reference, AO_TCC = 01\b. External Rsense = 50 Ω. Ta = -25 °C to 105 °C.	—	0.05	0.2	%FS
		Initial accuracy with factory calibration, Internal voltage reference, AO_TCC = 01\b. External Rsense = 50 Ω. Ta = -40 °C to 125 °C.	—	0.055	0.22	
Calibrated offset error	IOFF_Afc	Initial calibrated offset error with factory CAL coefficients. Internal voltage reference, External Rsense = 50 Ω. Ta = 40 °C.	-1.75	0.15	1.75	µA
Calibrated gain error	IGE_Afc	Initial calibrated gain error with factory calibration coefficients. Internal voltage reference, AO_TCC=01\b, External Rsense = 50 Ω. Ta = 40 °C.	-0.14	0.035	0.14	%FS
	IGE_OTfc	Initial calibrated gain error with factory calibration coefficients at 40 °C, Internal voltage reference, AO_TCC = 01\b. External Rsense = 50 Ω. Ta = -25 °C to 105 °C.	-0.19	0.0475	0.19	
		Initial calibrated gain error with factory calibration at 40 °C, Internal voltage reference, AO_TCC = 01\b. External Rsense = 50 Ω. Ta = -40 °C to 125 °C.	-0.21	0.0525	0.21	
Calibrated INL error	IINL_Afc	Initial calibrated INL error with factory CAL coefficients. External voltage reference, AO_TCC = 11\b. External Rsense = 50 Ω. Ta = 40 °C.	-0.6	0.4	0.6	µA
CURRENT OUTPUT DRIFT OVER TEMPERATURE						
TUE drift		ITDE [A/A] = (GEa+OE+INL)/FS/DeltaTemp				
TUE drift	ITDE	Internal voltage reference, Ta = -25 °C to 105 °C. AO_TCC = 01\b. External Rsense = 50 Ω	—	2.5	10	ppm/ °C
		Internal voltage reference, Ta = -40 °C to 125 °C. AO_TCC = 01\b. External Rsense = 50 Ω	—	2.5	10	
Offset drift	IOFFd	Internal voltage reference, Ta = -40 °C to 125 °C. AO_TCC = 01\b. External Rsense = 50 Ω	-4	1	4	nA/°C
Gain drift	IGEd	Internal voltage reference, Ta = -40 °C to 125 °C. AO_TCC = 01\b. External Rsense = 50 Ω	-8	2	8	ppm/ °C
	IGEd	External voltage reference, Ta = -40 °C to 125 °C. AO_TCC = 02\b. External Rsense = 50 Ω	-2	0.5	2	ppm/ °C
INL drift	IINLd	External voltage reference, Ta = -40 °C to 125 °C. AO_TCC = 11\b. External Rsense = 50 Ω	-0.4	0.1	0.4	nA/°C
CURRENT OUTPUT						
Output voltage headroom		(HVDD-AOx), gain error < 0.1 % with 20 mA.	1.5	1.1	—	V
Output voltage footroom		(AOx-HVSS), gain error < 0.1 % with -20 mA.	1.5	1.1	—	V
Load resistor		±20 mA and HVDD and HVSS set to meet the voltage headroom and footroom.	0	—	750	Ω
Inductive load stability		RL = 1 MΩ with external compensation capacitor 15 pF. (HS settling time 20 µs, 0.1 %)	—	—	200	nH
		RL = 1 kΩ with external compensation capacitor 15 pF. (HS Settling time 20 µs, 0.1 %)	—	—	200	nH
		RL = 1 kΩ with external compensation capacitor 100 pF. (LP Settling time 100 µs, 0.1 %)	—	—	100	µH
DC output impedance		Current output enabled, Iout = 10 mA	—	30	—	MΩ
ILEAK		Output disabled	—	1	—	nA
DC PSRR_HV		Iout = 0 mA, HVDD/HVSS = ±7 V to ±24 V, AVDD = 3.3 V	—	0.1	—	µA/V

Table 51. Analog output electrical characteristics...*continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, typical values are at Ta = 40 ºC, DAC at 100 ksps, analog output (AO) is connected to an external 1 kΩ load resistor connected to ground. The parameters are characterized to their linear ranges, unless otherwise stated.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
DC PSRR_LV		Iout = 0 mA, HVDD/HVSS = ±15 V, AVDD = 3.0 to 3.6 V	—	0.1	—	µA/V
Input impedance ISENSE P, N		No output load, Common mode, Rext = 50 Ω	—	250	—	kΩ

10.2 Analog input

Table 52. Analog input electrical characteristics

All specifications are at VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal 2.5 V reference, ADC at 3 kSPS in Normal-settling mode with 500 samples averaging, each HV analog input (AIxP, AIxN, AICOM) is connected to an external 2.5 kΩ resistor in series with 1 nF capacitor connected to GND. The offset, gain and INL parametric are single-ended input-referred to the input pin and characterized to their nominal (linear) ranges, the minimum and maximum specifications cover Ta = -40 °C to 125 °C, typical specifications are at Ta = 40 ºC, unless otherwise specified.

Total unadjusted error = gain error + offset error + integral non-linearity

TUE = GE + OE + INL

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HV INPUT RANGES						
Voltage input full-scale range (single-ended)	VIN,SE	Single-ended input gain: GSE				
		PGA1: Channel gain = 16 V/V	—	±0.78	—	V
		PGA0: Channel gain = 1 V/V	—	±12.5	—	
		Vsense	—	±12.5	—	
Voltage input linear range (single-ended)	VIN,SE	Single-ended input gain: GSE	—	—	—	V
		PGA1: Channel gain = 16 V/V	-0.625	—	0.625	
		PGA0: Channel gain = 1 V/V	-10.0	—	10.0	
		Vsense	-10.0	—	10.0	
Voltage input full-scale range (differential)	VIN,DF	Differential input gain: GDF	—	—	—	V
		PGA1: Channel gain = 16 V/V	—	±1.56	—	
		PGA0: Channel gain = 1 V/V	—	±25	—	
Voltage input linear range (differential)	VIN,DF	Differential input gain: GDF	—	—	—	V
		PGA1: Channel gain = 16 V/V	-1.250	—	1.250	
		PGA0: Channel gain = 1 V/V	-20.0	—	20.0	
HIGH-VOLTAGE INPUT ACCURACY WITHOUT CALIBRATION COEFFICIENTS						
Total unadjusted error	TUE	TUE [V/V] = (GEv+OE+INL)/FS				
Total unadjusted error at room temperature	VTUE_Ai	Initial accuracy without CAL coefficients. Single-ended inputs. Internal voltage reference. AI_TCC = 00\b. Ta = 40 °C.	—	0.5	1.0	%FS
Total unadjusted error over temperature	VTUE_OTi	Initial accuracy without CAL coefficients. Single-ended inputs. Internal voltage reference. AI_TCC = 00\b. Ta = -25 °C to 105 °C	—	0.6	1.1	%FS
Offset error	VOE_Ai	Initial accuracy without factory CAL coefficients. Single-ended inputs. Internal voltage reference, AI_TCC = 00\b. Ta = 40 °C	—	—	—	
		Gdiff = 16 V/V	—	2	4	mV
		Gse = 1 V/V	—	20	40	mV
		Vsense	—	20	40	mV
Gain error	VGE_Ai	Initial accuracy without factory CAL coefficients. Internal voltage reference, AI_TCC = 00\b. Ta = 40 °C	—	—	—	
		Gdiff = 16 V/V	—	0.2	0.6	%FS
		Gse = 1 V/V	—	0.2	0.6	
		Vsense	—	0.2	0.6	
INL error	VINL_Ai	Single-ended inputs. External voltage reference, AI_TCC = 00\b. Ta = 40 °C	—	—	—	
		Gdiff = 16 V/V	—	10	50	µV
		Gse = 1 V/V	—	50	200	
		Vsense	—	50	200	
HV INPUT ACCURACY WITH USER CALIBRATION COEFFICIENTS(1)						
Total unadjusted error	VTUE	TUE [V/V] = (GEv+OE+INL)/FS				
Total unadjusted error at room	VTUE_Auc	Initial accuracy after user calibration. Ta = 40 °C. Internal voltage reference, AI_TCC = 00\b.	—	0.005	0.01	%FS

Table 52. Analog input electrical characteristics...*continued*

All specifications are at VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal 2.5 V reference, ADC at 3 kSPS in Normal-settling mode with 500 samples averaging, each HV analog input (AIxP, AIxN, AICOM) is connected to an external 2.5 kΩ resistor in series with 1 nF capacitor connected to GND. The offset, gain and INL parametric are single-ended input-referred to the input pin and characterized to their nominal (linear) ranges, the minimum and maximum specifications cover Ta = -40 °C to 125 °C, typical specifications are at Ta = 40 ºC, unless otherwise specified.

Total unadjusted error = gain error + offset error + integral non-linearity

TUE = GE + OE + INL

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Total unadjusted error over temperature	VTUE_OTuc	Initial accuracy after user calibration at Ta = -25 °C to 105 °C. Internal voltage reference, AI_TCC = 00\b.	—	0.02	0.08	%FS
	VTUE_OTuc	Initial accuracy after user calibration at Ta = -40 °C to 125 °C. Internal voltage reference, AI_TCC = 00\b.	—	0.05	0.1	%FS
Calibrated offset error	VOE_Auc	Initial offset error with user calibration. Single-ended inputs. Ta = 40 °C Internal voltage reference, AI_TCC = 00\b.				
		AI1P - AI1N, Gdiff = 16 V/V.	—	5	20	µV
		AI1P - VCM, AI1N - VCM, Gse = 1 V/V	—	50	200	
		Vsense	—	50	200	
Calibrated gain error	VGE_Auc	Initial gain error with user calibration coefficients, Single-ended inputs. Ta = 40 °C. Internal voltage reference, AI_TCC = 00\b.				
		AI1P - AI1N, Gdiff = 16 V/V.	—	0.0025	0.01	%FS
		AI1P - VCM, AI1N - VCM, Gse = 1 V/V	—	0.0025	0.01	
		Vsense	—	0.0025	0.01	
INL error	VINL_Auc	Initial offset error with user calibration. Single-ended inputs. Internal voltage reference, Ta = 40 °C External voltage reference, AI_TCC = 00\b.				
		AI1P - AI1N, Gdiff = 16 V/V.	—	10	50	µV
		AI1P - VCM, AI1N - VCM, Gse = 1 V/V	—	50	200	
		Vsense	—	50	200	
HV INPUT ACCURACY WITH FACTORY CALIBRATION COEFFICIENTS(1)						
Total unadjusted error	VTUE	TUE [V/V] = (GEv+OE+INL)/FS				
Total unadjusted error at room	VTUE_Afc	Initial accuracy with factory calibration. Ta = 40 °C. Internal voltage reference, AI_TCC = 00\b.	—	0.04	0.15	%FS
Total unadjusted error over temperature	VTUE_Otfc	Initial accuracy with factory calibration at Ta = -25 °C to 105 °C. Internal voltage reference, AI_TCC = 00\b.	—	0.1	0.22	%FS
	VTUE_OTfc	Initial accuracy with factory calibration at Ta = -40 °C to 125 °C. Internal voltage reference, AI_TCC = 00\b.	—	0.1	0.25	%FS
Calibrated offset error	VOE_Afc	Initial offset error with factory calibration. Single-ended inputs. Ta = 40 °C Internal voltage reference, AI_TCC = 00\b.				
		AI1P - AI1N, Gdiff = 16 V/V.	—	5	20	µV
		AI1P - VCM, AI1N - VCM, Gse = 1 V/V	—	50	200	
		Vsense	—	50	200	
Calibrated gain error	VGE_Afc	Initial gain error with factory calibration coefficients, Single-ended inputs. Ta = 40 °C. Internal voltage reference, AI_TCC = 00\b.				
		AI1P - AI1N, Gdiff = 16 V/V.	—	0.04	0.14	%FS
		AI1P - VCM, AI1N - VCM, Gse = 1 V/V	—	0.04	0.14	
		Vsense	—	0.04	0.14	
INL error	VINL_Afc	Initial INL error with factory calibration. Single-ended inputs. Internal voltage reference, Ta = 40 °C External voltage reference, AI_TCC = 00\b.				
		AI1P - AI1N, Gdiff = 16 V/V.	—	10	50	µV
		AI1P - VCM, AI1N - VCM, Gse = 1 V/V	—	50	200	
		Vsense	—	50	200	
VOLTAGE INPUT DRIFT						
TUE drift	VTDE	TUE [V/V] = (GEv+OE+INL)/FS/DeltaTemp				
TUE drift	VTDE	Temperature drift error. Single-ended inputs. Internal voltage reference, AI_TCC = 00\b. Ta = -25 °C to 105 °C.	—	3	10	ppm/ °C
		Temperature drift error. Single-ended inputs. Internal voltage reference, AI_TCC = 00\b. Ta = -40 °C to 125 °C.	—	3	10	ppm/ °C
Offset drift	VOFFD	Temperature drift error. Single-ended inputs. Internal voltage reference, AI_TCC = 00\b. Ta = -40 °C to 125 °C.	—	—	—	

Table 52. Analog input electrical characteristics...*continued*

All specifications are at VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal 2.5 V reference, ADC at 3 kSPS in Normal-settling mode with 500 samples averaging, each HV analog input (AIxP, AIxN, AICOM) is connected to an external 2.5 kΩ resistor in series with 1 nF capacitor connected to GND. The offset, gain and INL parametric are single-ended input-referred to the input pin and characterized to their nominal (linear) ranges, the minimum and maximum specifications cover Ta = -40 °C to 125 °C, typical specifications are at Ta = 40 ºC, unless otherwise specified.

Total unadjusted error = gain error + offset error + integral non-linearity

TUE = GE + OE + INL

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		AI1P - AI1N, Gdiff = 16 V/V.	—	0.2	0.5	µV/°C
		AI1P - VCM, AI1N - VCM, Gse = 1 V/V	—	2	5	
		Vsense	—	2	5	
Gain drift over temperature	VGD	Temperature drift, Single-ended inputs. Ta = -40 °C to 125 °C.				
		AI1P, AI1N, G = 1 and 16 V/V. External voltage reference, AI_TCC = 1x\b.	—	1	2	ppm/ °C
		AI1P, AI1N, G = 1 and 16 V/V. Internal voltage reference, AI_TCC = 00\b.	—	4	8	
		Vsense. External voltage reference, AI_TCC = 1x\b.	—	1	2	
		Vsense. Internal voltage reference, AI_TCC = 00\b.	—	4	8	
Gain drift over time(2)	VGD1khr	AI1P-VCM, AI1N-VCM, Gse = 1 V/V AI1P-AI1N and Gdiff = 16 V/V. External voltage reference, AI_TCC = 1x\b. Ta = 125 °C.	—	50	—	ppm/ 1000h
		AI1P-VCM, AI1N-VCM, Gse = 1 V/V AI1P-AI1N and Gdiff = 16 V/V. Internal voltage reference, AI_TCC = 00\b. Ta = 125 °C.	—	1000	—	ppm/ 1000h
INL drift	VINLD	INL drift error with factory calibration. External voltage reference, AI_TCC = 00\b. Ta = -40 °C to 125 °C.				
		AI1P - AI1N, Gdiff = 16 V/V.	—	0.03	0.1	µV/°C
		AI1P - VCM, AI1N - VCM, Gse = 1 V/V	—	0.3	1	
		Vsense	—	0.3	1	
HV INPUT CHARACTERISTICS						
HV IO DC crosstalk		HV IO victim = 0 V with HV IO adjacent aggressor at ±Full Scale, Ta = 40 °C	—	1	10	µV/V
HV IO dynamic crosstalk		VAIxP = 10 V swtich to VAIyN = -10 V, SCS, Data rate = 12 ksps, CH_DELAY = 16.4 µs. Ta = 40 °C.	—	1	10	µV/V
Channel switch time	Tswitch	VIN changes from one input to another input, ADC output code settles within 0.01 % of final value. ADC is in Single-Cycle Settling mode, 12 kSPS, SINC4 filter	—	<16.4	—	µS
Input voltage noise	Vnoise	Inputs shorted to GND	—	—	—	µVrms
		ADC in Normal Settling mode versus data rate and channel gain		Noise Table		
		ADC in Normal Settling mode, 1.125KSPS, G = 1 V/V	—	16.4	—	
High-voltage headroom		VHVDD above positive input linear range of 10 V	3.8	—	—	V
		VHVSS below negative input linear range of -10 V	3.8	—	—	
Common mode rejection ratio	CMRRDC	Shorted differential inputs pair. VCM = -1 V to 1 V DC. DRO = 1.125 ksps	—	—	—	dB
		GDIFF = 16 V/V	—	104	—	
		GDIFF=1 V/V	—	80	—	
Common mode rejection ratio	CMRR50/60	Shorted differential inputs pair. VCM = -1 V to 1 V 50 Hz/60 Hz. DRO = 10 sps, SINC4+SINC4 filter	—	—	—	dB
		GDIFF = 16 V/V	—	184	—	
		GDIFF = 1 V/V	—	160	—	
Power supply rejection ratio (RTI)	PSRRHV	Shorted differential DC inputs at 0 V, VHVDD = 7 V to 24 V, VHVSS = -24 V to -7 V	—	—	—	dB
		GDIFF = 16 V/V	130	136	—	
		GDIFF=1 V/V	106	112	—	
	PSRRLV	Shorted differential DC Inputs at 0 V, VAVDD = VDVDD = 3 V to 3.6 V	—	—	—	
		GDIFF = 16 V/V	80	90	—	
		GDIFF=1 V/V	58	66	—	
Input impedance	RIN	AI1P, AI1N, G = 1 and G = 16. Ta = 40 °C	—	1000	—	MΩ
Input leakage current	IL	AI1P, AI1N and Vsense pins. Ta = -25 °C to 105 °C	—	1	5	nA
		AI1P, AI1N and Vsense pins., Ta = -40 °C to 125 °C	—	1	15	
CURRENT INPUT RANGE - I_SENSE						
Current input full-scale range	IOUT	±25.0 mA full-range, External Rsense = 50.	—	±25	—	mA
Current input linear range	IOUT	±20.0 mA linear-range, External Rsense = 50.	-20	—	20	mA

Table 52. Analog input electrical characteristics...*continued*

All specifications are at VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal 2.5 V reference, ADC at 3 kSPS in Normal-settling mode with 500 samples averaging, each HV analog input (AIxP, AIxN, AICOM) is connected to an external 2.5 kΩ resistor in series with 1 nF capacitor connected to GND. The offset, gain and INL parametric are single-ended input-referred to the input pin and characterized to their nominal (linear) ranges, the minimum and maximum specifications cover Ta = -40 °C to 125 °C, typical specifications are at Ta = 40 ºC, unless otherwise specified.

Total unadjusted error = gain error + offset error + integral non-linearity

TUE = GE + OE + INL

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT INPUT ACCURACY WITHOUT CALIBRATION COEFFICIENTS - I_SENSE						
Total unadjusted error	TUE	TUE [A/A] = (GEa+OE+INL)/FS				
Total unadjusted error at room temperature	TUE_Ai	Isense. Initial accuracy without CAL coefficients. Internal voltage reference. External 50 Ω sense resistor connected to GND via CISW. AI_TCC = 01\b. Ta = 40 °C.	—	0.5	1.0	%FS
Total unadjusted error over temperature	TUE_OTi	Isense. Initial accuracy without CAL coefficients. Internal voltage reference. External 50 Ω sense resistor connected to GND via CISW. AI_TCC = 01\b. Ta = -25 °C to 105 °C	—	0.6	1.1	%FS
Offset error	OEi	Isense. Initial accuracy without CAL coefficients. Internal voltage reference. External 50 Ω sense resistor connected to GND via CISW. AI_TCC = 01\b. Ta = 40 °C.	—	0.4	0.8	mA
Gain error	GEi	Isense. Initial accuracy without CAL coefficients. Internal voltage reference. External 50 Ω sense resistor connected to GND via CISW. AI_TCC = 01\b. Ta = 40 °C.	—	0.3	0.8	%FS
INL error	INL	Isense. Initial accuracy without CAL coefficients. External voltage reference. External 50 Ω sense resistor connected to GND via CISW. AI_TCC = 01\b. Ta = 40 °C.	—	0.2	0.5	µA
CURRENT INPUT ACCURACY WITH USER CALIBRATION COEFFICIENTS(1) - I-SENSE						
Total unadjusted error	TUE	TUE [A/A] = (GEa+OE+INL)/FS				
Total unadjusted error at room	TUE_ATC	Isense. Initial accuracy with user calibration coefficients, Ta = 40 °C. Internal voltage reference, 50 Ω sense resistor connected to GND via CISW. AI_TCC = 01\b.	—	0.005	0.01	%FS
Total unadjusted error over temperature	TUE_OTC	Isense. Initial accuracy with user calibration coefficients, Ta = -25 °C to 105 °C. Internal voltage reference, external Rsense = 50 Ω, AI_TCC = AI_TCC = 0.1\b.	—	0.05	0.1	%FS
Calibrated offset error	OEC	Isense. Initial gain error with user calibration coefficients, Ta = 40 °C. Internal voltage reference. External 50 Ω sense resistor connected to GND via CISW. AI_TCC = 01\b	—	2	5	µA
Calibrated gain error		Isense. Initial gain error with user calibration coefficients, Ta = 40 °C. Internal voltage reference, external 50 Ω sense resistor connected to GND via CISW. AI_TCC = 01\b	—	0.005	0.01	%FS
INL error		Isense. Initial gain error with user calibration coefficients, Ta = 40 °C. external voltage reference, external 50 Ω sense resistor connected to GND via CISW. AI_TCC = 01\b	—	0.2	0.5	µA
CURRENT INPUT ACCURACY WITH FACTORY CALIBRATION COEFFICIENTS(1) - I_SENSE						
Total unadjusted error	TUE	TUE [A/A] = (GEa+OE+INL)/FS				
Total unadjusted error at room	TUE_ATC	Isense. Initial accuracy with factory calibration coefficients, Ta = 40 °C. Internal voltage reference, 50 Ω sense resistor connected to GND via CISW. AI_TCC = 01\b.	—	0.04	0.15	%FS
Total unadjusted error over temperature	TUE_OTC	Isense. Initial accuracy with factory calibration coefficients, Ta = -25 °C to 105 °C. Internal voltage reference, external Rsense = 50 Ω, AI_TCC = AI_TCC = 0.1\b.	—	0.1	0.22	%FS
Calibrated offset error	OEC	Isense. Initial gain error with factory calibration coefficients, Ta = 40 °C. Internal voltage reference, external 50 Ω sense resistor connected to GND via CISW. AI_TCC = 01\b	—	2	5	µA
Calibrated gain error		Isense. Initial gain error with factory calibration coefficients, Ta = 40 °C. Internal voltage reference, external 50 Ω sense resistor connected to GND via CISW. AI_TCC = 01\b	—	0.04	0.14	%FS
INL error		Isense. Initial gain error with factory calibration coefficients, Ta = 40 °C. external voltage reference, external 50 Ω sense resistor connected to GND via CISW. AI_TCC = 01\b	—	0.2	0.5	µA
CURRENT DRIFT COEFFICIENTS - I_SENSE						
TUE drift	TDE	TUE [A/A] = (GEa+OE+INL)/FS/DeltaTemp				
TUE drift	TDE	Isense. External Rsense = 50 Ω connected to GDN via CISW. Ta = -25 °C to 105 °C. Internal voltage reference, AI_TCC = 01\b.	—	3	10	ppm/ °C
		Isense. External Rsense = 50 Ω connected to GDN via CISW. Ta = -40 °C to 125 °C. Internal voltage reference, AI_TCC = 01\b.	—	3	10	ppm/ °C
Offset drift	OD	Isense. External Rsense = 50 Ω connected to GDN via CISW. Ta = -40 °C to 125 °C. Internal voltage reference, AI_TCC = 01\b.	—	0.04	0.1	µA/°C
Gain drift over temperature	GD	Isense. External Rsense = 50 Ω connected to GDN via CISW. Ta = -40 °C to 125 °C. External reference, AI_TCC = 1x\b.	—	1	2	ppm/ °C
		Isense. External Rsense = 50 Ω connected to GDN via CISW. Ta = -40 °C to 125 °C. Internal voltage reference, AI_TCC = 01\b.	—	3	8	ppm/ °C
Gain drift over time(2)	GD1khr	Isense. External Rsense = 50 Ω connected to GDN via CISW. Ta = 125 °C. External reference, AI_TCC = 1x\b.	—	50	—	ppm over 1000h

Table 52. Analog input electrical characteristics*...continued*

All specifications are at VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal 2.5 V reference, ADC at 3 kSPS in Normal-settling mode with 500 samples averaging, each HV analog input (AIxP, AIxN, AICOM) is connected to an external 2.5 kΩ resistor in series with 1 nF capacitor connected to GND. The offset, gain and INL parametric are single-ended input-referred to the input pin and characterized to their nominal (linear) ranges, the minimum and maximum specifications cover Ta = -40 °C to 125 °C, typical specifications are at Ta = 40 ºC, unless otherwise specified.

Total unadjusted error = gain error + offset error + integral non-linearity

TUE = GE + OE + INL

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		Isense. External Rsense = 50 Ω connected to GDN via CISW. Ta = 125 °C. Internal voltage reference, AI_TCC = 01\b.	—	1000	—	ppm over 1000h
INL drift	INLD	Isense. External Rsense = 50 Ω connected to GDN via CISW. Ta = -40 °C to 125 °C. External voltage reference, AI_TCC = 01\b.	—	0.002	0.004	µA/°C
CISW						
ON resistance over temperature	OVT_RON	Ta = -40 °C to 125 °C. I = ±22 mA.	180	200	220	Ω
ON resistance linear error	LED_RON	Ta = -40 °C to 125 °C. I = ±22 mA.	—	0.3	—	Ω/ mA/C
ON resistance non-linear error	NLE_RON	Ta = -40 °C to 125 °C. I = ±22 mA.	—	2	—	Ω
OFF input leakage current	IL	CISW = 10 V. Ta = -25 °C to 105 °C	—	1	5	nA
		CISW = 10 V. Ta = -40 °C to 125 °C	—	1	15	
LV_MUX INPUTS						
LV measurement accuracy						
HVDD-GND	HVDD	—	—	2	—	%FS
HVSS-GND	HVSS	—	—	2	—	%FS
DVDD-GND	DVDD	—	—	2	—	%FS
LDO-GND	LDO	—	—	2	—	%FS
VREF1-GND	VREF1	—	—	2	—	%FS
VREF2-GND	VREF2	—	—	2	—	%FS
VCM-VCM	VCM	0 V through ADC readback.	—	30	—	µV
GPIO0 (ADCP), GPIO1 (ADCN) AS ANALOG INPUT						
Analog input signal range	GPIO0, GPIO1	Input range w.r.t the GND.	0.5	—	VREF	V
SINGLE-ENDED SIGNAL: ADCP-VCM, VCM-ADCN						
Offset error	OESE	Without calibration coefficients, single-ended input	—	2.5	—	mV
		With factory calibration coefficients, single-ended input	—	10	—	µV
		Precision mode (LV_input chop), single-ended input	—	2	—	µV
Gain error	GESE	Without calibration coefficients, single-ended input	—	6000	—	ppm
		With factory calibration coefficients, single-ended input	—	20	—	ppm
DIFFERENTIAL SIGNAL: ADCP-ADCN						
Offset error	OEDIFF	Without calibration coefficients, differential input	—	2.5	—	mV
		With factory calibration coefficients, differential input	—	10	—	µV
		Precision mode (LV_input chop), differential input	—	2	—	µV
Gain error	GEDIFF	Without calibration coefficients, differential input	—	6000	—	ppm
		With factory calibration coefficients, differential input	—	20	—	ppm

10.3 Common system

Table 53. Common system EC table

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, typical values are at Ta = 40 ºC, DAC at 100 ksps, analog output (AO) is connected to an external 1 kΩ load resistor connected to ground. The parameters are characterized to their linear ranges, unless otherwise stated.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TEMPERATURE SENSOR						
Temperature sensor resolution		Die temperature	—	1/64	—	°C
Temperature sensor accuracy		Die temperature	—	±3	—	°C
INTERNAL VOLTAGE REFERENCE						
Output voltage	VREF	Internal reference, REF_INT		2.496		V
Initial accuracy		Ta = 40 °C with internal reference	-0.5		0.5	%
Temperature coefficient	TCVREF	Ta = -25 °C to 105 °C	—	±4	±10	ppm/°C
		Ta = -40 °C to 125 °C	—	±6	±15	
Long-term stability(2)	LTS		—	1000	—	ppm over 1000h
Load regulation		0.1 mA sourcing and sinking current load	—	1	—	mV/mA
Supply regulation	SVREF	3 V ≤ VAVDD ≤ 3.6 V, Ta = 40 °C	—	10	—	µV/V
DACREFBUF						
Load regulation		0.5 mA sourcing and sinking current load	—	10	—	µV/mA
Supply regulation	SVREF	3V ≤ VAVDD ≤ 3.6 V, Ta = 40 °C	—	10	—	µV/V
ADCREFBUF						
Load regulation		0.5 mA sourcing and sinking current load	—	10	—	µV/mA
Supply regulation	SVREF	3 V ≤ VAVDD ≤ 3.6 V, Ta = 40 °C	—	10	—	µV/V
POWER SUPPLIES						
High-voltage supply	VHV	VHVDD - VHVSS	14	—	48	V
Positive high-voltage supply	VHVDD	Referenced to AGND	7	15	32	V
Negative high-voltage supply	VHVSS	Referenced to AGND	-32	-15	-7	V
Low-supply voltage	VVDD	VDD = VAVDD = VDVDD. Referenced to AGND	2.97	3.30	3.63	V
Low-voltage supply quiescent current	IVDD	AI off (PGA OFF, all LV buffer, ADC all off), Current output mode 0 mA (PA_ON = 1, VSA_ON = 1, CSA_ON = 1, CISW_ON = 0) VSENSE_pin = 0 V, HVDD = -HVSS = 15 V, AVDD = DVDD = 3.3 V, all other settings are POR default.	—	7.4	8.1	mA
High-voltage quiescent current	IHVDD		—	2.4	2.6	mA
High-voltage quiescent current	IHVSS		—	2.3	2.5	mA
Total quiescent power			—	95	104	mW
Low-voltage supply quiescent current	IVDD	AI partial on (PGA OFF, all LV buffer, ADC all on), Current output mode 0 mA (PA_ON = 1, VSA_ON = 1, CSA_ON = 1, CISW_ON = 0), VSENSE_pin = 0 V, HVDD = -HVSS = 15 V, AVDD = DVDD = 3.3 V, all other settings are POR default. (LP OPTION)	—	14.5	16.7	mA
High-voltage quiescent current	IHVDD		—	2.7	3.0	mA
High-voltage quiescent current	IHVSS		—	2.3	2.5	mA
Total quiescent power			—	123	138	mW
Low-voltage supply quiescent current	IVDD	AI on (PGA, all LV buffer, ADC all on), Current output mode 0 mA (PA_ON = 1, VSA_ON = 1, CSA_ON = 1, CISW_ON = 0), VSENSE_pin = 0 V, HVDD = -HVSS = 15 V, AVDD = DVDD = 3.3 V, all other settings are POR default.	—	14.5	16.7	mA
High-voltage quiescent current	IHVDD		—	3.9	4.3	mA
High-voltage quiescent current	IHVSS		—	3.5	3.9	mA
Total quiescent power			—	158	178	mW
DIGITAL I/Os						
Logic HIGH input voltage	VIH		0.7*VDVDD	—	—	V
Logic LOW input voltage	VIL		—	—	0.3*VDVDD	V
Input voltage hysteresis			—	0.3	—	V
Logic HIGH output voltage	VOH	IOH = 3 mA	0.8*VDVDD	—	—	V
Logic LOW output voltage	VOL	IOL = -3 mA	—	—	0.2*VDVDD	V
OSCILLATORS						
Clock frequency accuracy		Internal oscillator -40 °C to 125 °C	—	0.2	1.1	%
Clock frequency Accuracy		Internal oscillator -25 °C to 105 °C	—	0.2	0.9	%
Input clock duty cycle		External clock applied to OSCIN pin. Frequency = 18.432 MHz	45	50	55	%

Table 53. Common system EC table...*continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, typical values are at Ta = 40 ºC, DAC at 100 ksps, analog output (AO) is connected to an external 1 kΩ load resistor connected to ground. The parameters are characterized to their linear ranges, unless otherwise stated.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator input startup time	SUT OSCIN	18.432 MHz	—	50	—	µS

10.4 SPI timing specification

Table 54. SPI timing specification

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, typical values are at Ta = 40 ºC, unless otherwise stated.

PARAMETER	SYMBOL	CONDITIONS	Min	Typ	Max	Units
SERIAL INTERFACE						
SCLK frequency	f_{SCLK}	—	—	8	32	MHz
SCLK high-pulse width	t_{SCLK_H}	—	14.5	—	—	ns
SCLK low-pulse width	t_{SCLK_L}	—	14.5	—	—	ns
MOSI setup time	t_{IS}	Time to SCLK falling edge	5	—	—	ns
MOSI hold time	t_{IH}	Time after SCLK falling edge	5	—	—	ns
MISO transition time	t_{OT}	Time after SCLK rising edge	—	10.5	15	nA
CSB high pulse width	t_{CWH}	CSB high pulse width	32	—	—	ns
CSB falling setup time	t_{CFS}	Time before SCLK first rising edge	5	—	25	ns
CSB rising setup time	t_{CRS}	Time before SCLK rising edge	5	—	25	ns
DAC conversion wait time	t_{DAC_WAIT}	Required delay wait time from last falling edge of SCLK to the rising edge of CSB pin when SYNDAC_EN = 0; Required delay wait time from last falling edge of SCLK to the rising edge of SYNDAC pin when SYNDAC_EN = 1;	18	—	—	# of sys clock
SYNCDAC pulse width	$t_{SYNCDAC\_PW}$	SYNCDAC signal pulse width with SYNCDAC_EN = 1	2	—	—	# of sys clock

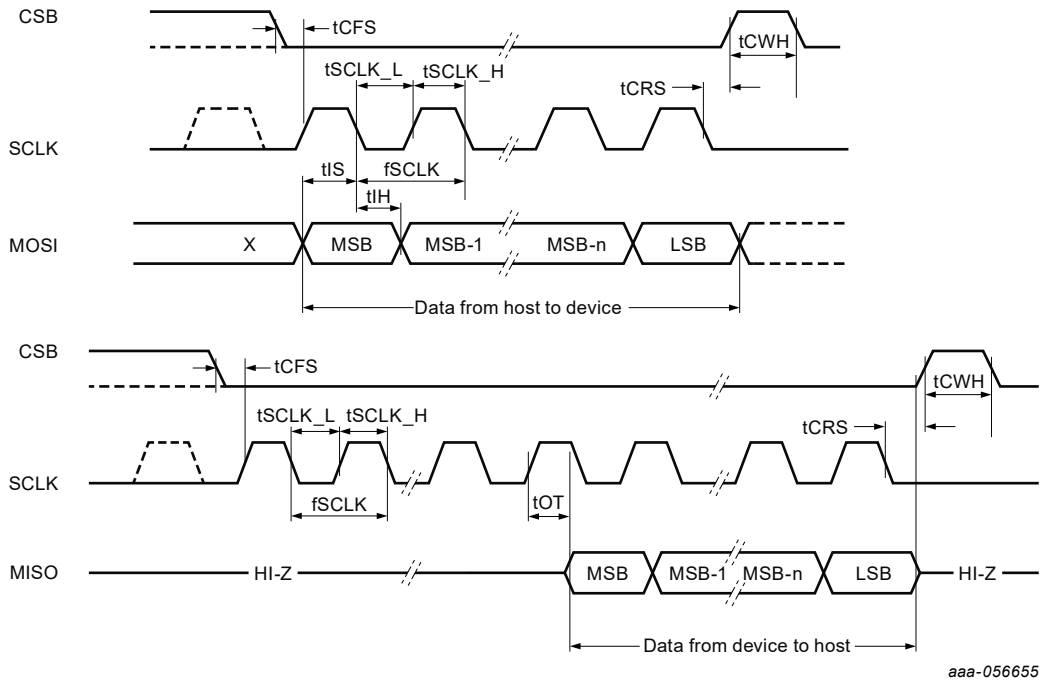


Figure 48. SPI timing

Table 55. Internal LDO output for digital core

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
LDO regulation	—	2.97 V < VDVDD < 3.63 V, 1 µF bypass cap	—	15	—	mV/V

Table 56. CISW internal resistor

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
On-resistance initial error	IE_RON	Ta = -40 °C. I = 2 mA	—	200	—	Ω
On-resistance over temp	OVT_RON	Ta = -25 °C to 105 °C. I = ±22 mA.	185	—	215	Ω
On-resistance over temp	OVT_RON	Ta = -40 °C to 125°C. I = ±22 mA.	180	—	220	Ω
On-resistance linear error	LE_RON	Ta = 40 °C. I = ±22 mA.	—	0.3	—	Ω/mA
On-resistance non-linear error	NLE_RON	Ta = 40 °C. I = ±22 mA.	—	±2	—	Ω
On-resistance linear error	LED_RON	Ta = -40 °C to 125 °C. I = ±22 mA.	—	0.2	TBD	Ω/mA/C
On-resistance non-linear error	NLED_ RON	Ta = -40 °C to = 125 °C. I = ±22 mA.	—	±0.02	TBD	Ω/C
Over current threshold - low to high	—	—	—	35	—	mA
Over current threshold - high to low	—	—	—	30	—	—
Current limiter settling	—	—	—	20	—	mA
Current limiter settling time	—	—	—	30	—	µS
Iq CISW	—	—	—	10	—	µA

Table 57. Reliability stress

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Post-stress VREF voltage drift	HAST	with PreCon, 130 ºC/85 % RH up to 384 hours with higher power supplies	-0.75	—	0.75	%
	TMCL	-65 ºC to 150 ºC temperature cycle at 500 and 1000 cycles read points	-0.75	—	0.75	%
	HTOL	125 ºC with highest supply voltages (±26 V, 3.63 V) up to 2000 hrs	-0.75	—	0.75	%
	PreCon	Bake: 125 ºC/24 hr, Soak: 30 ºC/60 % RH/192 hr, Reflow: 260 ºC/3 cyc	-0.75	—	0.75	%
	HTSL	175 ºC up to 600 hours	-0.75	—	0.75	%
Post-stress gain error drift	HAST	with PreCon, 130 ºC/85 % RH up to 384 hours with higher power supplies	-0.75	—	0.75	%
	TMCL	-65 ºC to 150 ºC temperature cycle at 500 and 1000 cycles readpoints	-0.75	—	0.75	%
	HTOL	125 ºC with highest supply voltages (±26 V, 3.63 V) up to 2000 hrs	-0.75	—	0.75	%
	PreCon	Bake: 125 ºC/24 hr, Soak: 30 ºC/60 %RH/192 hr, Reflow: 260 ºC/3 cyc	-0.75	—	0.75	%
	HTSL	175 ºC up to 600 hours	-0.75	—	0.75	%

11 Application information

11.1 AIO Voltage Output mode

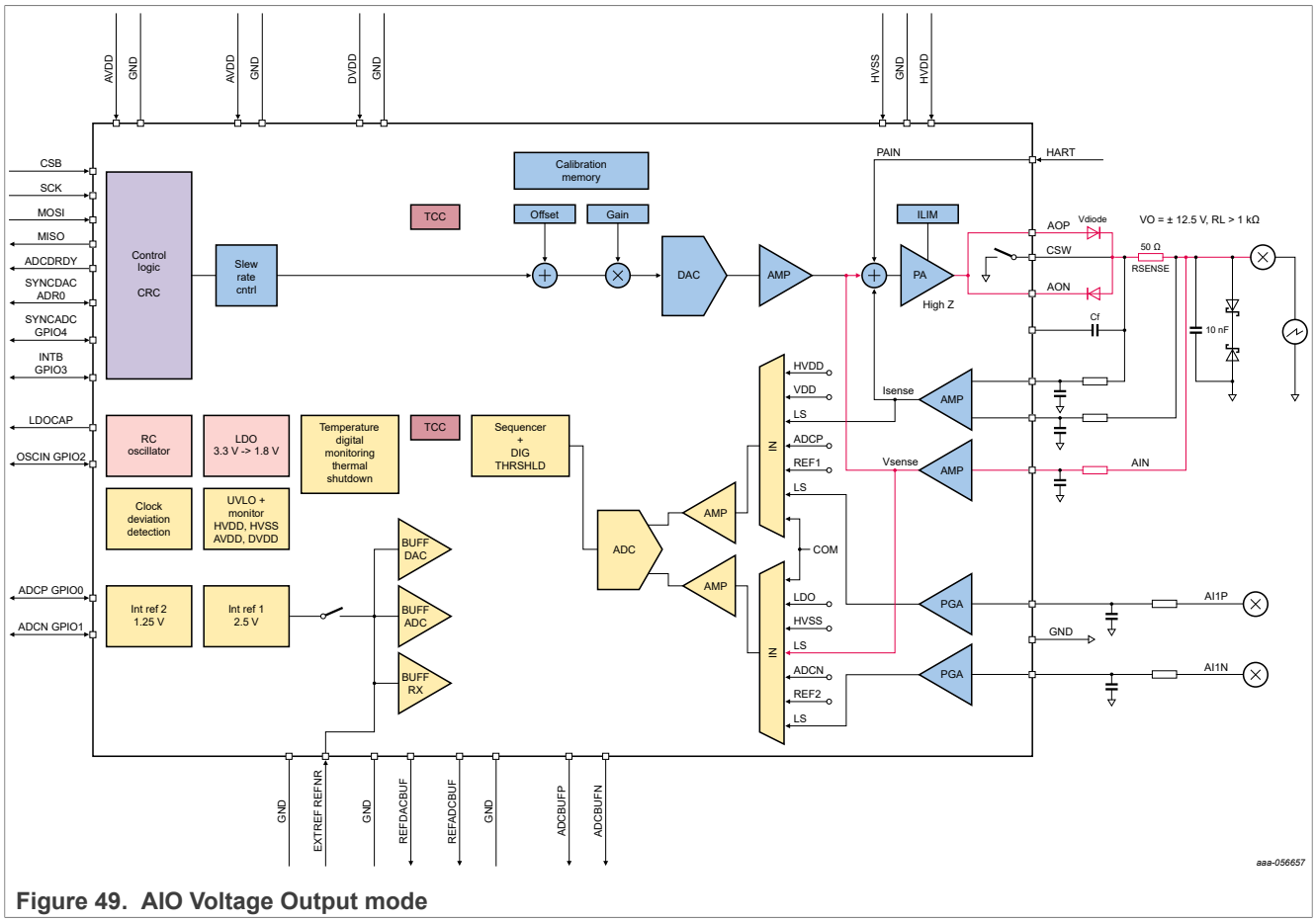


Figure 49. AIO Voltage Output mode

11.1.1 Output compliance voltage

The maximum output voltage is defined in Table 51.

The maximum allowable output compliance voltage can be calculated as below:

$$Voutmax = HVDD - HEADROOM - Vdiode - I*RSENSE$$

$$Voutmin = HVSS + HEADROOM + Vdiode + I*RSENSE$$

And V_{REF} = 2.5 V with internal reference voltage.

11.2 AIO Current Output mode

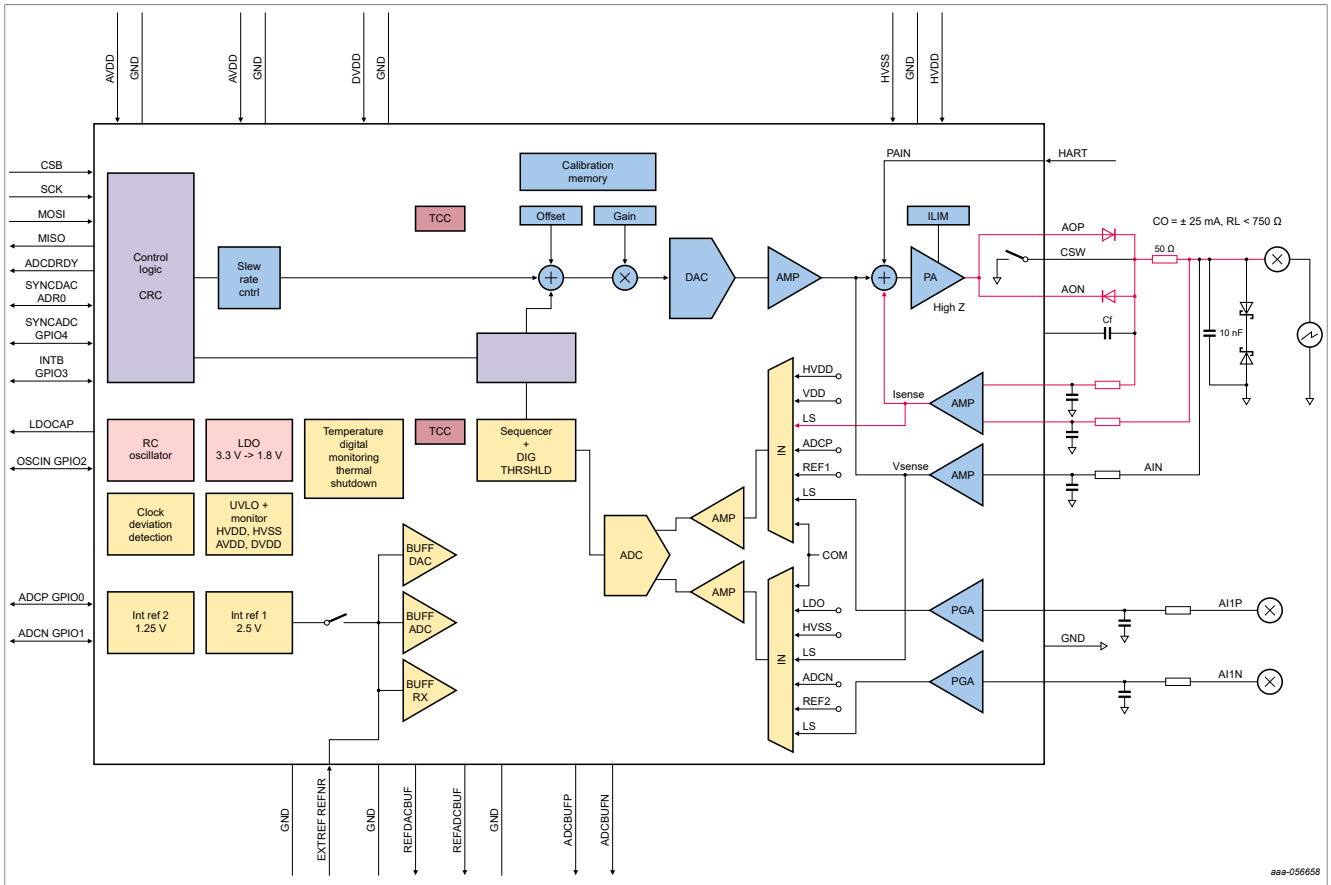


Figure 50. AIO Current Output mode

11.3 AIO Voltage Input mode

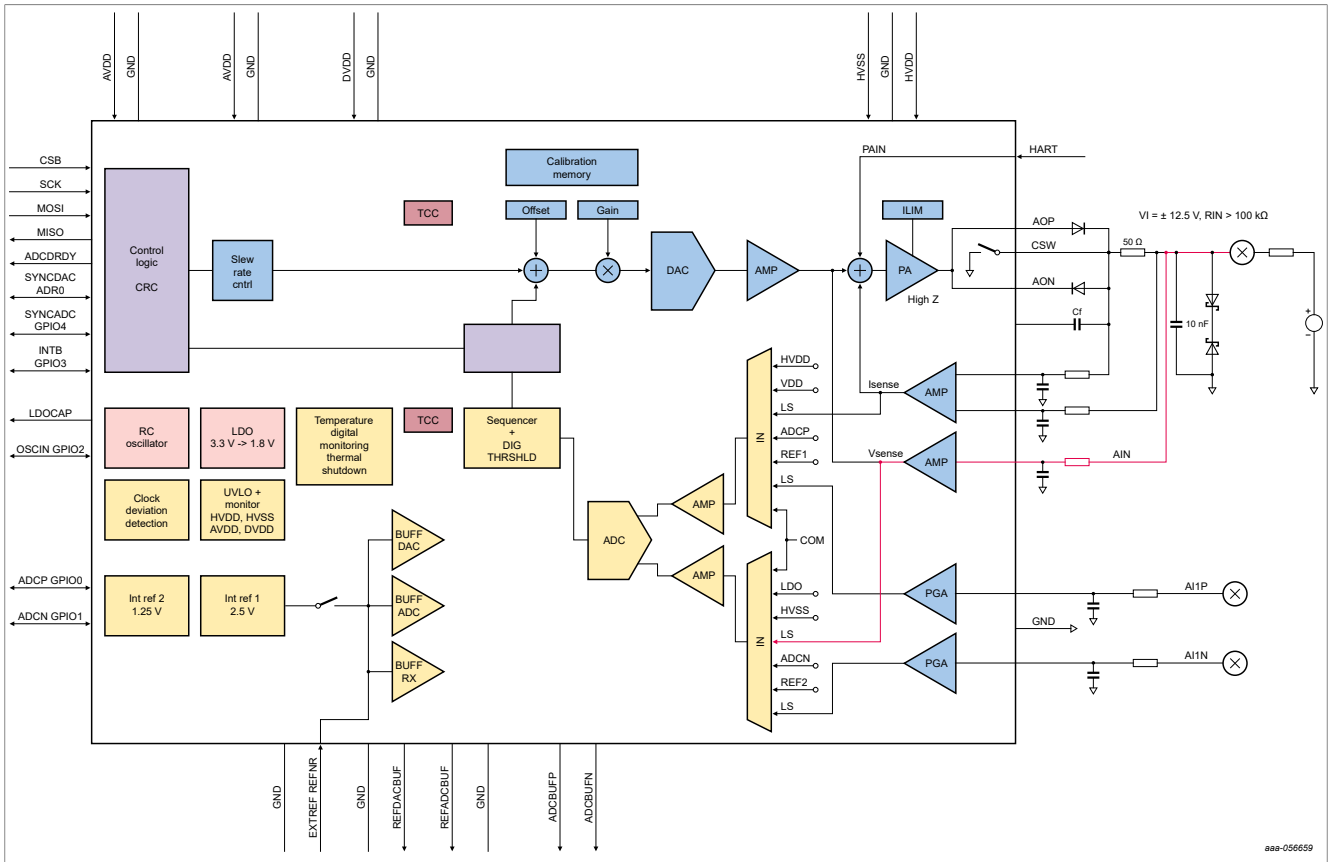


Figure 51. AIO Current Input mode

11.4 AIO Current Input mode

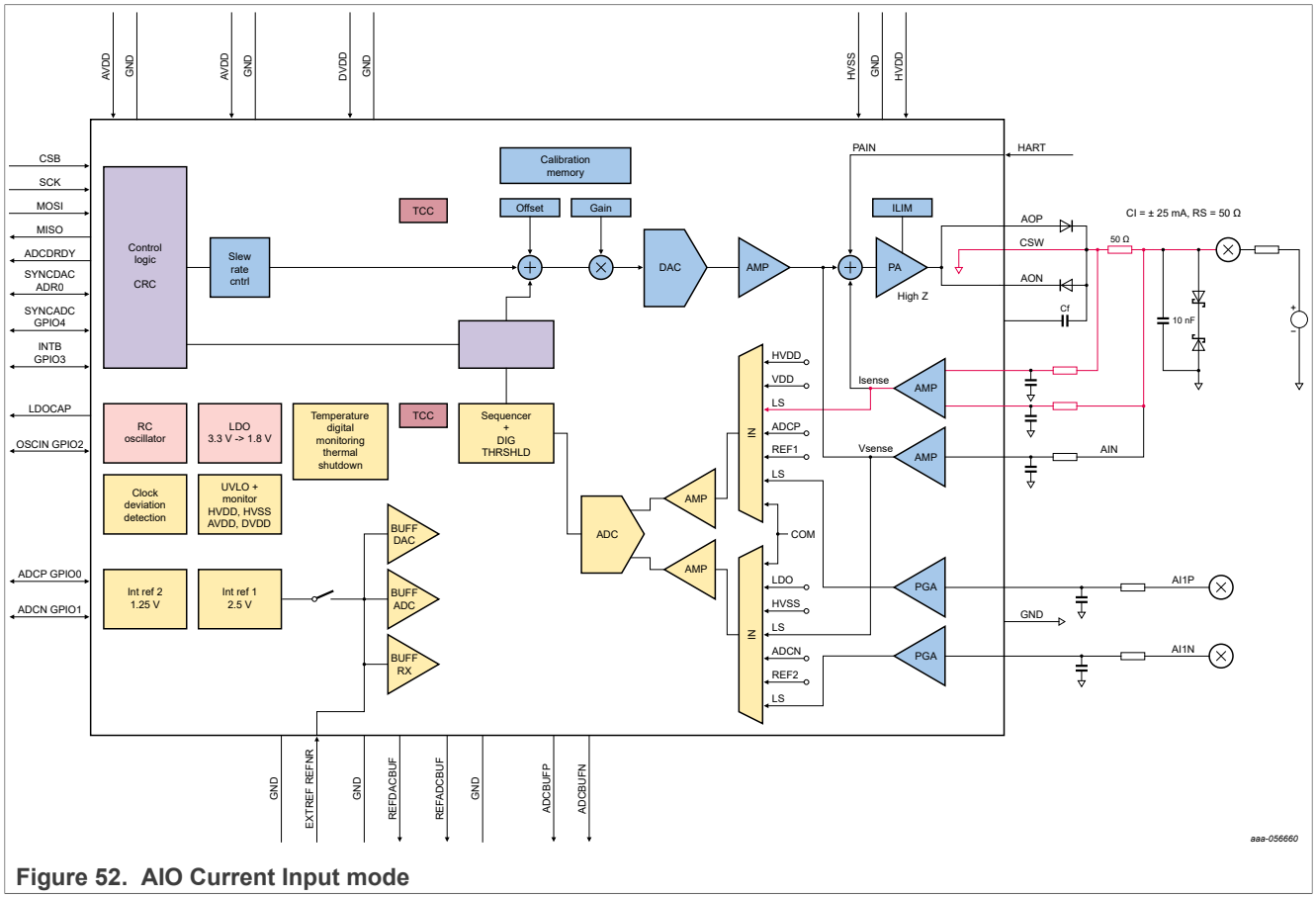


Figure 52. AIO Current Input mode

11.5 Universal analog input/output + TC and RTD capability block diagram

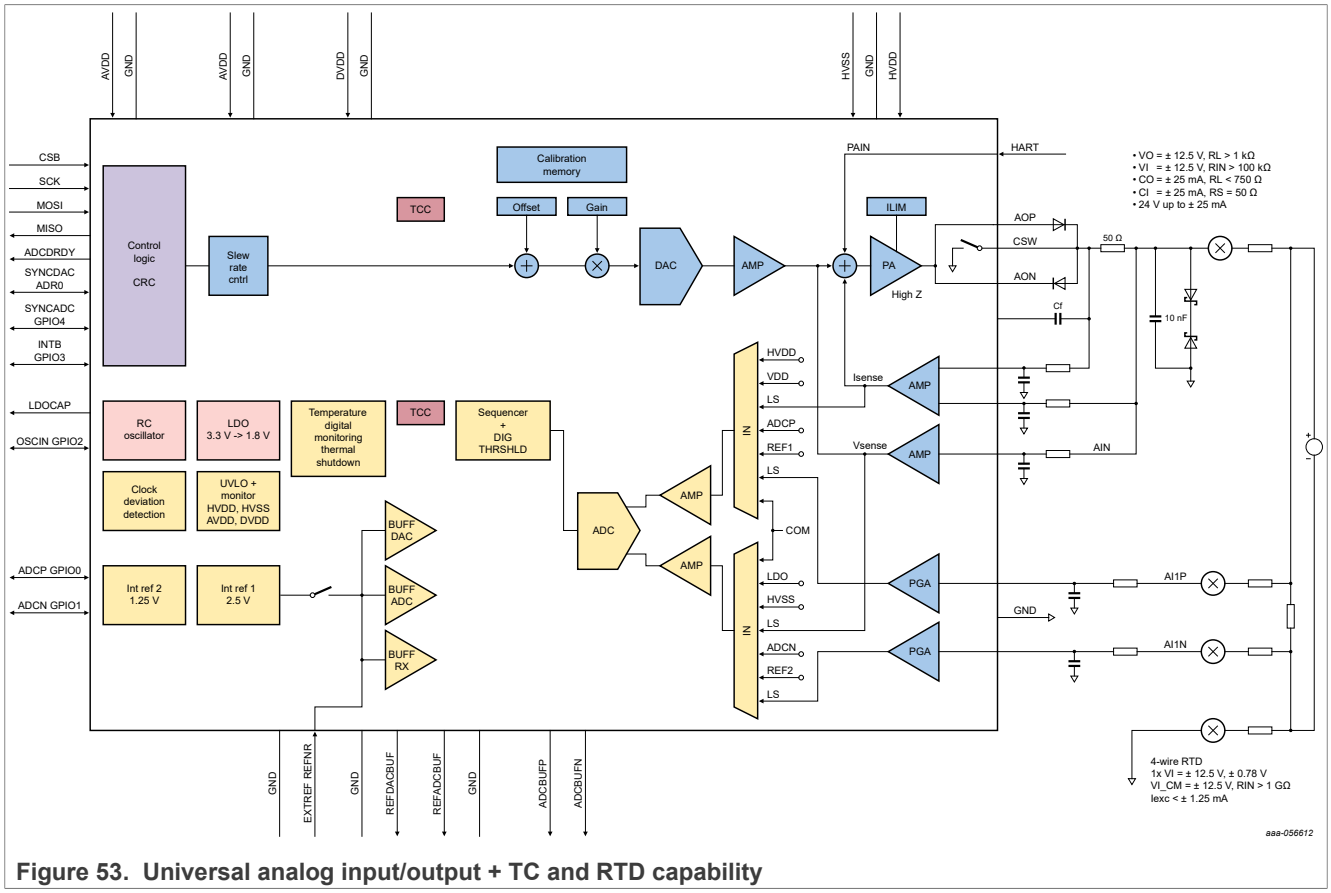


Figure 53. Universal analog input/output + TC and RTD capability

11.6 Universal analog input/output + universal analog input (combo solution) block diagram

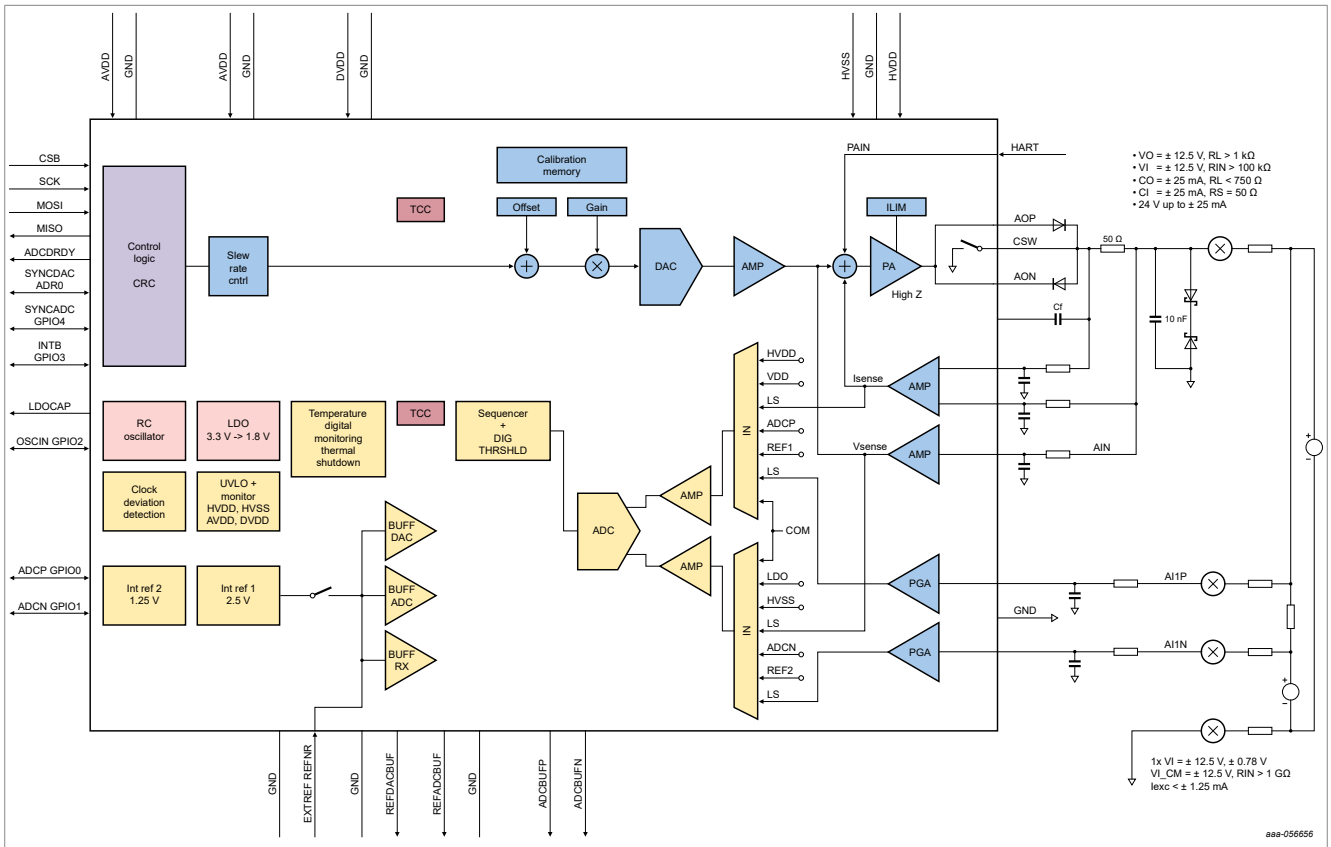


Figure 54. Universal analog input/output + universal analog input (combo solution)

12 Typical operating characteristics

Typical operating characteristics

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal 2.5 V reference, Ta = 40 °C, unless otherwise specified.

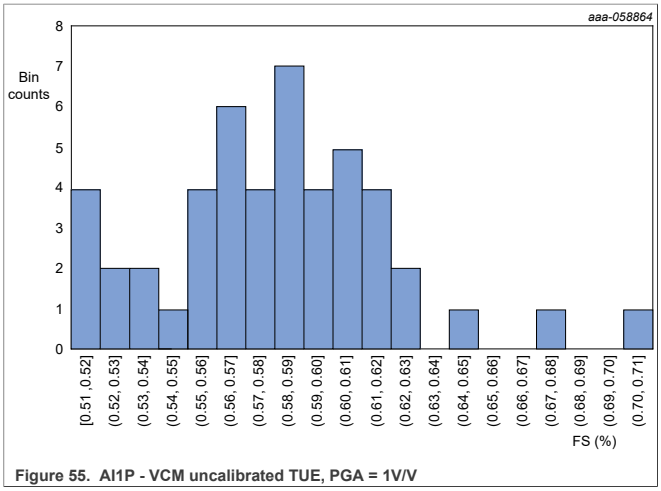


Figure 55. AI1P - VCM uncalibrated TUE, PGA = 1V/V

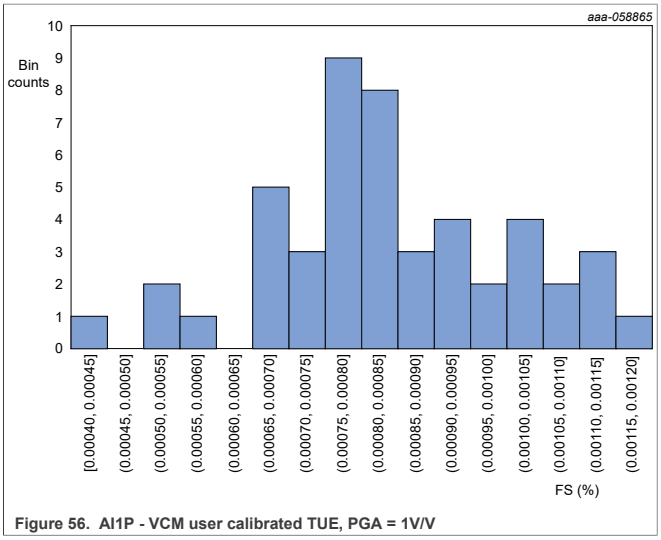


Figure 56. AI1P - VCM user calibrated TUE, PGA = 1V/V

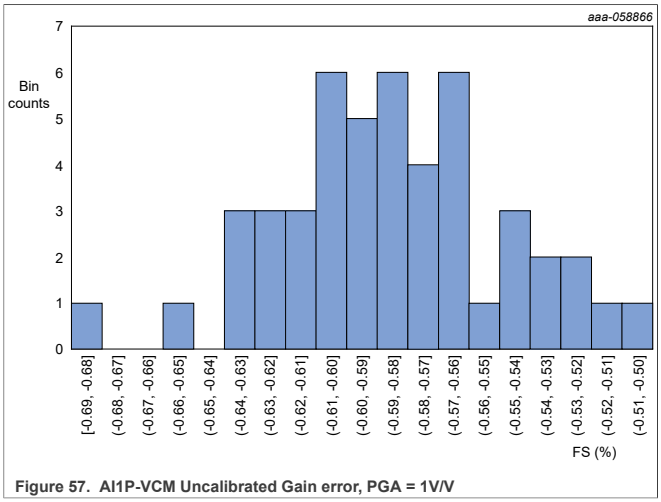


Figure 57. AI1P-VCM Uncalibrated Gain error, PGA = 1V/V

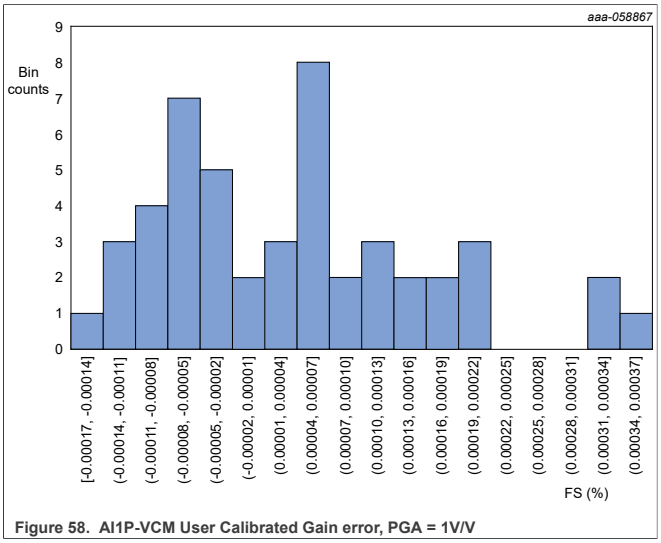


Figure 58. AI1P-VCM User Calibrated Gain error, PGA = 1V/V

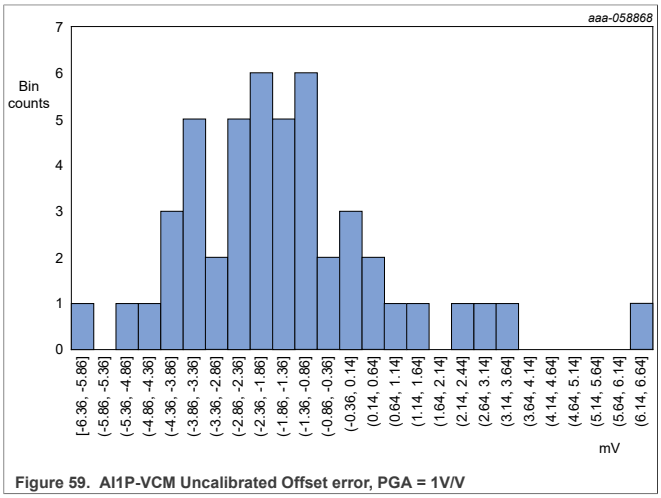


Figure 59. AI1P-VCM Uncalibrated Offset error, PGA = 1V/V

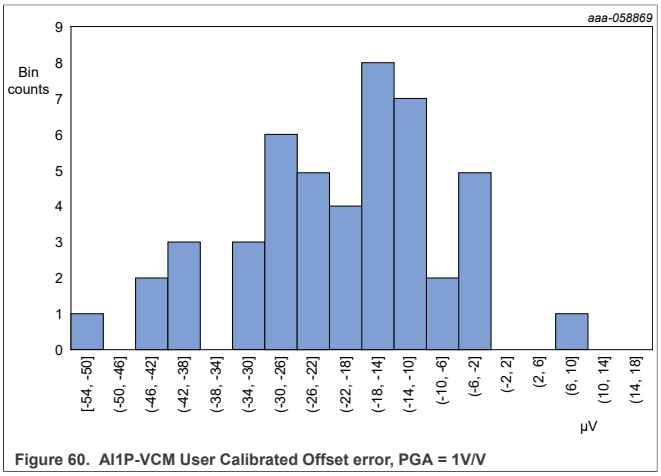


Figure 60. AI1P-VCM User Calibrated Offset error, PGA = 1V/V

Typical operating characteristics...*continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal 2.5 V reference, Ta = 40 °C, unless otherwise specified.

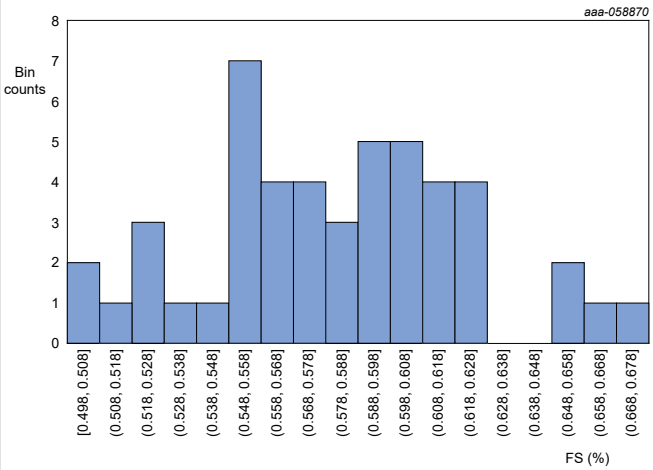


Figure 61. AI1N-VCM Uncalibrated TUE, PGA = 1V/V

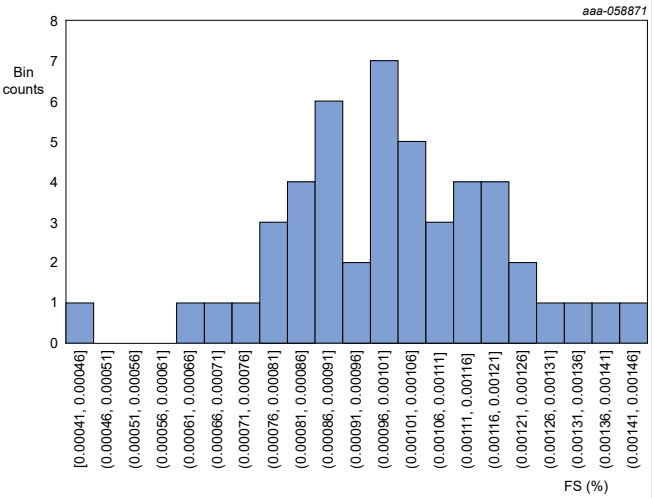


Figure 62. AI1N-VCM User Calibrated TUE, PGA = 1V/V

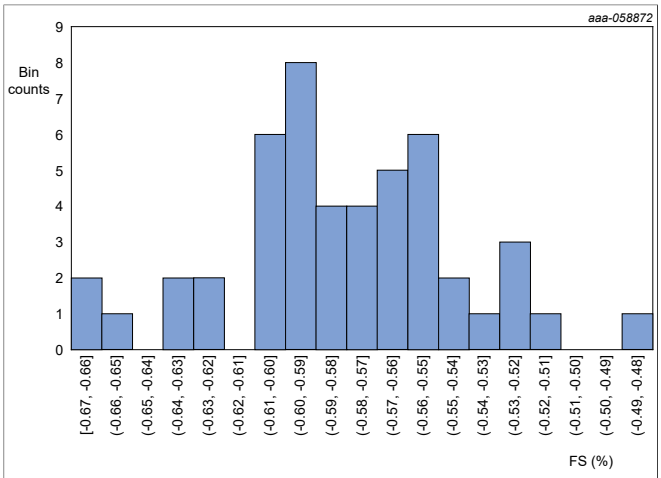


Figure 63. AI1N-VCM uncalibrated gain error, PGA = 1V/V

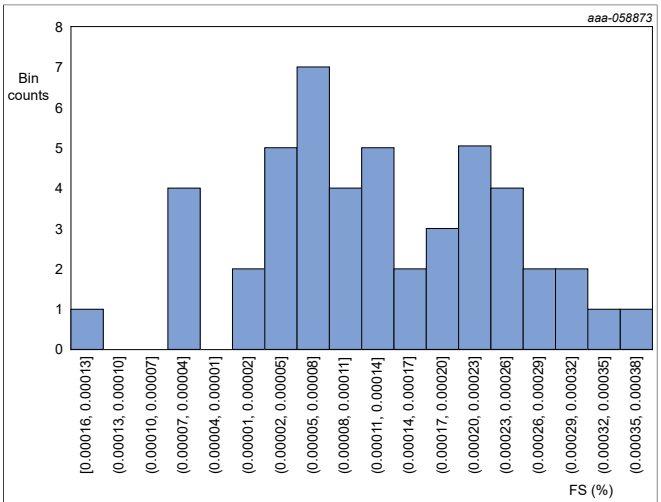


Figure 64. AI1N-VCM user calibrated gain error, PGA = 1V/V

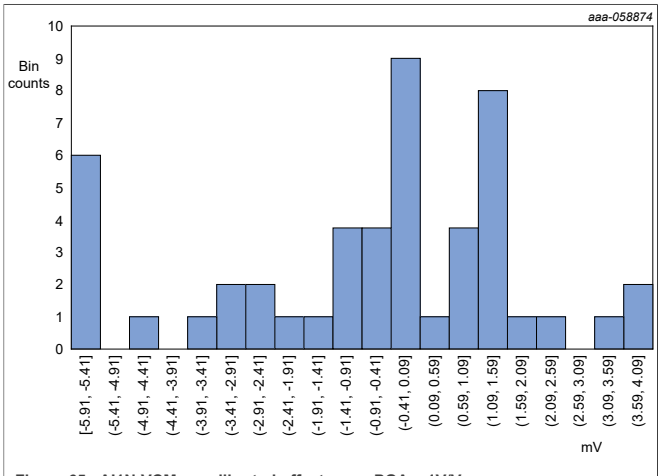


Figure 65. AI1N-VCM uncalibrated offset error, PGA = 1V/V

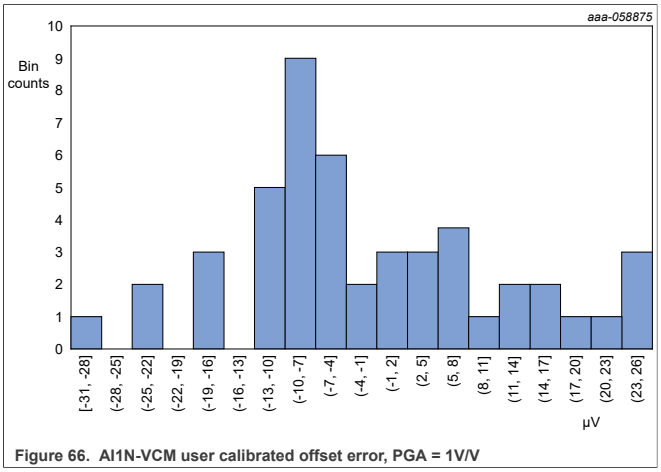


Figure 66. AI1N-VCM user calibrated offset error, PGA = 1V/V

Typical operating characteristics...*continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal 2.5 V reference, Ta = 40 °C, unless otherwise specified.

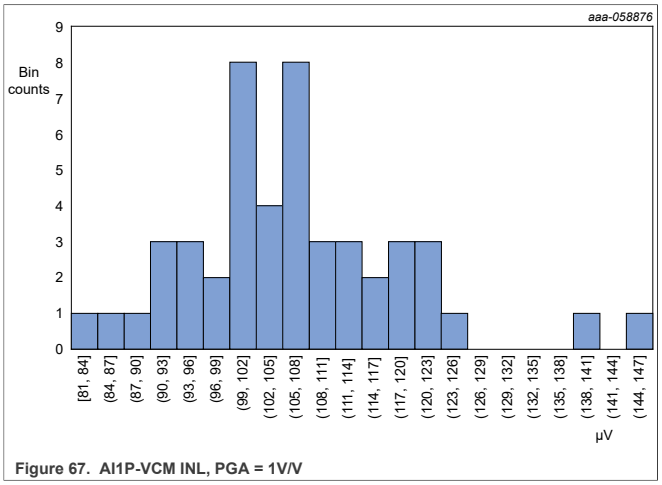


Figure 67. AI1P-VCM INL, PGA = 1V/V

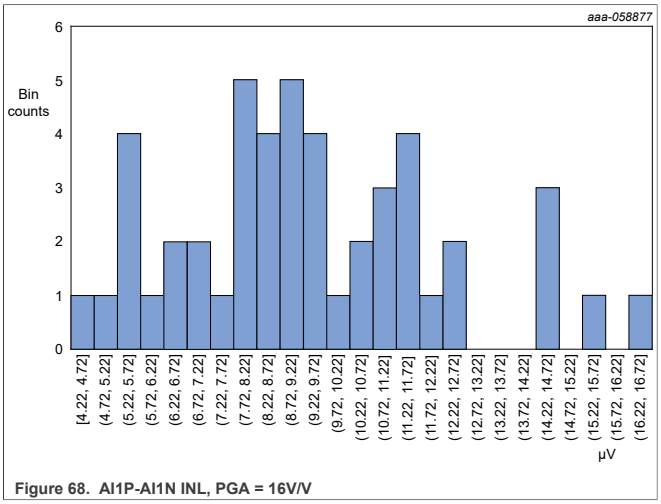


Figure 68. AI1P-AI1N INL, PGA = 16V/V

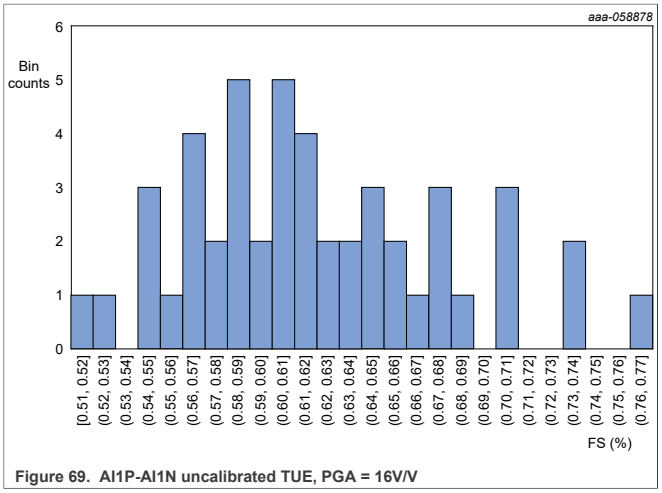


Figure 69. AI1P-AI1N uncalibrated TUE, PGA = 16V/V

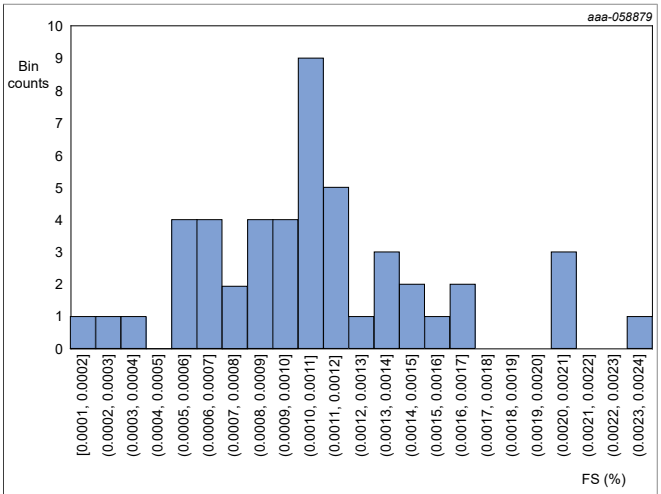


Figure 70. AI1P-AI1N user calibrated TUE, PGA = 16V/V

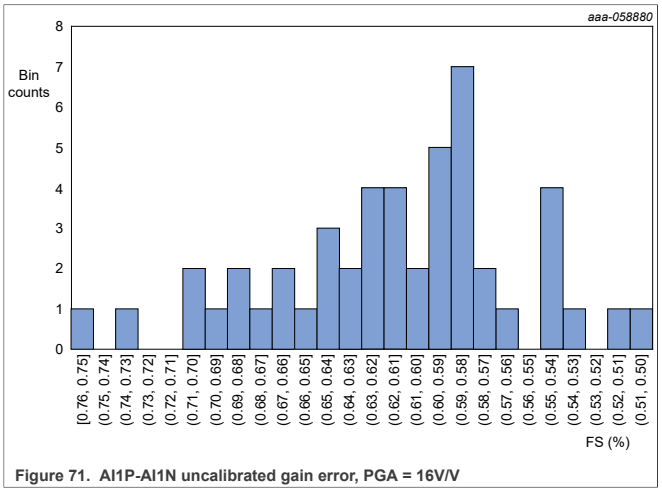


Figure 71. AI1P-AI1N uncalibrated gain error, PGA = 16V/V

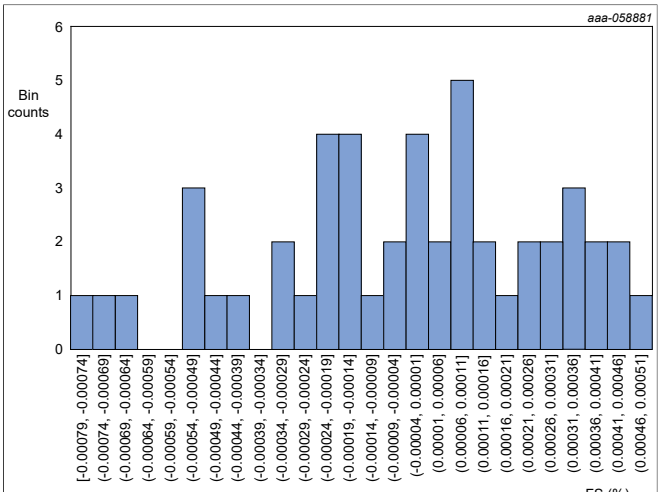


Figure 72. AI1P-AI1N user calibrated gain error, PGA = 16V/V

Typical operating characteristics...*continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal 2.5 V reference, Ta = 40 °C, unless otherwise specified.

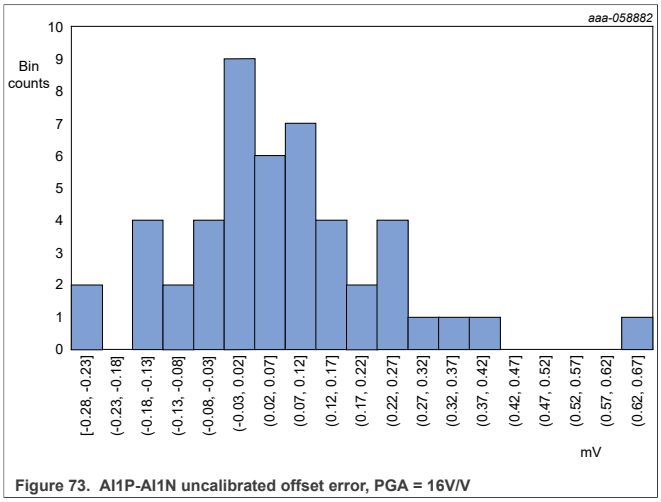


Figure 73. AI1P-AI1N uncalibrated offset error, PGA = 16V/V

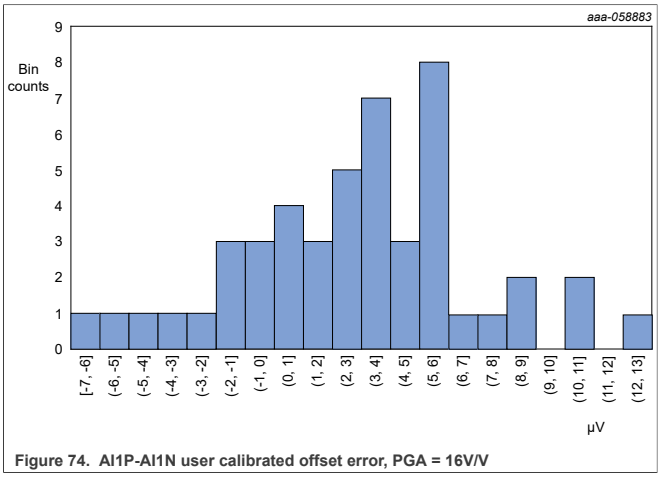


Figure 74. AI1P-AI1N user calibrated offset error, PGA = 16V/V

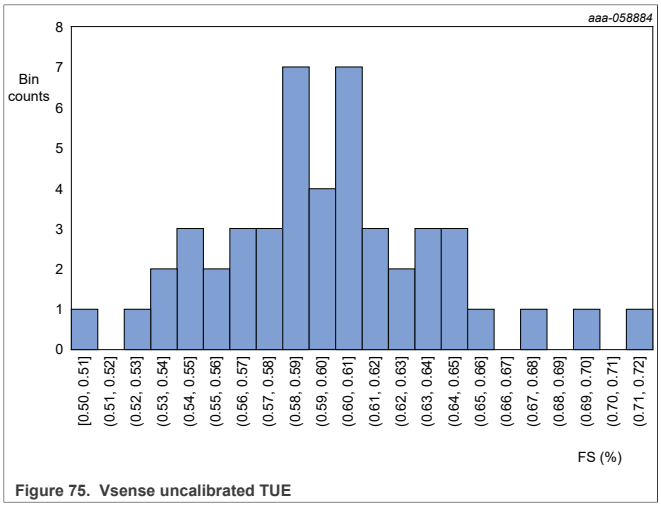


Figure 75. Vsense uncalibrated TUE

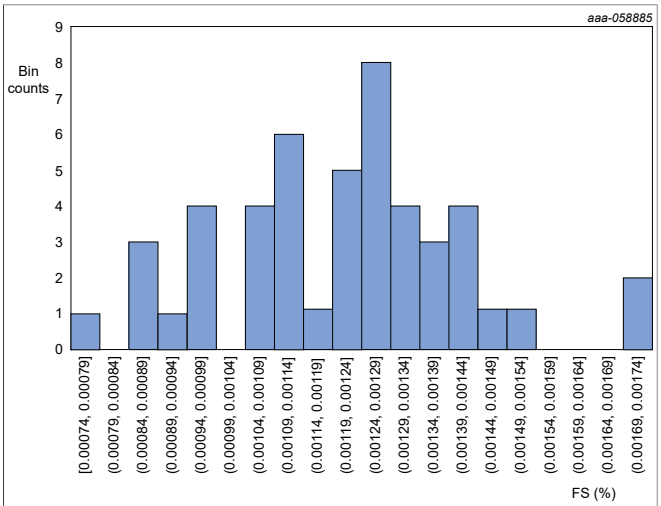


Figure 76. Vsense user calibrated TUE

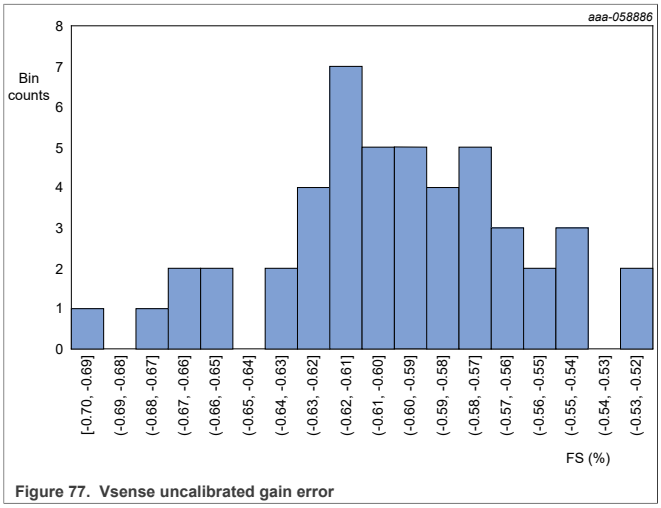


Figure 77. Vsense uncalibrated gain error

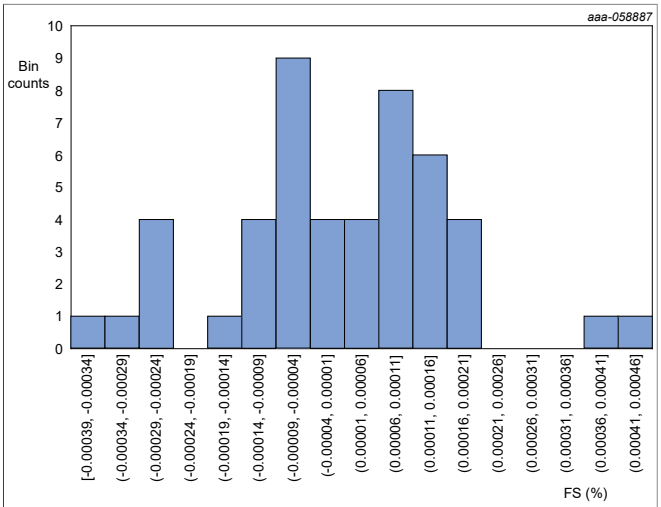


Figure 78. Vsense user calibrated gain error

Typical operating characteristics...*continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal 2.5 V reference, Ta = 40 °C, unless otherwise specified.

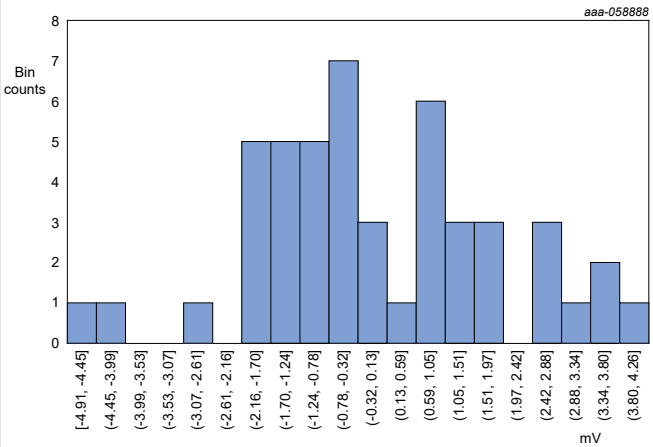


Figure 79. Vsense uncalibrated offset error

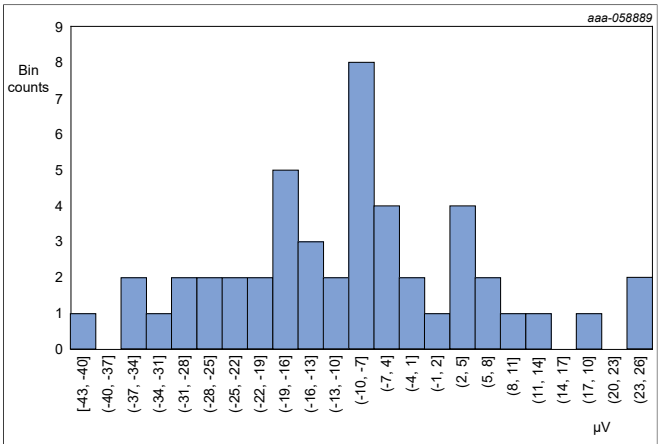


Figure 80. Vsense User calibrated offset error

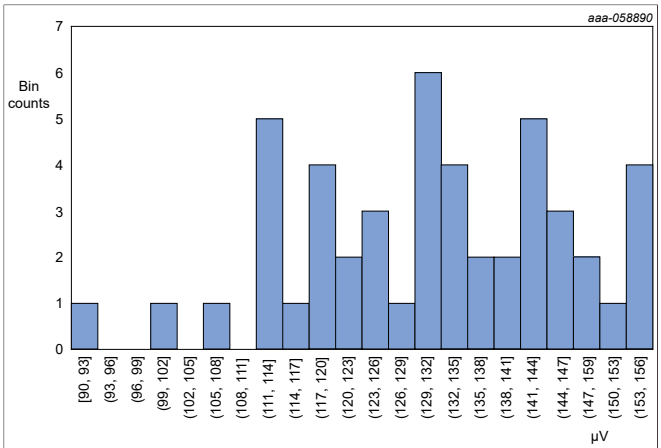


Figure 81. Vsense INL

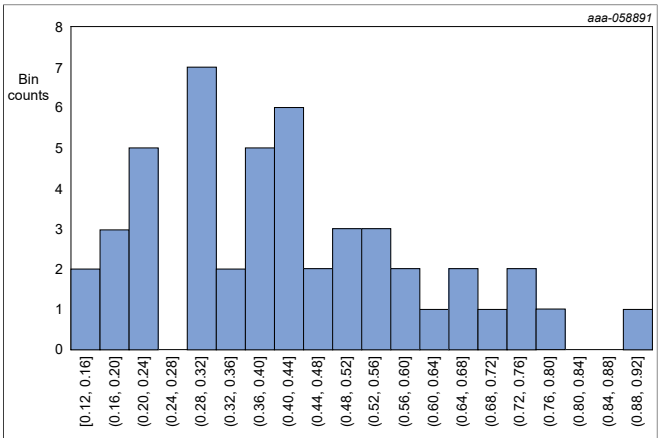


Figure 82. Isense INL

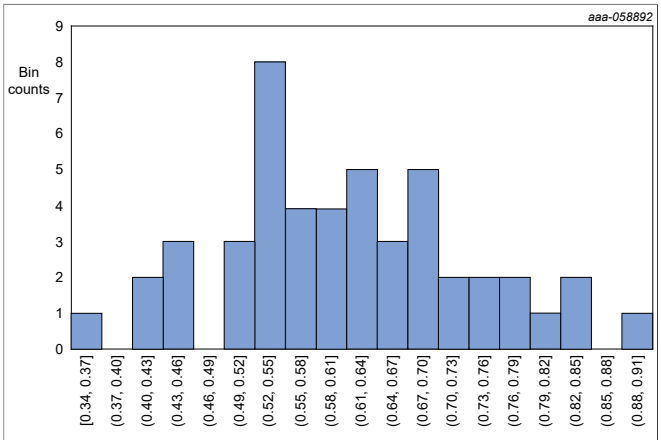


Figure 83. Isense uncalibrated TUE

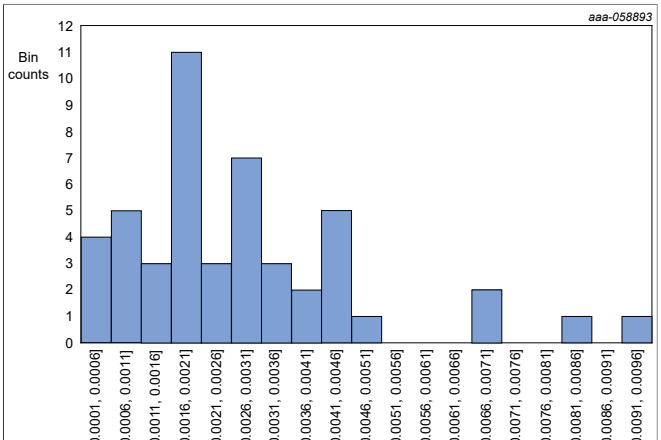


Figure 84. Isense user calibrated TUE

Typical operating characteristics...*continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal 2.5 V reference, Ta = 40 ºC, unless otherwise specified.

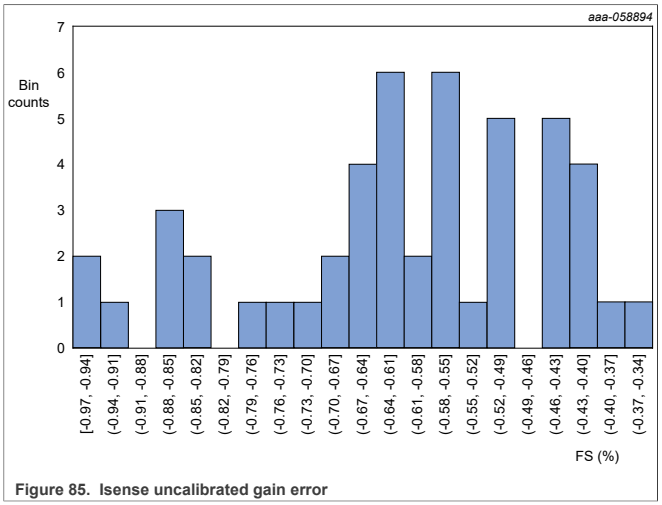


Figure 85. Isense uncalibrated gain error

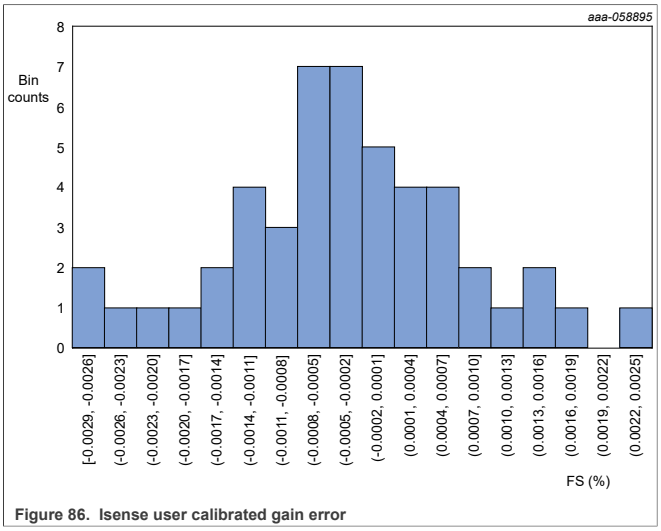


Figure 86. Isense user calibrated gain error

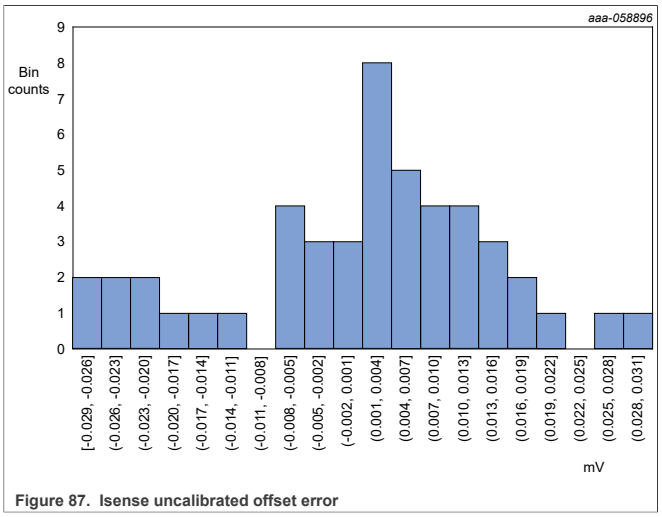


Figure 87. Isense uncalibrated offset error

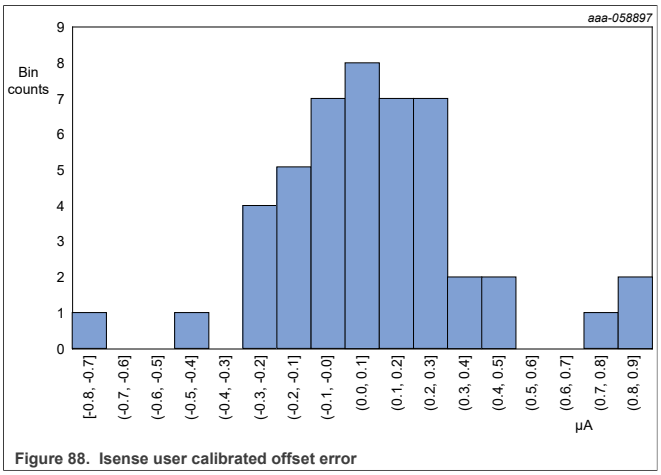


Figure 88. Isense user calibrated offset error

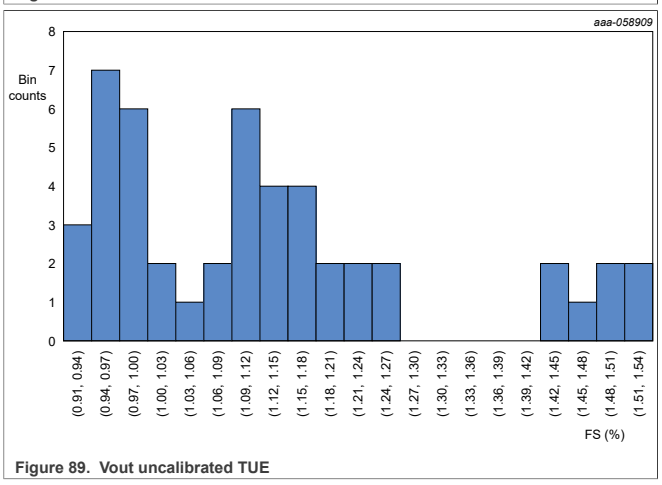


Figure 89. Vout uncalibrated TUE

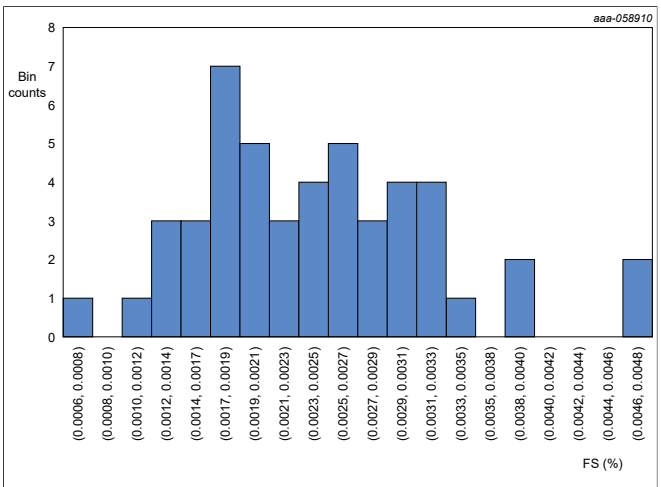


Figure 90. Vout user calibrated TUE

Typical operating characteristics...*continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal 2.5 V reference, Ta = 40 °C, unless otherwise specified.

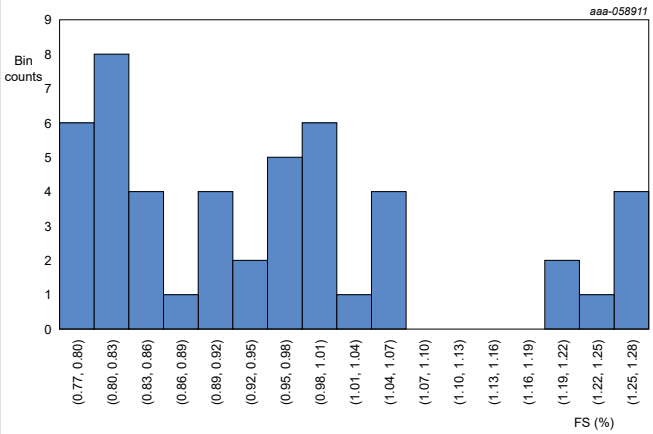


Figure 91. Vout uncalibrated gain error

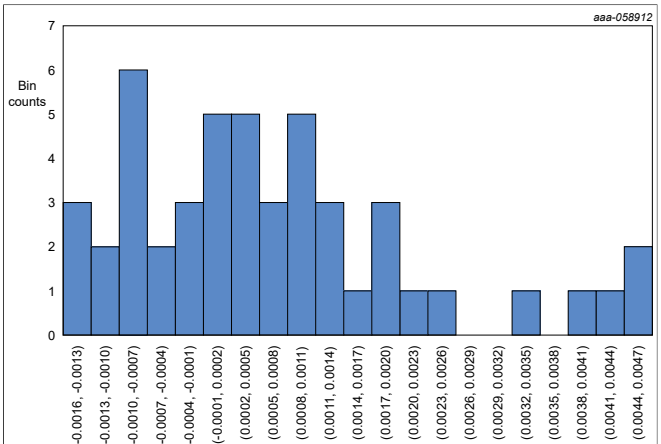


Figure 92. Vout user calibrated gain error

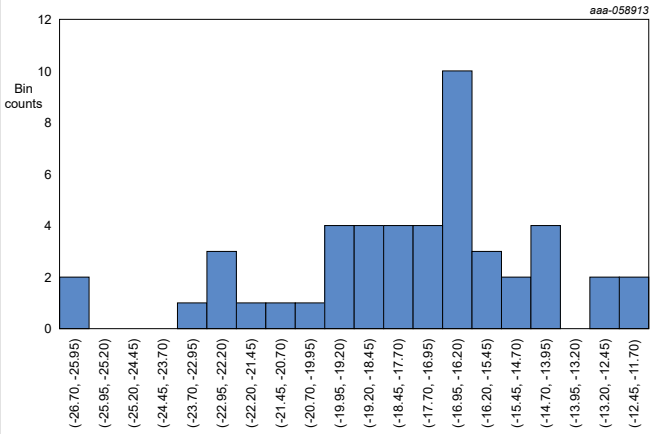


Figure 93. Vout uncalibrated offset error

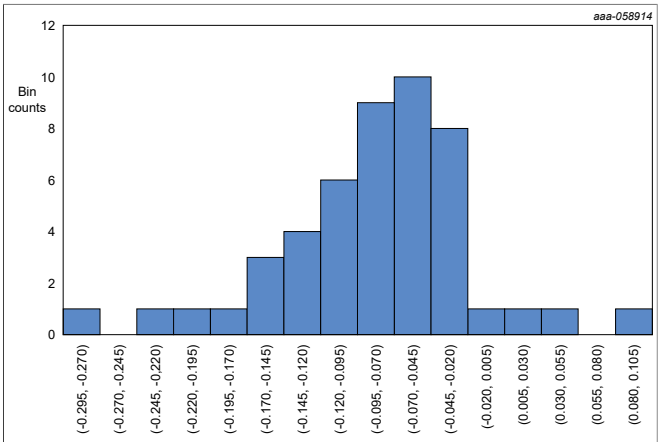


Figure 94. Vout user calibrated offset error

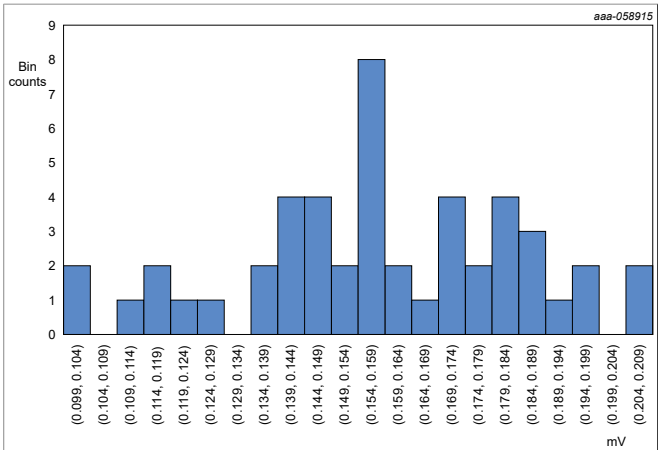


Figure 95. Vout INL

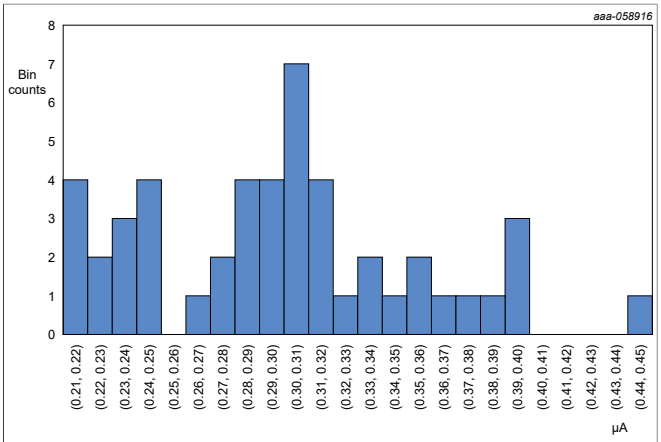


Figure 96. Cout INL

Typical operating characteristics...*continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal 2.5 V reference, Ta = 40 °C, unless otherwise specified.

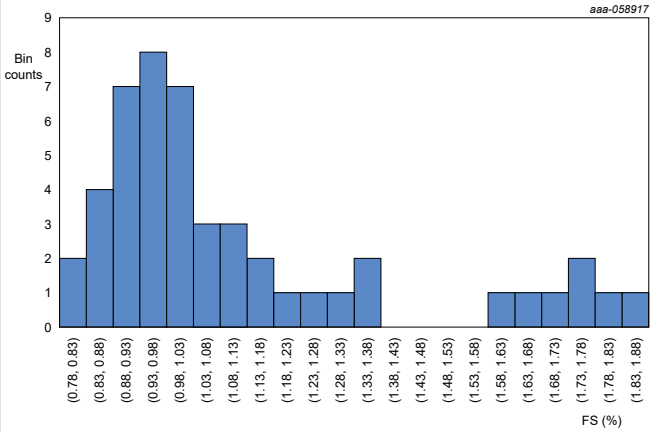


Figure 97. Cout uncalibrated TUE

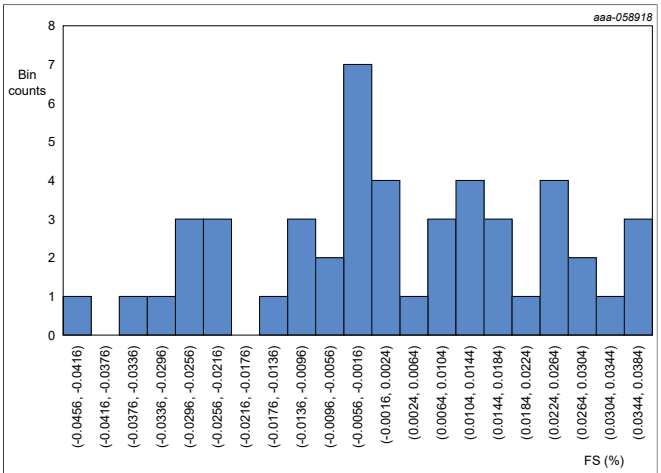


Figure 98. Cout user calibrated TUE

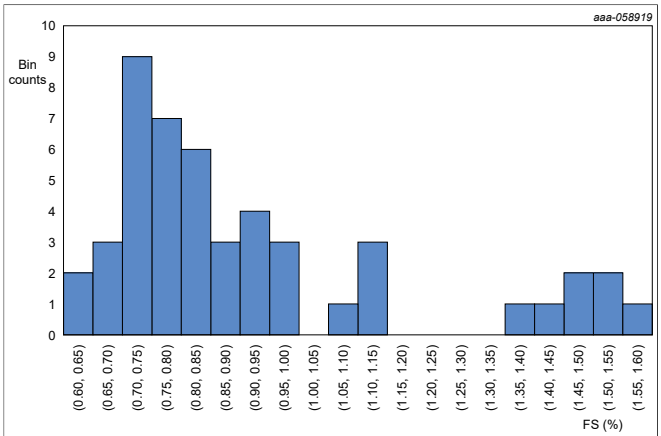


Figure 99. Cout uncalibrated gain error

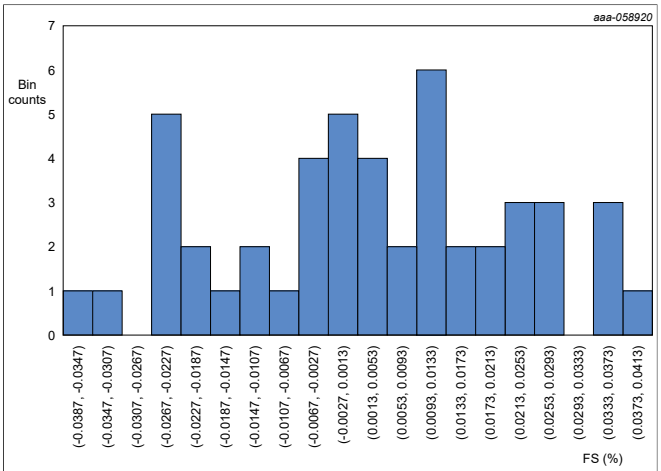


Figure 100. Cout user calibrated gain error

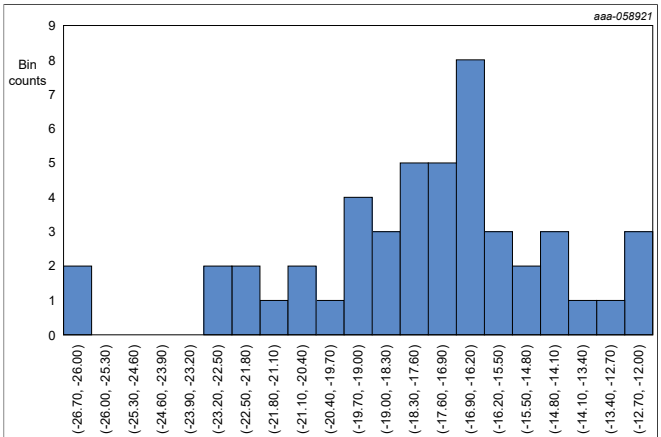


Figure 101. Cout uncalibrated offset error

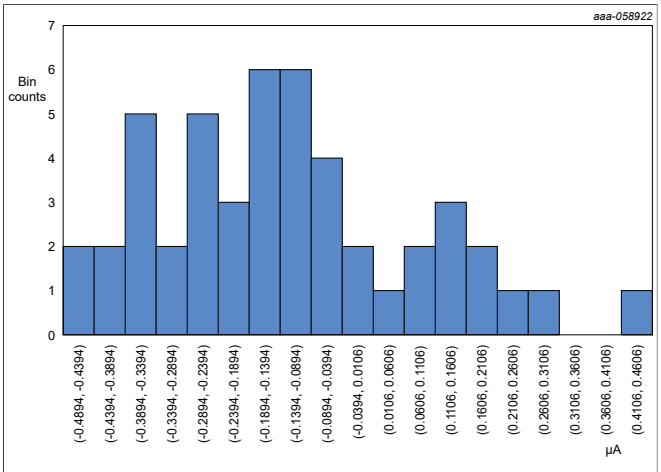


Figure 102. Cout user calibrated offset error

Typical operating characteristics...*continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal 2.5 V reference, Ta = 40 ºC, unless otherwise specified.

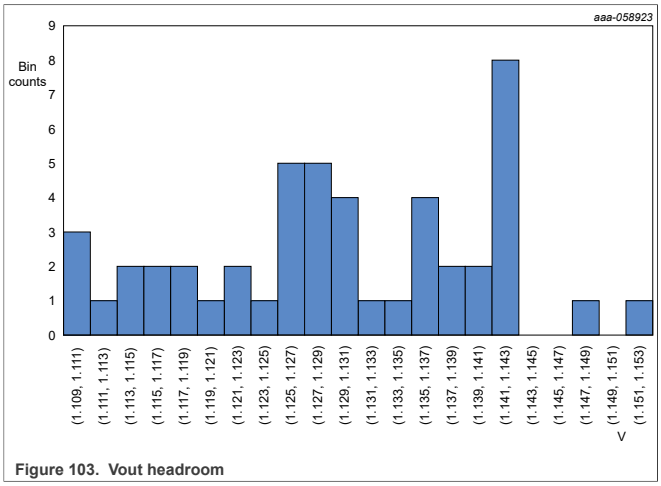


Figure 103. Vout headroom

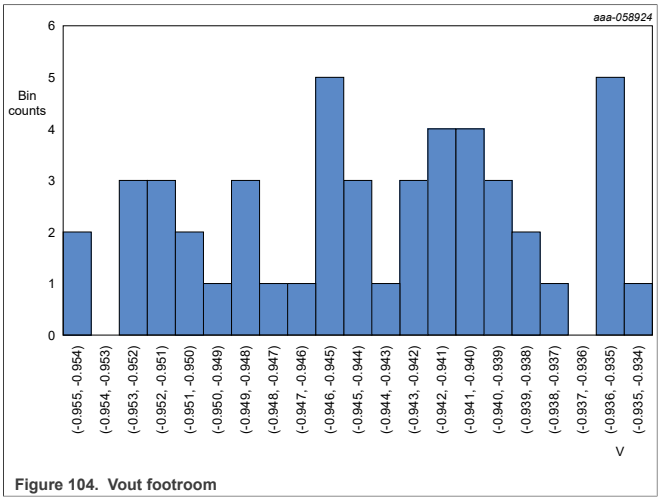


Figure 104. Vout footroom

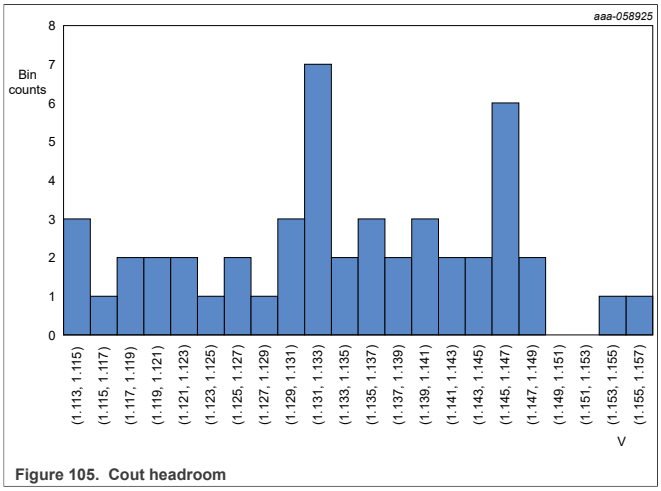


Figure 105. Cout headroom

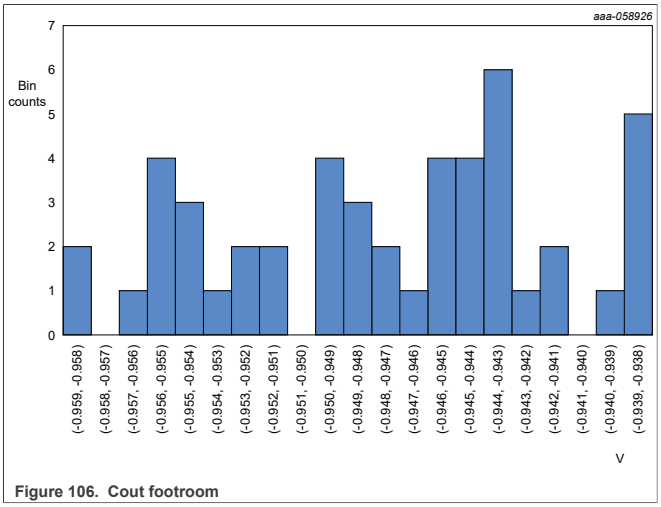


Figure 106. Cout footroom

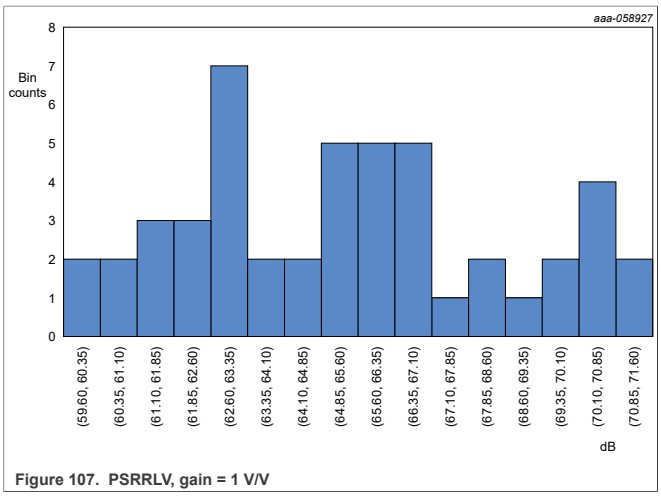


Figure 107. PSRRLV, gain = 1 V/V

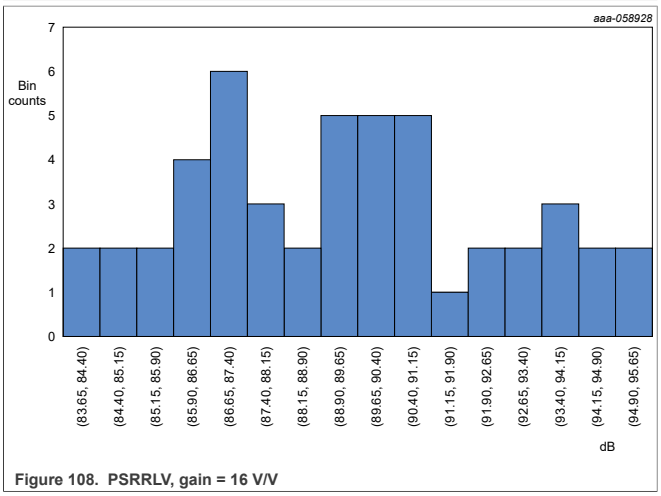


Figure 108. PSRRLV, gain = 16 V/V

Typical operating characteristics...*continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal 2.5 V reference, Ta = 40 °C, unless otherwise specified.

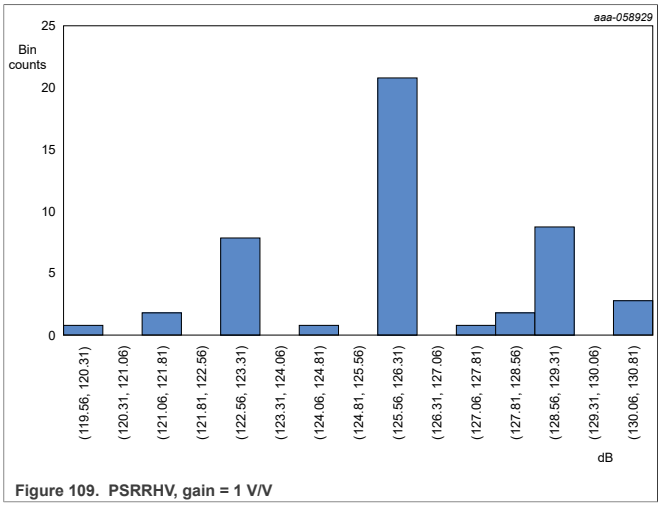


Figure 109. PSRRHV, gain = 1 V/V

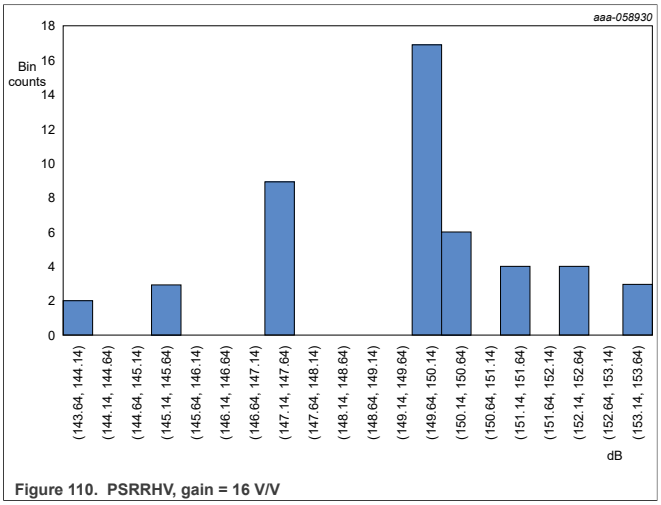


Figure 110. PSRRHV, gain = 16 V/V

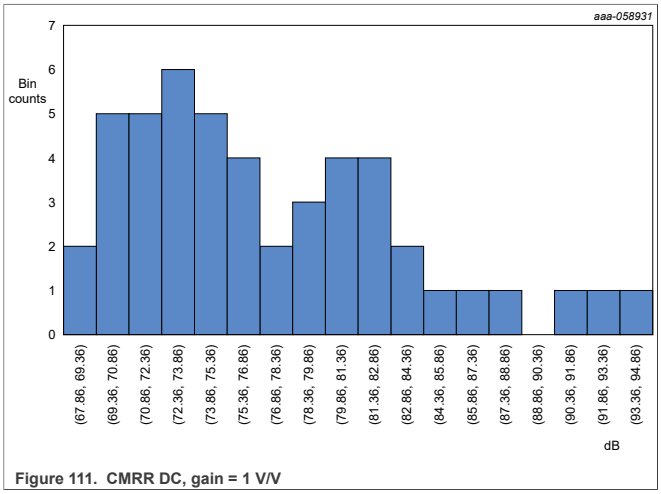


Figure 111. CMRR DC, gain = 1 V/V

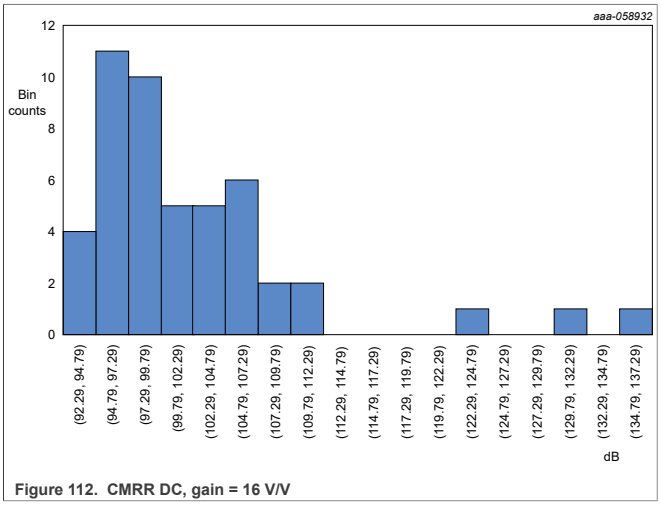


Figure 112. CMRR DC, gain = 16 V/V

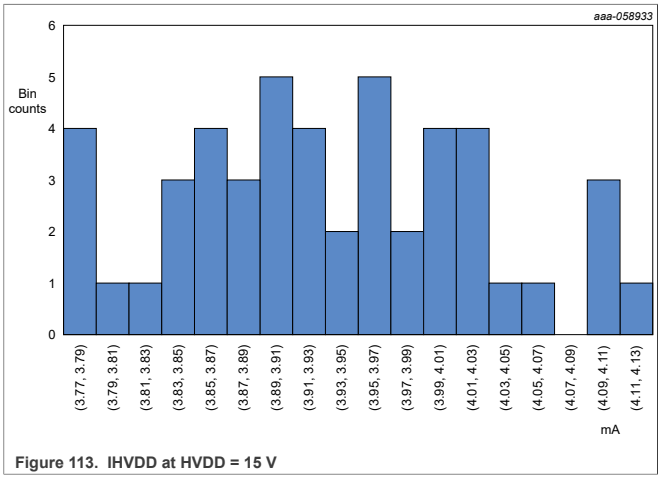


Figure 113. IHVDD at HVDD = 15 V

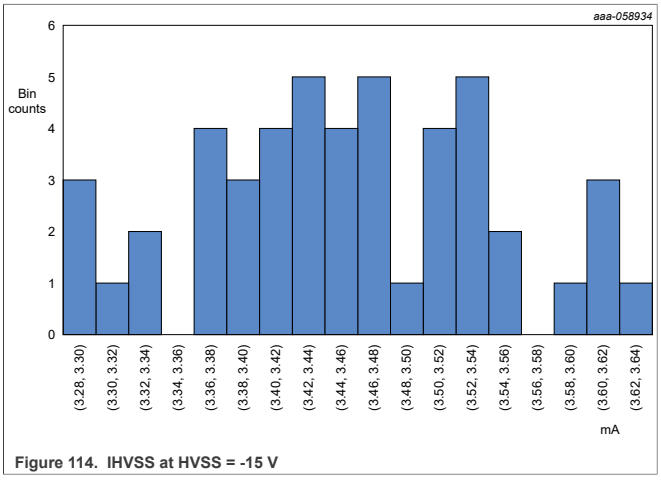


Figure 114. IHVSS at HVSS = -15 V

Typical operating characteristics...*continued*

VHVDD = -VHVSS = 15 V, VAVDD = VDVDD = 3.3 V, internal 2.5 V reference, Ta = 40 ºC, unless otherwise specified.

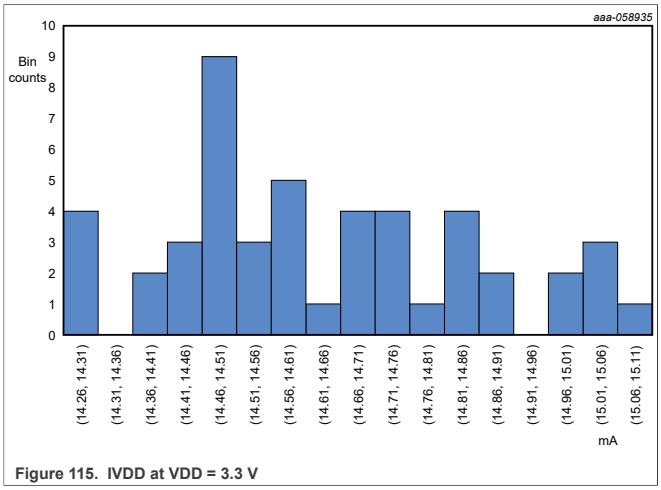


Figure 115. IVDD at VDD = 3.3 V

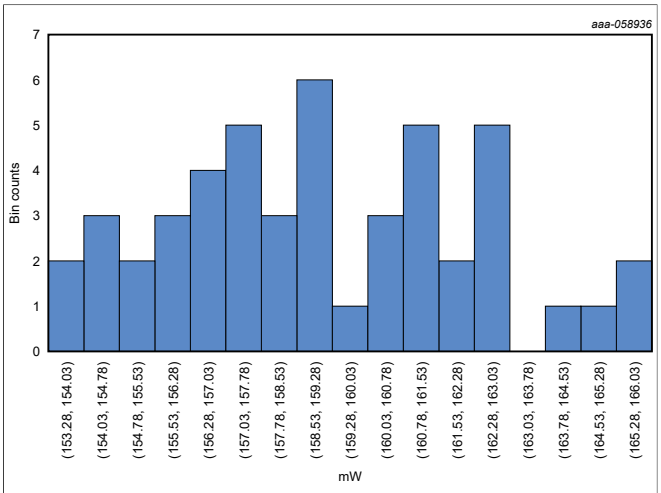


Figure 116. Total power (VDD = 3.3 V, HVDD = 15 V, HVSS = -15 V)

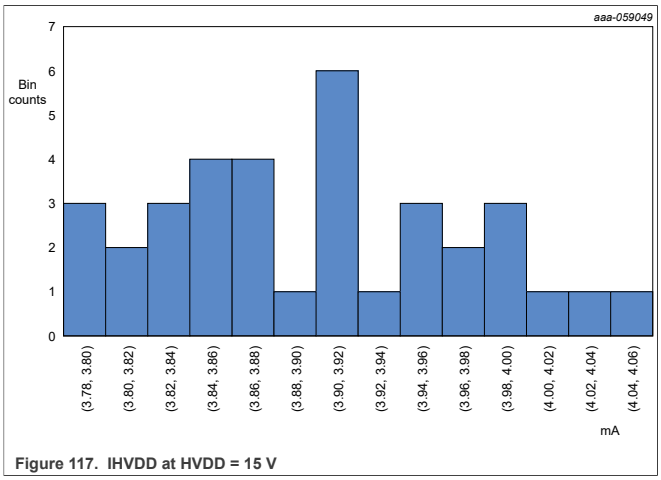


Figure 117. IHVDD at HVDD = 15 V

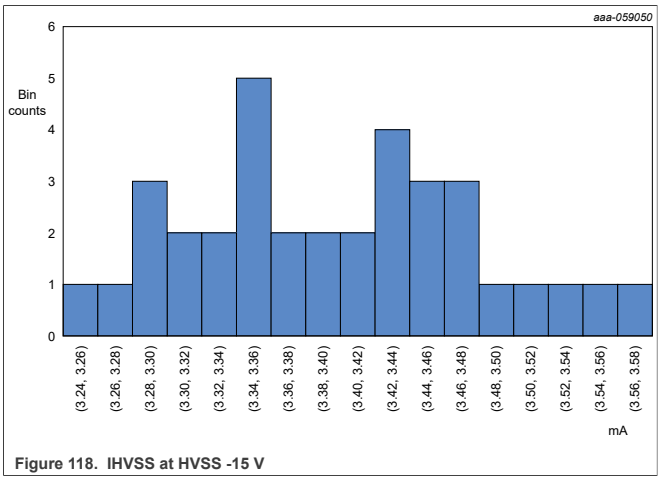


Figure 118. IHVSS at HVSS -15 V

13 Package outline

HVQFN-40, thermal enhanced thin quad flat package, no leads, dimple wettable flank; 40 terminals, 0.5 mm pitch, 6 mm x 6 mm x 0.8 mm body

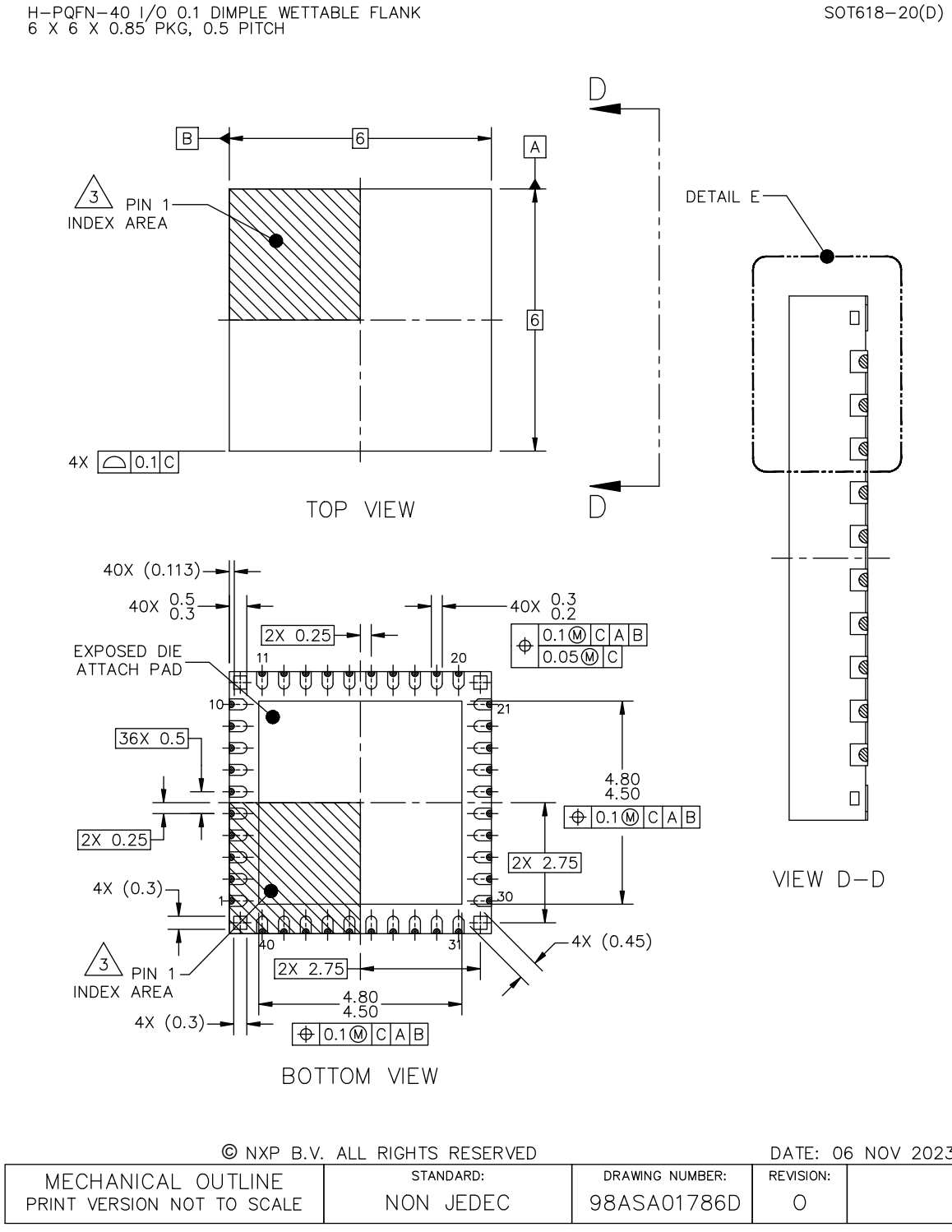
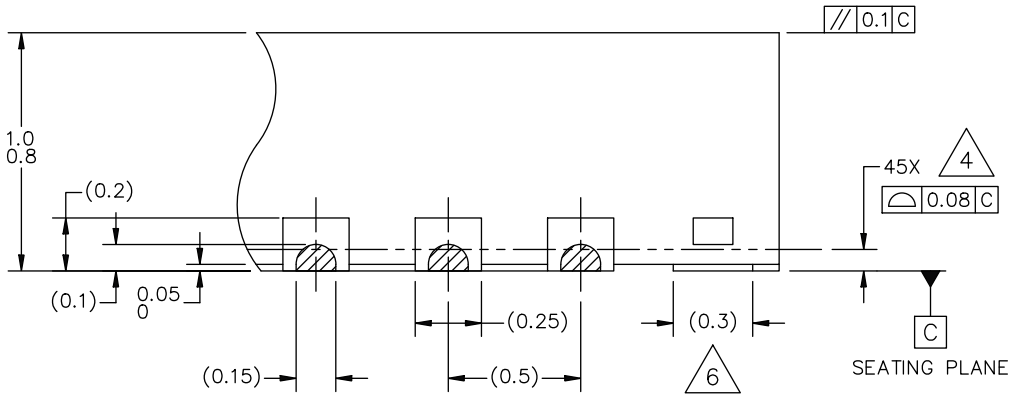


Figure 119. Top view/bottom view

H–PQFN–40 I/O 0.1 DIMPLE WETTABLE FLANK
6 X 6 X 0.85 PKG, 0.5 PITCH

SOT618–20(D)

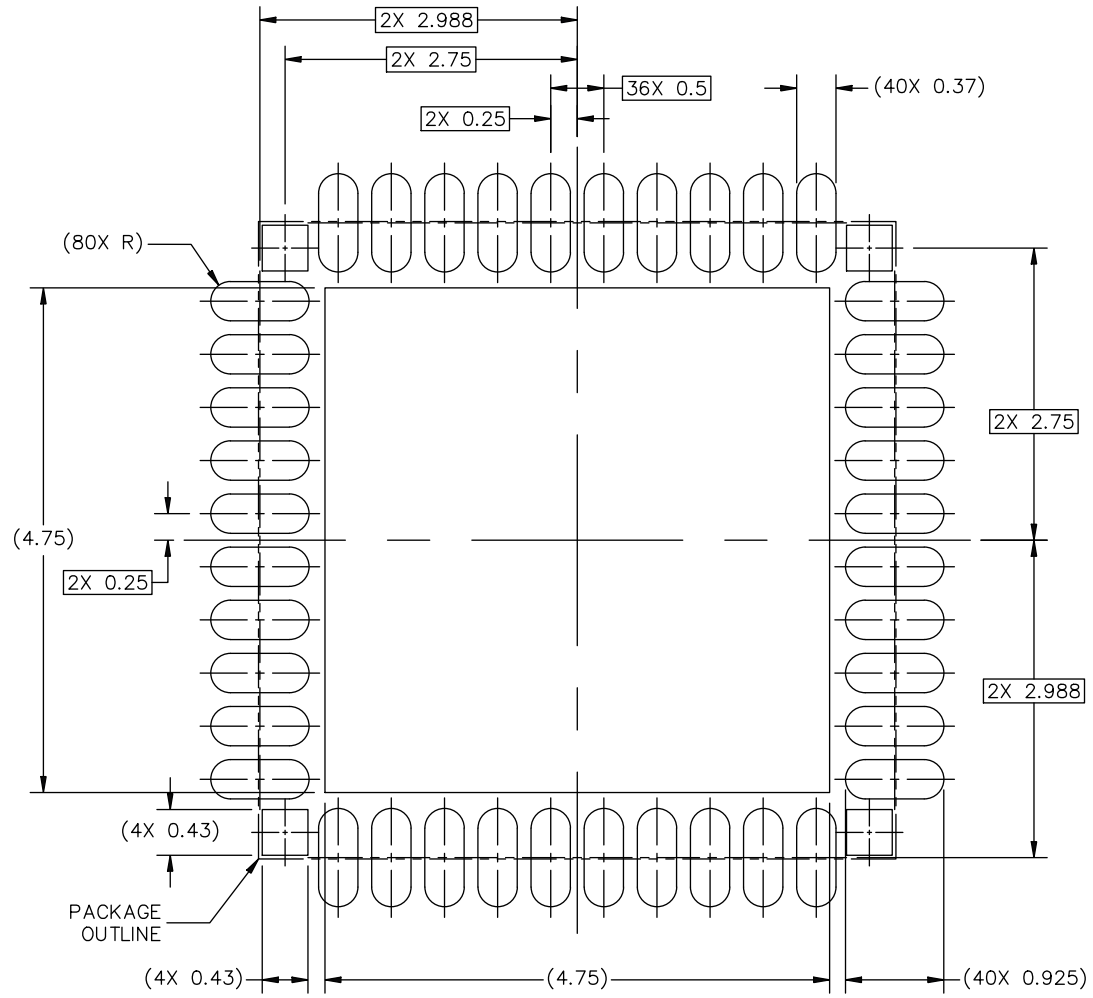


DETAIL E
VIEW ROTATED 90° CW

DATE: 06 NOV 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01786D	REVISION: O	

Figure 120. Detail E



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 06 NOV 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01786D	REVISION: O	

Figure 121. PCB design guidelines - Solder mask opening pattern

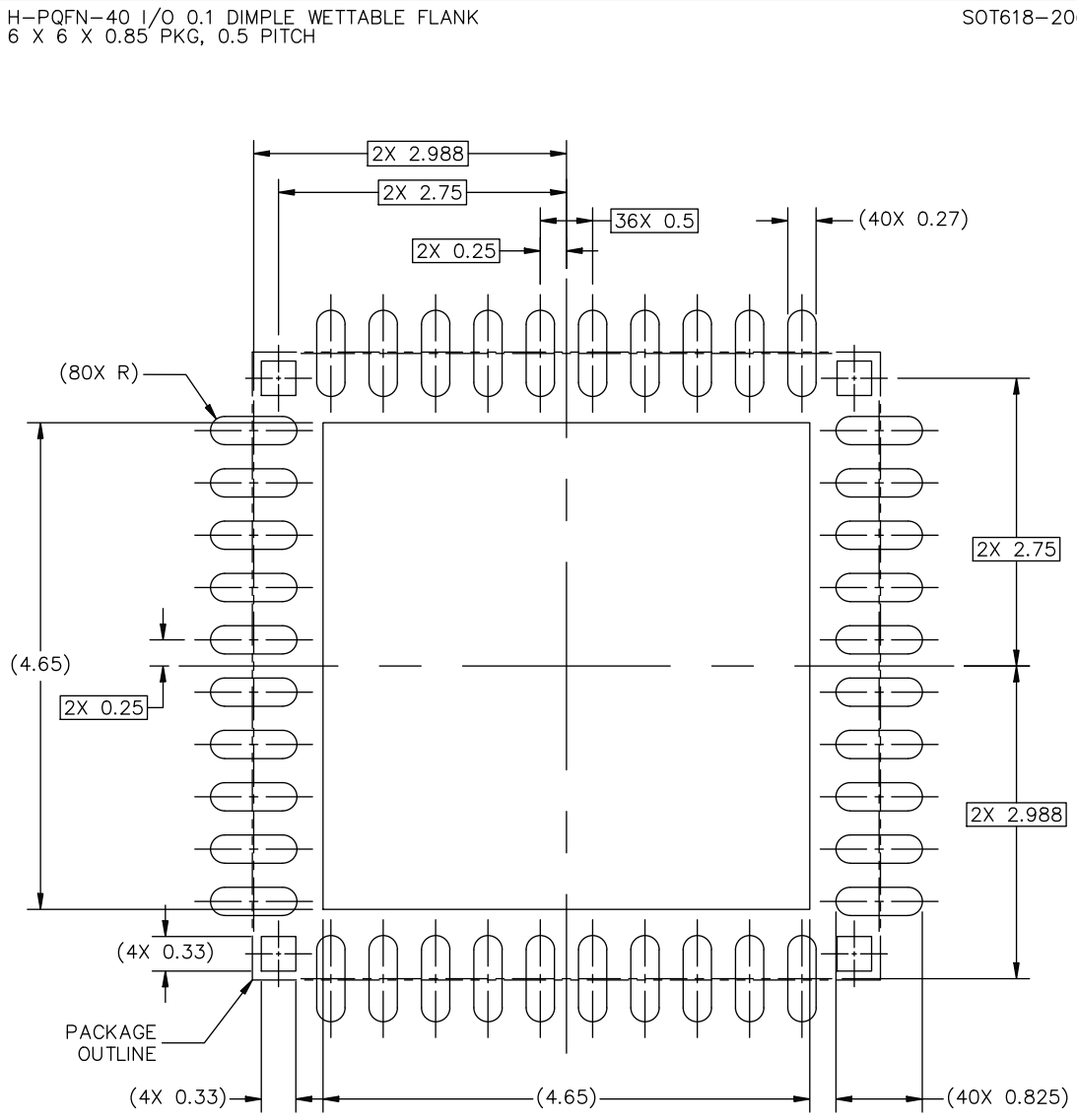


Figure 122. PCB design guidelines - I/O pads and solderable area

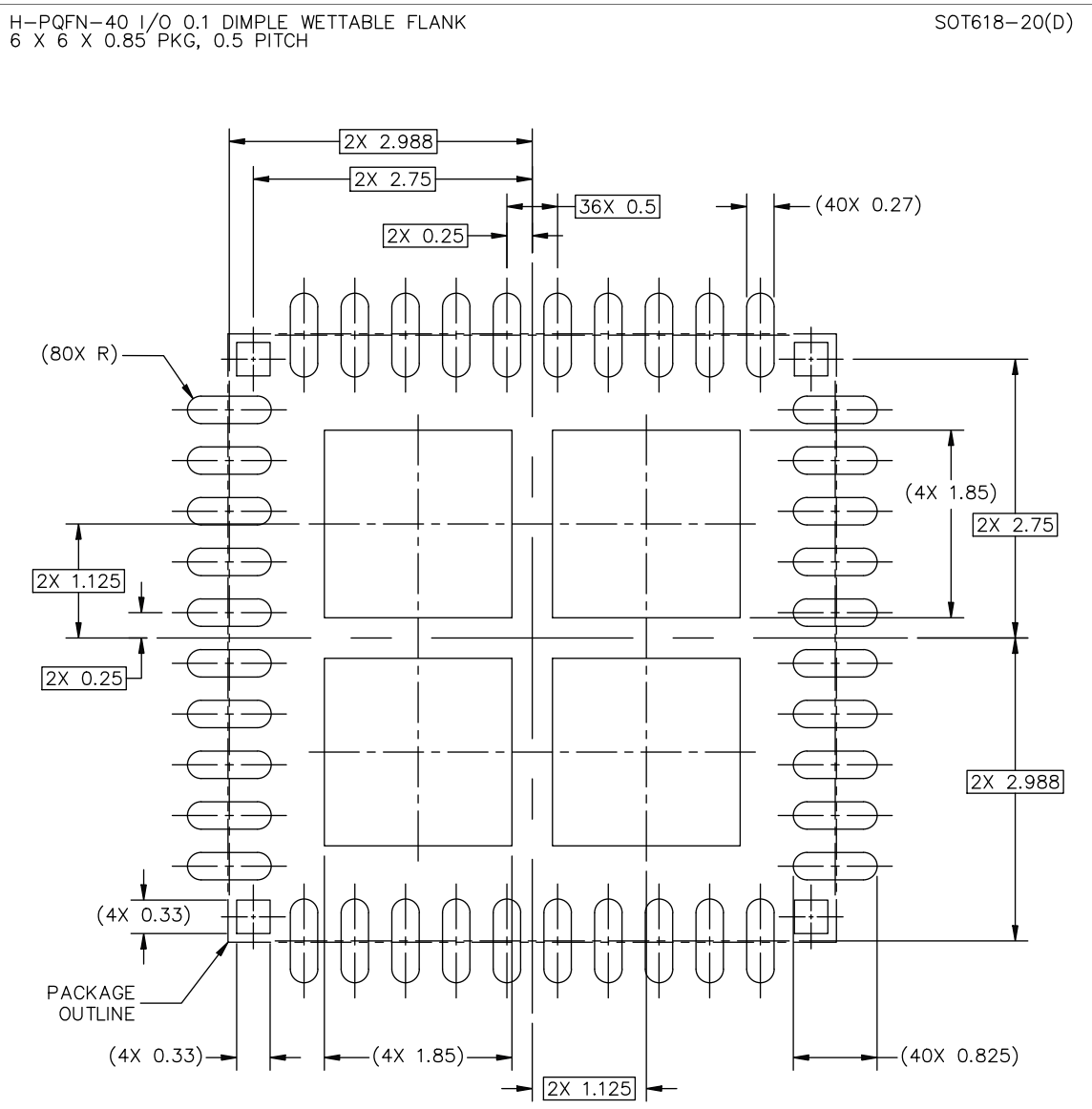


Figure 123. PCB design guidelines - solder paste stencil

Figure 124. Notes

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14 Revision history

Table 58. Revision history

Document ID	Release date	Description
NAFE93352 v.1.0	05 March 2025	Initial version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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