



Revised 15 October 2000

[Click here for information on how to use the Acrobat full-text Search function.](#)



[Click here to go to Table of Contents](#)

[Click here to go to List of Figures](#)

[Click here to go to List of Tables](#)

PREFACE

Section 1 OVERVIEW

Section 2 SIGNAL DESCRIPTIONS

Section 3 CENTRAL PROCESSING UNIT

Section 4 BURST BUFFER

Section 5 UNIFIED SYSTEM INTERFACE UNIT

Section 6 SYSTEM CONFIGURATION AND PROTECTION

Section 7 RESET

Section 8 CLOCKS AND POWER CONTROL

Section 9 EXTERNAL BUS INTERFACE

Section 10 MEMORY CONTROLLER

Section 11 L-BUS TO U-BUS INTERFACE (L2U)

Section 12 U-BUS TO IMB3 BUS INTERFACE (UIMB)

**Section 13 QUEUED ANALOG-TO-DIGITAL CONVERTER
MODULE-64**

Section 14 QUEUED SERIAL MULTI-CHANNEL MODULE

Section 15 MODULAR INPUT/OUTPUT SYSTEM (MIOS1)

Section 16 CAN 2.0B CONTROLLER MODULE

Section 17 TIME PROCESSOR UNIT 3

Section 18 DUAL-PORT RAM (DPTRAM)

Section 19 CDR MoneT FLASH EEPROM

Section 20 STATIC RANDOM ACCESS MEMORY (SRAM)

Section 21 DEVELOPMENT SUPPORT

Section 22 IEEE 1149.1-COMPLIANT INTERFACE (JTAG)

Appendix A MPC555 INTERNAL MEMORY MAP

Appendix B REGISTER GENERAL INDEX

Appendix C REGISTER DIAGRAM INDEX

Appendix D TPU ROM FUNCTIONS

Appendix E CLOCK AND BOARD GUIDELINES

Appendix F MEMORY ACCESS TIMING

Appendix G ELECTRICAL CHARACTERISTICS

**Appendix H FLASH ELECTRICAL CHARACTERISTICS FOR
ALL J76N MASK SETS AND 0K02A AND 1K02A ONLY**

INDEX