

LIST OF TABLES



Table	Title	Page
2-1	MPC509 Pin List.....	2-1
2-2	EBI Pin Definitions.....	2-2
2-3	MPC509 Power Connections.....	2-4
2-4	Pins with Internal Pull-Ups/Pulldowns.....	2-4
2-5	Signal Descriptions.....	2-5
2-6	Byte Enable Encodings.....	2-11
2-7	Address Type Definitions.....	2-14
3-1	RCPU Execution Units.....	3-5
3-2	FPSCR Bit Categories.....	3-11
3-3	FPSCR Bit Settings.....	3-12
3-4	Floating-Point Result Flags in FPSCR.....	3-13
3-5	Bit Settings for CR0 Field of CR.....	3-14
3-6	Bit Settings for CR1 Field of CR.....	3-15
3-7	CR n Field Bit Settings for Compare Instructions.....	3-15
3-8	Integer Exception Register Bit Definitions.....	3-16
3-9	Time Base Field Definitions.....	3-18
3-10	Machine State Register Bit Settings.....	3-19
3-11	Floating-Point Exception Mode Bits.....	3-20
3-12	Time Base Field Definitions.....	3-21
3-13	Uses of SPRG0–SPRG3.....	3-23
3-14	Processor Version Register Bit Settings.....	3-23
3-15	Manipulation of MSR[EE] and MSR[RI].....	3-24
3-16	Instruction Cache Control Registers.....	3-24
3-17	Development Support Registers.....	3-25
3-18	Instruction Set Summary.....	3-27
3-19	MPC509 Exception Classes.....	3-32
3-20	Exception Vector Offset Table.....	3-34
3-21	Instruction Latency and Blockage.....	3-36
4-1	Instruction Cache Programming Model.....	4-3
4-2	ICCST Bit Settings.....	4-4
4-3	I-Cache Address Register (ICADR).....	4-5
4-4	I-Cache Data Register (ICDAT).....	4-5
4-5	ICADR Bits Function for the Cache Read Command.....	4-8
4-6	ICDAT Layout During a Tag Read.....	4-9
5-1	SIU Address Map.....	5-3
5-2	SIUMCR Bit Settings.....	5-5
5-3	MEMMAP Bit Settings.....	5-7
5-4	Internal Memory Array Block Mapping.....	5-10



Table	Title	Page
5-5	EBI Signal Descriptions	5-13
5-6	Address Type Encodings.....	5-15
5-7	Byte Enable Encodings.....	5-15
5-8	Signals Driven at Start of Address Phase.....	5-20
5-9	Burst Access Address Wrapping	5-25
5-10	SPECADDR Bit Settings.....	5-26
5-11	SPECMASK Bit Settings.....	5-27
5-12	Example Speculative Mask Values.....	5-27
5-13	EBI Read and Write Access to 16-Bit Ports.....	5-28
5-14	Cycle Type Encodings	5-30
5-15	EBI Storage Reservation Interface Signals	5-35
5-16	Chip-Select Pin Functions	5-37
5-17	Chip-Select Module Address Map	5-40
5-18	Chip-Select Base Address Registers Bit Settings	5-41
5-19	Chip-Select Option Register Bit Settings	5-45
5-20	Block Size Encoding.....	5-47
5-21	Main Block and Sub-Block Pairings.....	5-49
5-22	TADLY and Wait State Control.....	5-52
5-23	Port Size	5-52
5-24	Pin Configuration Encodings	5-53
5-25	BYTE Field Encodings.....	5-54
5-26	REGION Field Encodings	5-54
5-27	Interface Types.....	5-56
5-28	Pipelined Reads and Writes	5-59
5-29	Data Bus Configuration Word Settings for Chip Selects.....	5-69
5-30	Clocks Module Signal Descriptions	5-72
5-31	Clock Module Power Supplies.....	5-72
5-32	System Clock Sources.....	5-73
5-33	CLKOUT Frequencies with a 4-MHz Crystal	5-77
5-34	Multiplication Factor Bits.....	5-78
5-35	Reduced Frequency Divider Bits	5-79
5-36	Exiting Low-Power Mode	5-81
5-37	System Clock Lock Bits	5-82
5-38	SCCR Bit Settings	5-86
5-39	SCLSR Bit Settings.....	5-88
5-40	System Protection Address Map	5-89
5-41	PCFS Encodings	5-90
5-42	Recommended Settings for PCFS[0:2].....	5-90
5-43	Example PIT Time-Out Periods.....	5-91
5-44	PICSR Bit Settings.....	5-93
5-45	BMCR Bit Settings	5-95



Table	Title	Page
5-46	Reset Status Register Bit Settings.....	5-96
5-47	Reset Behavior for Different Clock Modes.....	5-101
5-48	Pin Configuration During Reset	5-101
5-49	Data Bus Reset Configuration Word.....	5-103
5-50	SIU Port Registers Address Map.....	5-106
5-51	Port M Pin Assignments	5-108
5-52	Port A Pin Assignments	5-110
5-53	Port B Pin Assignments	5-110
5-54	Port I Pin Assignments	5-112
5-55	Port J Pin Assignments.....	5-112
5-56	Port K Pin Assignments	5-112
5-57	Port L Pin Assignments	5-113
6-1	PCU Address Map	6-2
6-2	PCUMCR Bit Settings.....	6-3
6-3	SWCR/SWTC Bit Settings.....	6-5
6-4	IMB2 Interrupt Multiplexing.....	6-8
6-5	Interrupt Controller Registers.....	6-9
6-6	PITQIL Bit Settings	6-11
6-7	Port Q Pin Assignments.....	6-13
6-8	Port Q Edge Select Field Encoding	6-13
7-1	MPC509 SRAM Module Addresses.....	7-2
7-2	SRAMMCR Bit Settings	7-4
8-1	Program Trace Cycle Attribute Encodings.....	8-3
8-2	Fetch Show Cycles Control	8-4
8-3	VF Pins Instruction Encodings.....	8-5
8-4	VF Pins Queue Flush Encodings.....	8-6
8-5	VFLS Pin Encodings.....	8-6
8-6	Cycle Type Encodings.....	8-7
8-7	Detecting the Trace Buffer Starting Point	8-10
8-8	I-bus Watchpoint Programming Options.....	8-17
8-9	L-Bus Data Events.....	8-19
8-10	L-Bus Watchpoints Programming Options.....	8-19
8-11	Trap Enable Data Shifted Into Development Port Shift Register	8-31
8-12	Breakpoint Data Shifted Into Development Port Shift Register	8-31
8-13	CPU Instructions/Data Shifted into Shift Register.....	8-31
8-14	Status Shifted Out of Shift Register — Non-Debug Mode	8-32
8-15	Status/Data Shifted Out of Shift Register	8-32
8-16	Sequencing Error Activity	8-33



Table	Title	Page
8-17	Checkstop State and Debug Mode.....	8-38
8-18	Debug Mode Development Port Usage.....	8-39
8-19	Non-Debug Mode Development Port Usage.....	8-41
8-20	Prologue Events.....	8-42
8-21	Epilogue Events.....	8-42
8-22	Peek Instruction Sequence.....	8-43
8-23	Poke Instruction Sequence.....	8-43
8-24	Development Support Programming Model.....	8-46
8-25	Development Support Registers Read Access Protection.....	8-47
8-26	Development Support Registers Write Access Protection.....	8-47
8-27	CMPE–CMPD Bit Settings.....	8-48
8-28	CMPE–CMPF Bit Settings.....	8-48
8-29	CMPG–CMPH Bit Settings.....	8-49
8-30	ICTRL Bit Settings.....	8-50
8-31	LCTRL1 Bit Settings.....	8-52
8-32	LCTRL2 Bit Settings.....	8-53
8-33	Breakpoint Counter A Value and Control Register (COUNTA).....	8-55
8-34	Breakpoint Counter B Value and Control Register (COUNTB).....	8-56
8-35	ECR Bit Settings.....	8-57
8-36	DER Bit Settings.....	8-58
9-1	JTAG Interface Pin Descriptions.....	9-3
9-2	Instruction Register Encoding.....	9-4