



APPENDIX B REGISTER GENERAL INDEX

–B–

BCSBAR (base address register) 3-116
BCSOR1 (BCS option register 1) 3-116, 3-117
BIUMCR (BIUSM module configuration register) 9-50
BIUSM
 module configuration register (BIUMCR) 9-50, 9-53
 time base register (BIUTBR) 9-51
BIUTBR (BIUSM time base register) 9-51

–C–

CANCTRL0 (control register 0) 10-25
CANCTRL1 (control register 1) 10-26
CANCTRL2 (control register 2) 10-28
CANICR (TouCAN interrupt configuration register) 10-24
CANMCR (TouCAN module configuration register) 10-23
CCW (conversion command word table) 8-48
CFSR0 (TPU3 channel function select register 0) 5-16
CFSR1 (TPU3 channel function select register 1) 5-16
CFSR2 (TPU3 channel function select register 2) 5-16
CFSR3 (TPU3 channel function select register 3) 5-16
CIER (TPU3 channel interrupt enable register) 5-15
CISR (TPU3 channel interrupt status register) 5-19
CPCR (CPSM control register) 9-53
CPR0 (TPU3 channel priority register 0) 5-18
CPR1 (TPU3 channel priority register 1) 5-19
CSBAR1 (base address register) 3-104, 3-105
CSBAR7 (base address register) 3-104, 3-105
CSOR1 (asynchronous chip selection option register) 3-105, 3-106
CSOR7 (asynchronous chip selection option register) 3-105, 3-106

–D–

DASM
 data register A (DASMA) 9-37
 data register B (DASMB) 9-38
 status/interrupt control register (DASMSIC) 9-35
DASMA (DASM data register A) 9-37, 9-38
DASMSIC (DASM status/interrupt control register) 9-35
DDRAB (Port A/B data direction register) 3-26
DDRC (Port data direction register) 3-29
DDRD (Port D data direction register) 3-32
DDRE (Port E data direction register) 3-35
DDRF (Port F data direction register) 3-40
DDRG (Port G data direction register) 3-44
DDRH (Port H data direction register) 3-45
DDRK (Port K data direction register) 3-48
DDRQA (PORTQA data direction register) 8-37
DLCMD2 command register (CMD) 11-34, 11-35, 11-38
DLCMD2 interrupt level register (ILR) 11-30
DLCMD2 interrupt pending register (IPR) 11-29



DLCMD2 module configuration register (MCR) 11-27
DLCMD2 receive data register (RDATA) 11-43
DLCMD2 status register (STAT) 11-40, 11-41
DLCMD2 symbol timing control and pre-scaler register (SCTL) 11-31
DPTBAR (RAM array base address register) 6-5
DPTMCR (DPTRAM module configuration register) 6-3
DPTRAM
 module configuration register (DPTMCR) 6-3
 RAMbase address register (DPTBAR) 6-4
 test register 6-4
DSCR (TPU3 development support control register) 5-13
DSSR (TPU3 development support status register) 5-14

–E–

ESTAT (error and status register) 10-30

–F–

FASRAM array base address registers (FBAR) 4-16
FASRAM array base address registers (FBAR-H) 4-17
FASRAM array base address registers (FBAR-L) 4-17
FASRAM comparator value registers (FCCR0, FCCR1) 4-18
FASRAM most recent match address register (FMATCH) 4-19, 4-20
FASRAM most recent match status register (FSTATUS) 4-20
FCSM
 status/interrupt control register (FMSMSIC) 9-7
FCSMCNT (FCSM counter register) 9-9
FCSMSIC (FCSM status/interrupt control register) 9-7

–H–

HSQR0 (TPU3 host sequence register 0) 5-17
HSQR1 (TPU3 host sequence register 1) 5-17
HSSR0 (TPU3 host service request register 0) 5-18
HSSR1 (TPU3 host service request register 1) 5-18

–I–

IFLAG (interrupt flag register) 10-32
IMASK (interrupt mask register) 10-32

–L–

LJSRR (left justified, signed result register) 8-51
LJURR (left justified, unsigned result register) 8-51

–M–

MCR (Module configuration register) 3-19, 3-20, 3-21
MCSM
 counter register (MCSMCNT) 9-14
 status/interrupt control register (MCSMSIC) 9-12
MCSMCNT (MCSM counter register) 9-14
MCSMML (MCSM modulus latch register) 9-14
MCSMSIC (MCSM status/interrupt control register) 9-12
MDR (Module disable register) 3-21
MISCNT (MISC counter) 6-6
MISRH (multiple input signature register high) 6-5
MISRL (multiple input signature register low) 6-5



PCON (Port configuration shadow register) 3-22
 PCPAR (Port C assignment register) 3-28
 PDPAR (Port D pin assignment register) 3-31
 PEPAR (Port D pin assignment register) 3-34
 PFEER (Port F edge-detect I/O register) 3-42
 PFLVR (Port F interrupt level register) 3-43
 PFPAR (Port F pin assignment register) 3-40
 PKPAR (Port K pin assignment register) 3-47
 PORTA (Port A output data register) 3-26
 PORTAP (Port A output data register) 3-27
 PORTB (Port B output data register) 3-27
 PORTBP (Port B pin data register) 3-27
 PORTC (Port C output data register) 3-29
 PORTCP (Port C pin data register) 3-30
 PORTD (Port D output data register) 3-32
 PORTDP (Port D pin data register) 3-33
 PORTE (Port E output data register) 3-35
 PORTEP (Port E pin data register) 3-35
 PORTF (Port F output data register) 3-41
 PORTFE (Port F edge-detect flag register) 3-42
 PORTFP (Port F pin data register) 3-41
 PORTG (Port G output data register) 3-44
 PORTG (Port G pin data register) 3-45
 PORTH (Port H output data register) 3-45
 PORTHP (Port H pin data register) 3-46
 PORTK (Port K output data register) 3-48
 PORTK (Port K pin data register) 3-48
 PORTQA (port QA data register) 8-36
 PORTQB (port QB data register) 8-36
 PRE (system protection prescaler register) 3-83
 PRES DIV (prescaler divide register) 10-27
 PWM
 counter register (PWMC) 9-48
 period register (PWMA) 9-47
 pulse width register (PWMB) 9-48
 PWMA (PWM period register) 9-48
 PWMB (PWM pulse width register) 9-48
 PWMC (PWM counter register) 9-49
 PWMSIC (PWSM status/interrupt control register) 9-45

QACR0 (QADC64 control register 0) 8-37
 QACR1 (QADC64 control register 1) 8-38
 QACR2 (QADC64 control register 2) 8-41
 QADC64
 control register 0 (QACR0) 8-37
 control register 1 (QACR1) 8-38
 control register 2 (QACR2) 8-40
 interrupt register (QADC64INT) 8-35
 port A/B data register (PORTQA/B) 8-36
 PORTQA data direction register (DDRQA) 8-37
 status register 0 (QASR0) 8-42
 status register 1 (QASR1) 8-44
 successive approximation register (SAR) 8-14
 QADC64INT (QADC64 interrupt register) 8-36
 QADC64MCR (QADC64 module configuration register) 8-35
 QASR0 (QADC64 status register 0) 8-43, 8-44
 QSM



configuration registers (QSMCR) 7-13
data direction registers (DDRQS) 7-17
interrupt level registers (QILR) 7-15
interrupt vector registers (QIVR) 7-15
pin assignment registers (PQSPAR) 7-16, 7-17
port data registers (PORTQS) 7-16

QSPI

control registers 0 (SPCR0) 7-21, 7-22
control registers 1 (SPCR1) 7-23
control registers 2 (SPCR2) 7-24, 7-25
control registers 3 (SPCR3) 7-26
status registers (SPSR) 7-27

–R–

RAMMCR (SRAM module configuration register) 12-4
RAMMCR RAMBAH, RAMBAL (SRAM array base address register) 12-5
RJURR (right justified, unsigned result register) 8-51
RSR (reset status register) 3-71, 3-72
RTI (Real-time interval register) 3-85
RTIT (Real-time interval counter and RTC operation register) 3-89
RXECTR (receive error counter) 10-33
RXGMSKHI (receive global mask register high) 10-29

–S–

SASM

data register A (SDATA) 9-22
data register B (SDATB) 9-23
status/interrupt control register A (SICA) 9-20
status/interrupt control register B (SICB) 9-22

SCI

control registers 0 (SCCR0) 7-49
control registers 1 (SCCR1) 7-50
data registers (SCDR) 7-55
status registers (SCSR) 7-52, 7-53
SDATA (SASM data register A) 9-22
SDATB (SASM data register B) 9-23
SICA (SASM status/interrupt control register A) 9-20
SICB (SASM status/interrupt control register B) 9-23
SWI (SWDOG interval register) 3-84
SWIT (Software watchdog interval timer operation register) 3-86
SWS (SWDOG service register) 3-82
SYNCR (synthesize control register) 3-62
SYNCR (synthesizer control register) 3-62
SYNST (synthesizer status register) 3-63
SYPCR (synthesizer protection control register) 3-78

–T–

TIC (timer protection control register) 3-80
TICR (TPU3 interrupt configuration register) 5-15
TIMER (free running timer register) 10-28
TIV (timer interrupt vector register) 3-81
TouCAN

control register 0 (CANCTRL0) 10-25
control register 1 (CANCTRL1) 10-26
control register 2 (CANCTRL2) 10-28
error and status register (ESTAT) 10-30
interrupt configuration register (CANICR) 10-24
interrupt flag register (IFLAG) 10-32



interrupt mask register (IMASK) 10-32
module configuration register (CANMCR) 10-23
prescaler divide register (PRES DIV) 10-27
receive buffer 14 mask registers 10-29
receive buffer 15 mask registers 10-30
receive global mask registers (RXGMSKHI) 10-29
receive mask registers 10-7

TPU3

channel function select registers (CFSRx) 5-16
channel interrupt enable register (CIER) 5-15
channel interrupt status register (CISR) 5-19
channel priority registers (CPRx) 5-18
development support control register (DSCR) 5-13
development support status register (DSSR) 5-14
host sequence registers (HSQRx) 5-17
host service request registers (HSSRx) 5-17
interrupt configuration register (TICR) 5-15
module configuration register (TPUMCR) 5-12
module configuration register 2 (TPUMCR2) 5-20
module configuration register 3 (TPUMCR3) 5-21
TPUMCR (TPU3 module configuration register) 5-12
TPUMCR2 (TPU3 module configuration register 2) 5-20
TPUMCR3 (TPU3 module configuration register 3) 5-21

