



APPENDIX C REGISTER DIAGRAM INDEX

–B–

BAR (breakpoint address register) 22-45
BBCMCR BBC module configuration register 4-25
BR0 (BR3 - memory controller base registers 0 - 3) 10-29

–C–

CALRLAM_OTR CALRAM ownership trace register 21-21
CANCTRL0 (control register 0) 16-25
CANCTRL1 (control register 1) 16-26
CANCTRL2 (control register 2) 16-28
CANICR (TouCAN interrupt configuration register) 16-24
CANMCR (TouCAN module configuration register) 16-22
CFSR0 (TPU3 channel function select register 0) 18-17
CFSR1 (TPU3 channel function select register 1) 18-17
CFSR2 (TPU3 channel function select register 2) 18-17
CFSR3 (TPU3 channel function select register 3) 18-17
CIER (TPU3 channel interrupt enable register) 18-16
CISR (TPU3 channel interrupt status register) 18-20
CMPA-CMPD (comparator A-D value register) 22-44
CMPE-CMPF (comparator E-F value registers) 22-45
CMPG-CMPH (comparator G-H value registers) 22-45
COLIR (change of lock interrupt register) 8-36
COUNTA (breakpoint counter A value and control register) 22-50
COUNTB (breakpoint counter B value and control register) 22-51
CPR0 (TPU3 channel priority register 0) 18-19
CPR1 (TPU3 channel priority register 1) 18-20
CR (condition register) 3-16
CRAM_RBAX CALRAM region base address register 21-19
CRAMMCR CALRAM module configuration register 6-36, 8-30, 21-16
CRAMOVLCALRAM overlay configuration register 21-20
CTR (count register) 3-19

–D–

DAR (data address register) 3-22
DDRQS (PORTQS data direction register) 14-14
DEC (decrementer register) 3-24, 6-39
DER (debug enable register) 22-53
DLCMD2 command register (CMD) 15-36
DLCMD2 interrupt level register (ILR) 15-31
DLCMD2 interrupt level register (ILR) 15-32
DLCMD2 interrupt pending register (IPR) 15-30
DLCMD2 Module configuration register (MCR) 15-27
DLCMD2 receive data register (RDATA) 15-34, 15-44
DLCMD2 status register (STAT) 15-41
DLCMD2 transmit data register (TDATA) 15-40
DMBR (dual mapping base register) 10-33
DMOR (dual mapping option register) 10-34
DPTMCR (DPTRAM module configuration register) 19-4
DSCR (TPU3 development support control register) 18-13
DSISR (dae/source instruction service register) 3-22

DSSR (TPU3 development support status register) 18-15

–E–

ECR (exception cause register) 22-52

EIBADR external interrupt relocation table base address register 4-31

EMCR (external master control register) 6-29

ESTAT (error and status register) 16-30

–F–

FASRAM module test register (FTEST) 17-42

FPRs - (floating-point registers) 3-12

FPSCR (floating-point status and control register) 3-13

–G–

GPRs (general-purpose registers) 3-12

–H–

HSQR0 (TPU3 host sequence register 0) 18-18

HSQR1 (TPU3 host sequence register 1) 18-18

HSSR0 (TPU3 host service request register 0) 18-19

HSSR1 (TPU3 host service request register 1) 18-19

–I–

ICTRL (i-bus support control register) 22-46

IFLAG (interrupt flag register) 16-33

IMASK (interrupt mask register) 16-32

IMMR (internal memory mapping register) 6-28

–L–

L2U_GRA (L2U global region attribute register) 11-16

L2U_MCR (L2U module configuration register) 11-14

L2U_RAx (L2U region X attribute register) 11-15

L2U_RBAx (L2U region x base address register) 11-14

LCTRL1 (I-bus support control register 1) 22-48

LCTRL2 (I-bus support control register 2) 22-49

LR (link register) 3-19

–M–

MCPSMSCR MCPSM status/control register 17-36

MDASMAR MDASM DataA register 17-60

MDASMBR MDASM DataB register 17-61

MDASMSCR MDASM status/control register 17-62

MI_GRA Global region attribute register 4-29

MIOS14ER1 interrupt enable register 17-29

MIOS14LVL0 interrupt register 17-30

MIOS14LVL1 register 17-30

MIOS14MCR module configuration register 17-34

MIOS14RPR0 request pending register 17-28

MIOS14RPR1 request pending register 17-29

MIOS14SR0 interrupt status register 17-27

MIOS14SR1 interrupt status register 17-28

MIOS14TPCR test and pin control register 17-32

MIOS14VEC vector register 17-33

MIOS14VNR module-version number register 17-33

MISCNT (MISC counter) 19-6, 20-7, 20-10, 20-13

MISRH (multiple input signature register high) 19-6





MISRL (multiple input signature register low) 19-6
MMCSMMML MMCSM modulus latch register 17-42
MMCSMSCR MMCSM status/control register 17-43
MPIO SMDDR MPIO SM data direction register 17-82
MPIO SMDR MPIO SM data register 17-82
MPWMCNTR MPWMSM counter register 17-76
MPWMPERR MPWMSM period register 17-75
MPWMPULR MPWMSM pulse width register 17-75
MPWMSCR MPWMSM status/control register 17-77
MRTCSMFRCH MRTCSM32-bit counter high buffer register 17-92
MRTCSMFRCL MRTCSM32-bit counter low buffer register 17-93
MRTCSMSCR MRTCSM status/control register 17-93
MSR (machine state register) 3-20
MSTAT (memory controller status register) 10-29

—O—

OR0 (OR3 - memory controller option registers 0 - 3) 10-31

—P—

PDMCR pads module configuration register 2-4
PDMCR2 pads module configuration register 2-5
PISCR (periodic interrupt status and control register) 6-43
PITC (periodic interrupt timer count) 6-43
PITR (periodic interrupt timer register) 6-44
PLPRCR (PLL, low power, and reset control register) 8-34
PORTQS (port QS data register) 14-12
PQSPAR (PORTQS pin assignment register) 14-13
PRES DIV (prescaler divide register) 16-27
PVR (processor version register) 3-26

—Q—

QADC64E control register 0 (QACR0) 13-16
QADC64E control register 1 (QACR1) 13-18
QADC64E control register 2 (QACR2) 13-20
QADC64E conversion command word table register (CCW) 13-33
QADC64E left justified, unsigned result format register (LJURR) 13-37
QADC64E left justified, signed result format register (LJSRR) 13-37
QADC64E port A data direction registers (DDRQA) 13-16
QADC64E port A data register (PORTQA) 13-15
QADC64E port B data direction register (DDRQB) 13-16
QADC64E port B data registers (PORTQB) 13-15
QADC64E right justified, unsigned result format register (RJURR) 13-37
QADC64E status register 0 (QASR0) 13-23
QADC64E status register 1 (QASR1) 13-29
QADCINT-QADC64E interrupt register (with IACK(C)/with ILBS(D) QADCINT 13-14
QDSCI_IL (QSM2 dual SCI interrupt level register) 14-9
QSCI1CR (QSCI1 control register) 14-60
QSCI1SR (QSCI1 status register) 14-62
QSMCMCCR (QSMCM module configuration register) 14-9
QSPI_IL (QSPI interrupt level register) 14-10

—R—

RAMBAR (ram array base address register) 19-5
READI DC 23-10
READI DID 23-9
READI DTA 1 and 2 23-16
READI RWA 23-13



READI UBA 23-12, 23-15
READI_OTR READI ownership trace register 23-8
Region base address registers (0 - 3) 4-27
Regionattribute registers (0 - 3) 4-27
RSR (reset status register) 7-5
RTC (real time clock) 6-42
RTCAL (real time clock alarm) 6-42
RTCSC (real time clock status and control register) 6-41
RXECTR (receive error counter) 16-33
RXGMSKHI (receive global mask register high) 16-29

–S–

SCCxR0 (QSMCM SCI control register 0) 14-46
SCCxR1 (QSMCM SCI control register 1) 14-47
SCDR (QSMCM SCI data register) 14-50
SCxSR (QSMCM SCIx status register) 14-48
SGPIOCR (SGPIO control register) 6-46
SGPIODT1 (SGPIO data register 1) 6-45
SGPIODT2 (SGPIO data register 2) 6-45
SIEL (SIU interrupt edge level register) 6-34
SIMASK (SIU interrupt mask register) 6-32, 6-33
SIPEND (SIU interrupt pending register) 6-31, 6-32
SIVEC (SIU interrupt vector) 6-34
SPCR0 (QSPI control register 0) 14-18
SPCR1 (QSPI control register 1) 14-19
SPCR2 (QSPI control register 2) 14-20
SPCR3 (QSPI control register) 14-21
SPRG0-SPRG3 (general special-purpose registers 0-3) 3-25
SPSR (QSPI status register) 14-21
SRR0 (machine status save/restore register 0) 3-24
SRR1 (machine status save/restore register 1) 3-25
SWSR (software service register) 6-38
SYPCR (system protection control register) 6-37

–T–

TB (time base) 3-19, 3-23, 6-40
TBREF0 (time base reference register 0) 6-40
TBREF1 (time base reference register 1) 6-40
TBSCR (time base control and status register) 6-41
TESR (transfer error status register) 6-38
TICR (TPU3 interrupt configuration register) 18-15
TIMER (free running timer register) 16-29
TPUMCR (TPU3 module configuration register) 18-11
TPUMCR2 (TPU3 module configuration register 2) 18-21
TPUMCR3 (TPU3 module configuration register 3) 18-23

–U–

UC3FCFIG (hard reset configuration word) 20-19
UIPEND (UIMB pending interrupt request register) 12-8
UMCR (UIMB module configuration register) 12-7

–V–

VSRMSR (VDDSRM control register) 8-37

–X–

XER (integer exception register) 3-18