IW611

1x1 Dual-band Wi-Fi 6 and Bluetooth 5.4 Solution

Rev. 7.0 — 20 March 2025 Product data sheet

1 Product overview

The IW611 is a highly integrated 2.4/5 GHz dual-band 1x1 Wi-Fi 6 and Bluetooth/Bluetooth Low Energy 5.4 single-chip solution optimized for a broad array of IoT and Industrial applications in smart home, smart devices and accessories, smart appliances, smart energy, industrial automation, gateways and many more. This high degree of integration contributes to very low system costs and a minimum external BOM while achieving efficient co-existence between all internal radios as well as external radios.

IW611 includes a full-feature Wi-Fi subsystem powered by NXP's 802.11ax (Wi-Fi 6) technology bringing higher throughput, better network efficiency, lower latency and improved range over previous generation Wi-Fi standards. The Wi-Fi subsystem integrates a Wi-Fi MAC, baseband, and direct-conversion radio with integrated PA, LNA, and transmit/receive switch removing the need for an RF front end module (FEMs), saving cost ,and reducing system complexity.

In addition to a Wi-Fi 6 radio, the IW611 integrates an independent Bluetooth 5.4 subsystem that supports Bluetooth and Bluetooth Low Energy (LE). The device features Bluetooth Profiles such as hands free (HFP), advanced audio distribution profile (A2DP) for audio streaming as well as additional profiles like dual wide band speech (WBS). For Bluetooth Low Energy, the IW611 enables 2 Mbit/s high speed data rate, long range, and extended advertising. Finally, LE Audio is supported utilizing Isochronous channels for a better overall audio experience.

The IW611 supports two front-end antenna configurations: single-antenna (Figure 1) and dual antenna (Figure 2). Read more about the single and dual antenna configurations in Section 5.

The IW611 integrates dedicated CPUs and memories for both the Wi-Fi and Bluetooth subsystems which enable real time, independent protocol processing. Interfaces for connecting the IW611 to external host processors include SDIO 3.0 for Wi-Fi and UART for Bluetooth.

Figure 1 shows the application diagram for the single-antenna configuration.

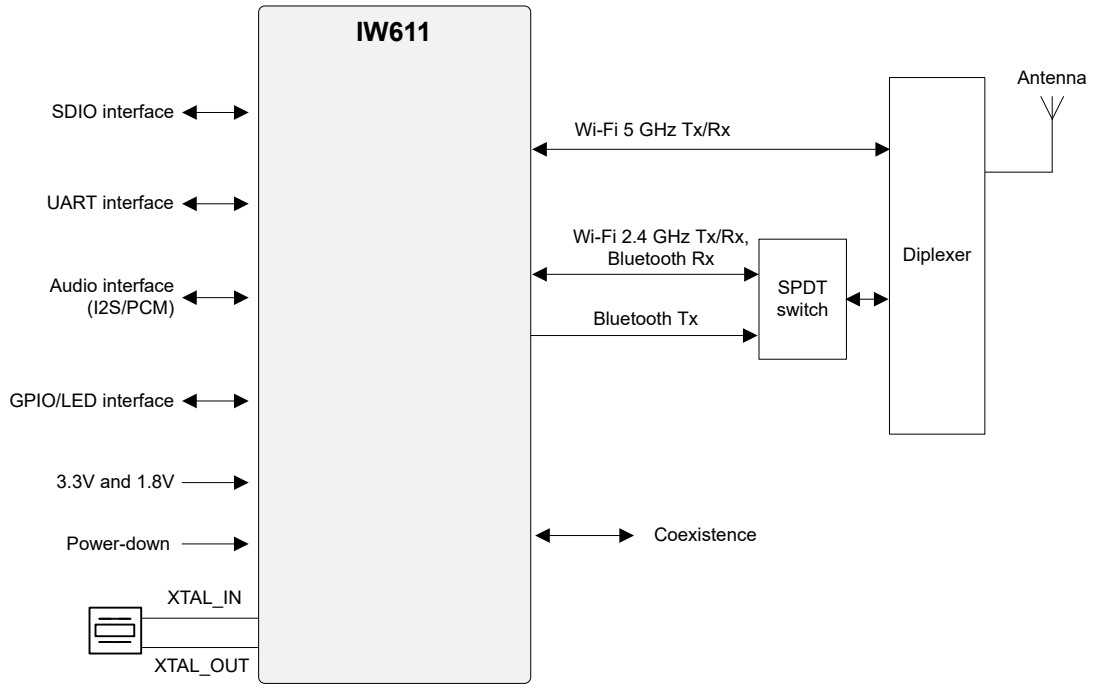

Figure 1. Application diagram - Single antenna configuration

Figure 2 shows the application diagram for the dual-antenna configuration.

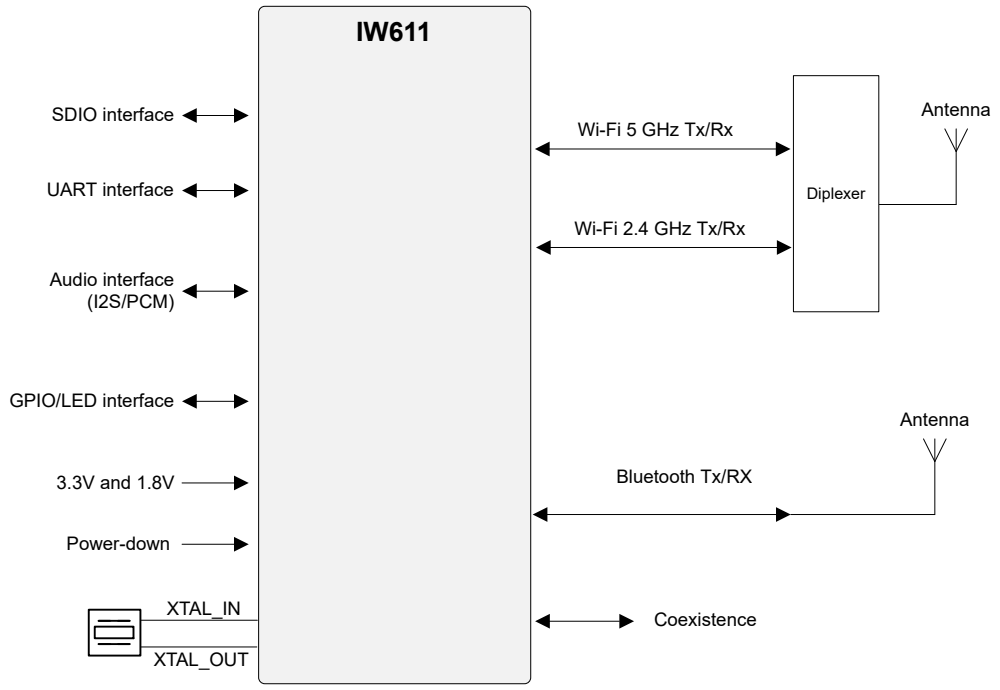

Figure 2. Application diagram – Dual-antenna configuration

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1.1 Applications

- Smart entertainment — Smart speaker, sound bar, audio receiver, smart display, streaming/OTT device, smart television, tablet
- Gateways/hubs/bridges — Voice assistant front-end, audio controller, and other radios to Wi-Fi/IP network
- Smart home — Control panel, security system, thermostat, sprinkler controller, security camera, garage door controller, smart outlet, light switch, smart doorbell, smoke alarm/CO detector
- Industrial — Building automation, smart lighting, Wi-Fi to other radio bridge, point of sale (POS) terminal
- Smart appliances — Refrigerator, washer, dryer, oven range, microwave, dishwasher, water heater, air conditioner, coffee pot, rice cooker, vacuum cleaner, air purifier

1.2 Wi-Fi key features

- IEEE 802.11a/b/g/n/ac/ax, 1x1 SISO 2.4 GHz and 5 GHz, up to 80 MHz channel bandwidth
- Peak data rates up to 480 Mbps
- Integrated high power PA up to +21 dBm transmit power
- Integrated LNA and T/R switches
- UL/DL OFDMA, UL/DL MU-MIMO (station only)
- 802.11ax TWT (station only)
- 802.11ax ER, DCM
- WPA2 and WPA3 personal and enterprise security
- Antenna diversity

1.3 Bluetooth key features

- Supports Bluetooth 5.2 (Class 1/Class 2) and Bluetooth Low Energy features
- Bluetooth 5.4 certified
- Integrated high power PA up to +19 dBm transmit power for Bluetooth LE and BDR[1,2,3]
- Integrated high power PA up to +10 dBm transmit power for EDR
- BDR/EDR packet types—1 Mbps (GFSK), 2 Mbps (π/4-DQPSK), 3 Mbps (8DPSK)
- Bluetooth LE long range (125/500 kbps) support
- Bluetooth LE 2 Mbps
- Bluetooth LE advertising extensions for improved capacity
- Isochronous channels (ISOC) supporting LE Audio and Auracast™ Broadcast Audio

1.4 Host interfaces

Wi-Fi and Bluetooth interface options

Table 1. Host interfaces

Wi-Fi	Bluetooth
SDIO 3.0	UART

1 Meets the Bluetooth SIG requirement of maximum power difference between GFSK and QPSK portions of the EDR packet to less than 10 dB.
2 The maximum TX power is limited to 14 dBm for Bluetooth LE Long Range packets.
3 The maximum TX power is 18 dBm for Bluetooth LE 2 Mbps for 2480 MHz channel.

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1.5 Operating characteristics

- Supply voltage: 1.8V and 3.3V
- Operating temperature
  - Commercial: 0 to 70°C
  - Industrial: -40 to 85°C
- Storage temperature: -55 to 125°C

1.6 General features

- Package options
  - HVQFN116 (dual-row) 9 mm x 9 mm x 0.85 mm with 0.5 mm pitch
  - WLCSP140 4.385 mm x 4.96 mm x 0.455 mm with 0.3 mm pitch
- Simultaneous Wi-Fi and Bluetooth receive
  - Single and dual antenna configurations supported
- Simultaneous Wi-Fi and Bluetooth transmit
  - Dual antenna configuration supported
- Coexistence
  - Internal coexistence between Wi-Fi, Bluetooth
  - External coexistence interface for connection to external radios such as LTE
- Power management
  - Efficient power management system
  - Deep-sleep low-power mode
  - Integrated high-efficiency buck DC-DC converter
  - Wake-up through GPIO, host interface, and RTC
- One Time Programmable (OTP) memory to store the MAC address and calibration data
- Security
  - Hardware root of trust
  - Authenticated and secured boot
  - OTP-based life-cycle state support

1.7 Product family devices

- AW611: Automotive AECQ-100 grade 3, Wi-Fi 6 and Bluetooth/Bluetooth Low Energy (LE)
- IW611: Wi-Fi 6 and Bluetooth/Bluetooth Low Energy (LE)
- IW612: Wi-Fi 6, Bluetooth/Bluetooth Low Energy (LE), and 802.15.4 Tri-radio

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1.8 Internal block diagram

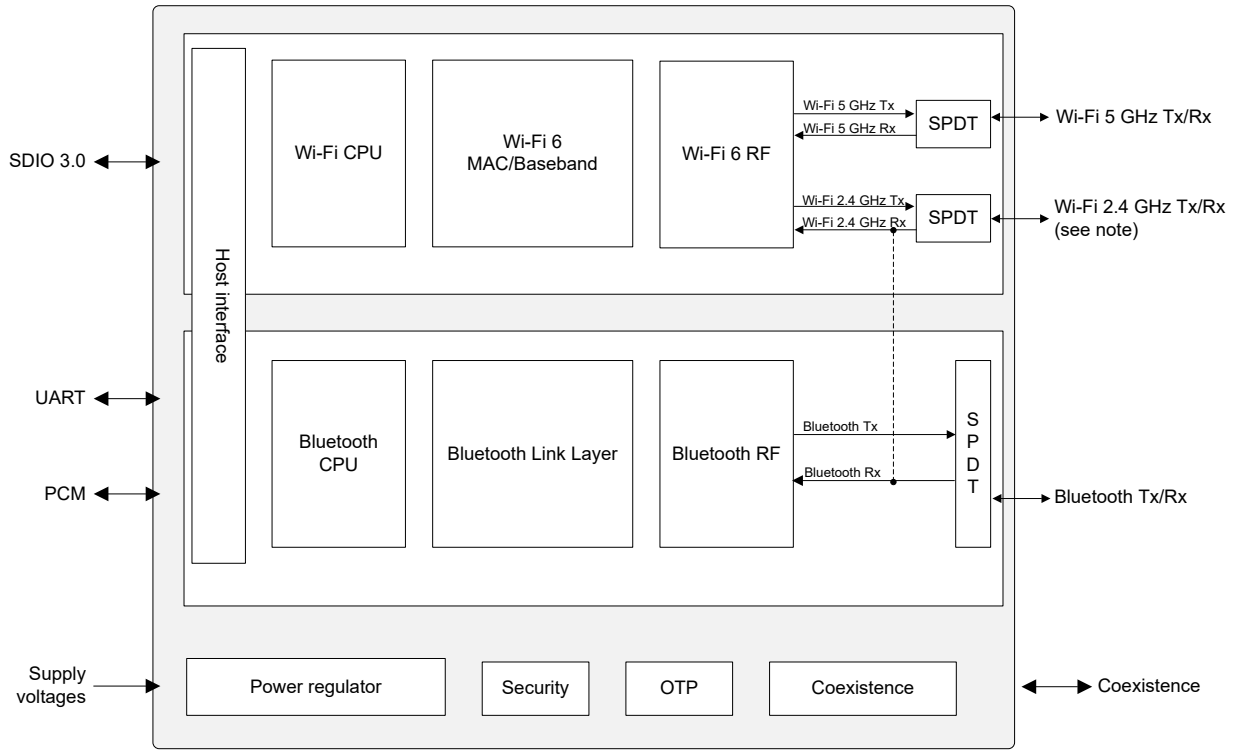

Figure 3. IW611 internal block diagram

Note: *Optional simultaneous receive path between Wi-Fi and Bluetooth (single-antenna configuration)*

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2 Ordering information

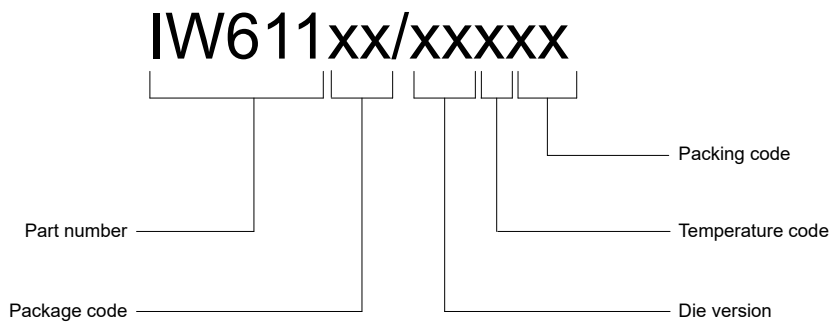

Figure 4. IW611 part numbering scheme

Table 2. Part order codes

Part order code	Package type	Operating temperature range	Packing
IW611HN/A1CK	HVQFN116 (dual-row) 9 mm x 9 mm x 0.85 mm with 0.5 mm pitch	Commercial	Tray
IW611HN/A1CMP	HVQFN116 (dual-row) 9 mm x 9 mm x 0.85 mm with 0.5 mm pitch	Commercial	Tape and Reel
IW611HN/A1IK	HVQFN116 (dual-row) 9 mm x 9 mm x 0.85 mm with 0.5 mm pitch	Industrial	Tray
IW611HN/A1IMP	HVQFN116 (dual-row) 9 mm x 9 mm x 0.85 mm with 0.5 mm pitch	Industrial	Tape and Reel
IW611UK/A1CZ	WLCSP140 4.385 mm x 4.96 mm x 0.455 mm with 0.3 mm pitch	Commercial	Tape and Reel
IW611UK/A1IZ	WLCSP140 4.385 mm x 4.96 mm x 0.455 mm with 0.3 mm pitch	Industrial	Tape and Reel

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3 Wi-Fi subsystem

3.1 IEEE 802.11 standards

- 802.11ax 1x1 SU and MU-MIMO/OFDMA
- 802.11ac Wave 1/2 backward compatible
- 802.11n/a/g/b backward compatible
- 802.11d operation in additional regulatory domains
- 802.11az accurate ranging
- 802.11e quality of service
- 802.11h transmit power control
- 802.11h DFS radar pulse detection
- 802.11k radio resource measurement
- 802.11mc precise indoor location positioning
- 802.11r fast hand-off for AP roaming
- 802.11v BTM frame transmission/reception
- 802.11w protected management frames
- 802.11y ECSA
- 802.11z tunneled direct link setup
- Fully supports clients (stations) implementing IEEE Power Save mode

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3.2 Wi-Fi MAC

- 802.11ax 1x1 MU-MIMO MAC
- Trigger Frame Formats
  - Basic trigger frame
  - MU-BAR, MU-RTS, Beamforming Report Poll (BFRP), BSR Poll (BSRP) trigger variant
  - Trigger frame MAC padding
- HE Variants of HT Control
  - Basic format
  - UL Power Headroom
  - Receive Operation Mode control subfield
- HE MU Frame Exchange Sequences
- M-BA and C-BA Variants in BA Frames
- MU-RTS/CTS Procedures
- Target Wait Time Scheduling
- HE Dual-NAV
- UL Carrier Sensing
- Buffer Status Reports in response to BSRP trigger frames
- Operating Mode Indication (OMI)
- A-MPDU Rx (de-aggregation) and Tx (aggregation) (supports single-MPDU A-MPDU)
- Reduced Inter-Frame Spacing (RIFS) receive
- Management information base counters
- Radio resource measurement counters
- Quality of service queues
- Block acknowledgment extension
- Dynamic frequency selection
- Multiple-BSS/Station
- Long and short preamble generation on a frame-by-frame basis for 802.11b frames
- Transmit rate adaptation
- Transmit power control
- Mobile hotspot

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3.3 Wi-Fi baseband

- 802.11ax 1x1 MU-MIMO baseband, backward compatible with 802.11ac/n/a/g/b technology
- Bandwidth support
  - 20 MHz
  - 40 MHz
  - 80 MHz
- Modulation and Coding Schemes (MCS)
  - 802.11ax—MCS0~11
  - 802.11ac—MCS0~9
  - 802.11n—MCS0~7
  - Dual Sub-Carrier Modulation (DCM)
    - MCS0
  - BCC and LDPC coding
- Frame Formats
  - 802.11ax HE_SU (Tx/Rx)
  - 802.11ax HE_MU (Rx)
  - 802.11ax HE_ER_SU (Tx/Rx)
  - 802.11ax HE_TB (Tx)
  - 802.11ac VHT
  - 802.11n HT
  - 802.11a (including dup/quad modes)
  - 802.11g (including dup mode)
  - 802.11b
- Uplink MU-MIMO Tx as STA
- Downlink MU-MIMO Rx as STA
- Aggressive Packet Extension
- Range Extension
- Receiver Beam Change
- Guard Interval Modes
  - 1x HE-LTF with 0.8 us GI
  - 1x HE-LTF with 1.6 us GI (for UL TB PPDU)
  - 2x HE-LTF with 0.8 us GI
  - 2x HE-LTF with 1.6 us GI
  - 4x HE-LTF with 3.2 us GI
  - 4x HE-LTF with 0.8 us GI
- Dynamic Frequency Selection (DFS) (radar detection)
- Optional 802.11ac and 802.11n MIMO features:
  - 20/40/80 MHz coexistence with middle-packet detection (GI detection) for enhanced CCA
  - LDPC transmission and reception for both 802.11ac and 802.11n
  - Short guard interval (0.4 us)
  - RIFS on receive path for 802.11n packets
  - VHT MU-PPDU (receive)
- Power save features

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3.4 Wi-Fi radio

- 5 GHz and 2.4 GHz Wi-Fi band operation
- 802.11ax 1x1 MU-MIMO on-chip RF radio
- Integrated PA, LNA

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3.5 RF channels

Table 3 shows the list of supported channels for 2.4 GHz and 5 GHz.

Table 3. List of supported Wi-Fi channels

Channel number	Frequency	Channel number	Frequency	Channel number	Frequency
2.4 GHz channel					
1	2412 MHz	2	2417 MHz	3	2422 MHz
4	2427 MHz	5	2432 MHz	6	2437 MHz
7	2442 MHz	8	2447 MHz	9	2452 MHz
10	2457 MHz	11	2462 MHz	12	2467 MHz
13	2472 MHz	—	—	—	—
5 GHz channel					
36	5180 MHz	40	5200 MHz	44	5220 MHz
48	5240 MHz	52	5260 MHz	56	5280 MHz
60	5300 MHz	64	5320 MHz	100	5500 MHz
104	5520 MHz	108	5540 MHz	112	5560 MHz
116	5580 MHz	120	5600 MHz	124	5620 MHz
128	5640 MHz	132	5660 MHz	136	5680 MHz
140	5700 MHz	144	5720 MHz	149	5745 MHz
153	5765 MHz	157	5785 MHz	161	5805 MHz
165	5825 MHz	169	5845 MHz	173	5865 MHz
177	5885 MHz	—	—	—	—

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3.6 Wi-Fi encryption

- Supports WPA2 and WPA3 personal and enterprise
- Data Frame Encryption/Decryption
  - Advanced Encryption Standard (AES) / Counter-Mode/CBC-MAC Protocol (CCMP)
  - Advanced Encryption Standard (AES) / Galois/Counter Mode Protocol (GCMP)
  - WLAN Authentication and Privacy Infrastructure (WAPI)
- Management Frame Encryption/Decryption for broadcast/multicast packets
  - Advanced Encryption Standard (AES) / Cipher-based Message Authentication Code (CMAC)
  - BIP-GMAC
- Management Frame Encryption/Decryption for unicast packets
  - AES/CCMP
  - AES/GCMP

3.7 Beamforming

- 802.11ax/ac/n Explicit Beamformee
  - Supports sounding feedback for up to 4x4 Beamformer

3.8 Wi-Fi host interface

- SDIO 3.0 (4-bit SDIO and 1-bit SDIO) with transfer rates up to SDR104 (208 MHz)

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4 Bluetooth subsystem

4.1 Bluetooth features

- Bluetooth 5.4 certified
- Bluetooth 5.2 features supported
- Bluetooth Class 2
- Bluetooth Class 1
- Single-ended, shared TX/RX path for Bluetooth
- Wi-Fi/Bluetooth coexistence protocol support
- I2S/PCM interface for voice applications
- Baseband/radio BDR/EDR packet types—1 Mbps (GFSK), 2 Mbps (π/4-DQPSK), 3 Mbps (8DPSK)
- Fully functional Bluetooth baseband—AFH, forward error correction, header error control, access code correlation, CRC, encryption bit stream generation, and whitening
- Interlaced scan for faster connection setup
- Simultaneous active ACL connection support
- Automatic ACL packet type selection
- Full central and peripheral piconet support[4]
- Scatternet support
- Standard UART HCI transport layer
- HCI layer to integrate with profile stack
- SCO/eSCO links with hardware accelerated audio signal processing and hardware supported PPEC algorithm for speech quality improvement
- All standard SCO/eSCO voice coding
- A2DP support
- All standard pairing, authentication, link key, and encryption operations
- Standard Bluetooth power-saving mechanisms (hold, sniff modes, and sniff subrating)
- Enhanced Power Control (EPC)
- Channel Quality Driven Data Rate (CQDDR)
- Wideband Speech (WBS) support (2 WBS links)
- Encryption (AES) support

4 The master/slave replacement in this document follows the recommendation of Bluetooth SIG.

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4.2 Bluetooth Low Energy (LE) features

- Bluetooth LE 5.4 certified
- Bluetooth LE 5.2 features supported
- Supports up to 16 simultaneous central/peripheral connections[5]
- Wi-Fi/Bluetooth coexistence protocol support
- Shared RF with BDR/EDR
- Encryption (AES) support
- Intelligent Adaptive Frequency Hopping (AFH)
- Bluetooth LE Privacy 1.3
- Bluetooth LE Secure Connection
- Bluetooth LE Data Length Extension
- Bluetooth LE Advertising Extension
- Bluetooth LE Long Range
- Bluetooth LE 2 Mbps
- Bluetooth LE power control
- Bluetooth LE isochronous channels[6]

4.3 Bluetooth host interface

- High-Speed UART with support up to 3 Mbps baud rate

5 The master/slave replacement in this document follows the recommendation of Bluetooth SIG.
6 Bluetooth LE audio supported with external host running Low Complexity Communication codec (LC3) through HCI interface

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4.4 Digital audio interfaces

4.4.1 I2S interface

- Central or peripheral mode[7]
- I2S (Inter-IC Sound) interface for audio data connection to Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC)
- 3-state I2S interface capability
- I2S pins shared with PCM pins
- Supports clock speeds of 4.096 MHz, 2.048 MHz, and 2 MHz

4.4.1.1 I2S interface signals

Refer to Section 6.7.8 "Digital audio interface".

4.4.1.2 I2S interface protocol

Figure 5 shows I2S interface protocol.

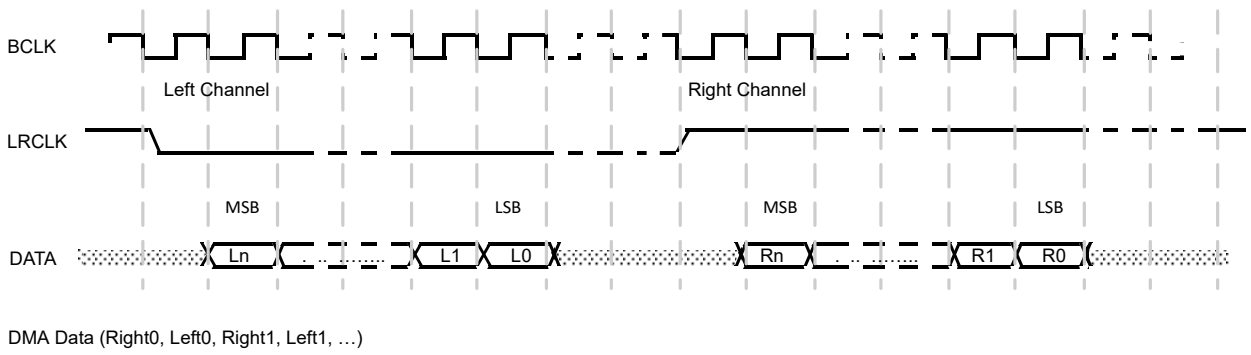

Figure 5. I2S interface protocol

7 The master/slave replacement in this document follows the recommendation of Bluetooth SIG.

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IW611 supports mono and dual channel modes.

In mono-channel mode, by default the left channel is used for data.

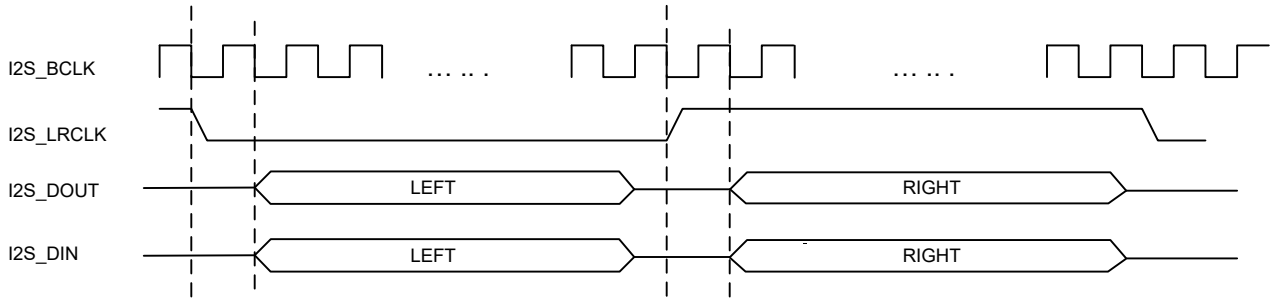

Figure 6. I2S timing specification diagram—Mono channel mode

In dual-channel mode, the two channels are supported on two time slots.

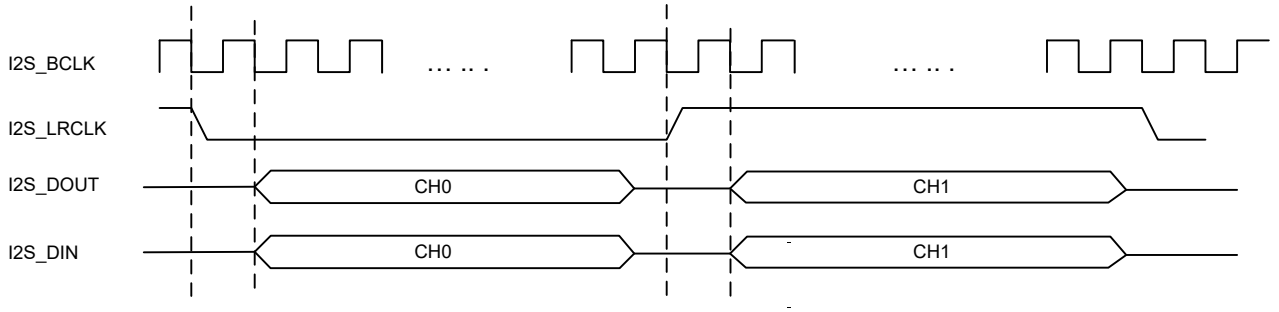

Figure 7. I2S timing specification diagram—Dual channel mode - Single Bluetooth

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4.4.1.3 Clock frequency and audio data resolutions

Audio data may arrive with different input data formats with different sampling rates.

In central mode, the I2S interface uses an audio input clock of 4.096 MHz or 2.048 MHz to provide the appropriate M clock (MCLK) and bit clock (I2S_BCLK) frequency to match the sampling rates of each audio data format. The sampling rates can be 8 kHz to 16 kHz.[8]

In peripheral mode, the I2S interface does not provide the bit clock (I2S_BCLK) but it can provide the M clock (MCLK)[8].

8 The master/slave replacement in this document follows the recommendation of Bluetooth SIG.

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4.4.2 PCM interface

- Central or peripheral mode[9]
- PCM bit width size of 16 bits
- Up to four slots with configurable bit width and start positions
- 3-state PCM interface capability
- PCM short frame synchronization
- PCM pins shared with I2S pins
- Supports clock speeds of 4.096 MHz, 2.048 MHz, and 2 MHz

4.4.2.1 PCM interface signal description

Refer to Section 6.7.8 "Digital audio interface".

4.4.2.2 PCM protocol

The PCM interface supports short frame sync. Figure 8 shows an example of a PCM interface with four signals.

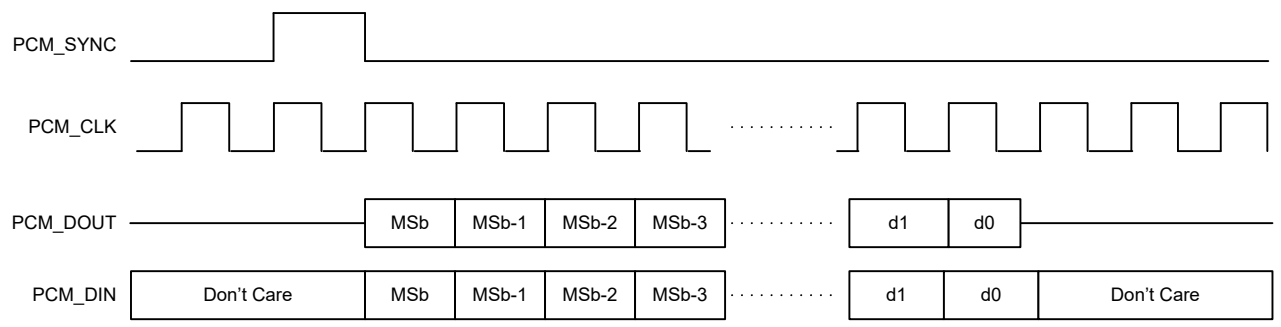

Figure 8. PCM short frame sync

9 The master/slave replacement in this document follows the recommendation of Bluetooth SIG.

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IW611 supports mono and dual channel modes.

Note: *Figure 9 and Figure 10 illustrate PCM mono and dual channel modes in short frame sync.*

In mono-channel mode, by default the left channel is used for data.

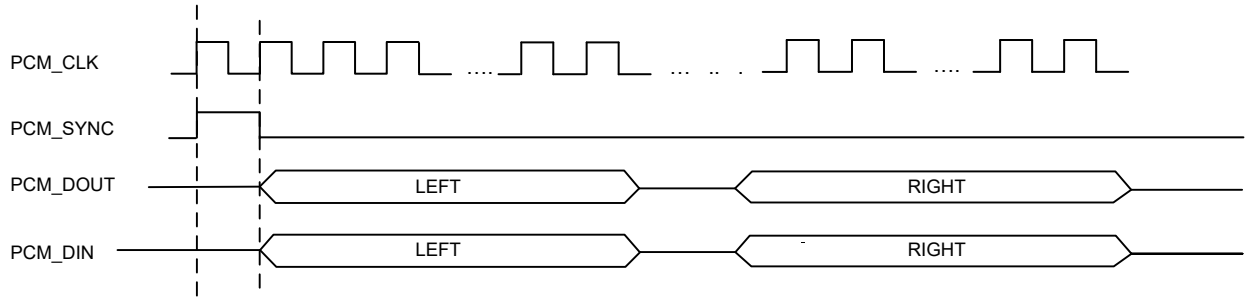

Figure 9. PCM mono channel mode (short frame sync)

In dual-channel mode, the two channels are supported on two time slots.

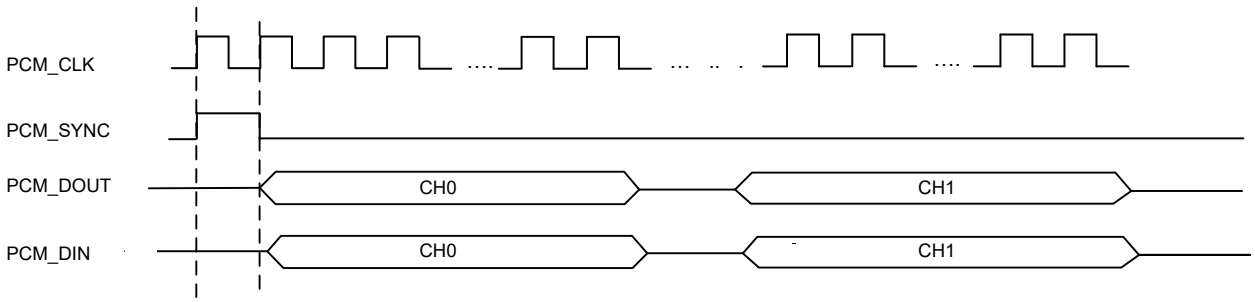

Figure 10. PCM dual channel mode (short frame sync)

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4.4.2.3 PCM modes of operation

The PCM interface supports two modes of operation:

- PCM central[10]
- PCM peripheral[10]

When in PCM central[10] mode, the interface generates a 2 MHz or a 2.048 MHz PCM_CLK and 8 kHz PCM_SYNC signal. An alternative PCM central[10] mode is available that uses an externally generated PCM_CLK, but still generates the 8 kHz PCM_SYNC. The external PCM_CLK must have a frequency that is an integer multiple of 8 kHz. Supported frequencies are in the 512 kHz to 4 MHz range.

When in PCM peripheral[10] mode, the interface has both PCM_CLK and PCM_SYNC as inputs, thereby letting another unit on the PCM bus generate the signals.

The PCM interface consists of up to four PCM slots (time divided) preceded by a PCM sync signal. Each PCM slot is 16 bits wide. The slots can be separated in time, but are not required to follow immediately after one other. The timing is relative to PCM_CLK. Figure 11 shows an example of a PCM burst with two slots.

The burst starts with a PCM_SYNC and then follows the PCM burst. In this example, the PCM burst consists of two PCM slots separated with two PCM_CLK clock cycles. The PCM slots can be configured to start at an arbitrary point in time, and the start value is given relative to the start of the PCM_SYNC. The timing of the four PCM slots must be such that slot 0 is always located before slot 1, slot 1 before slot 2, etc. It is possible to only use for example slot 1 and not slot 0.

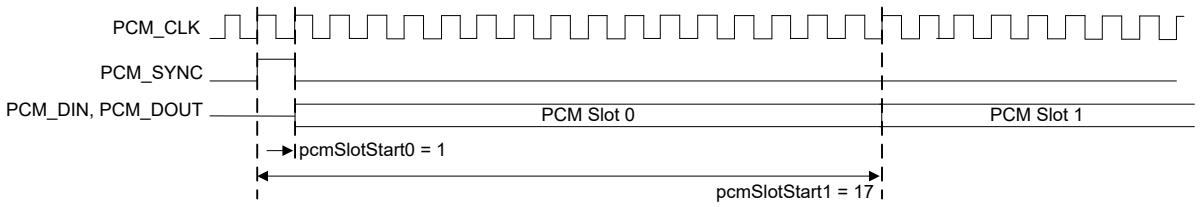

Figure 11. PCM burst with two PCM slots - PCM short frame sync

10 The master/slave replacement in this document follows the recommendation of Bluetooth SIG.

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5 Coexistence

5.1 Antenna configurations

The IW611 supports two antenna configurations: single-antenna and dual-antenna configurations.

5.1.1 Dual-antenna configuration

The two separate antennas allow simultaneous independent operation of the Wi-Fi and Bluetooth radios.

5.1.2 Single-antenna configuration

In single-antenna configuration, there is arbitration for the transmit operation of the Wi-Fi 2.4 GHz and Bluetooth/Bluetooth LE radios.

Table 4 shows the supported TX and/or RX operations with the IW611 single-antenna configuration.

Table 4. Wi-Fi and Bluetooth/Bluetooth LE supported TX and or RX operations - Single-antenna configuration

Row #	Bluetooth/ Bluetooth LE	Wi-Fi 2.4 GHz	Wi-Fi 5 GHz
1	TX	—	TX/RX
2	—	TX	—
3	RX	RX	—
4	RX	—	TX/RX

In single-antenna configuration:

- Wi-Fi 2.4 GHz TX and Bluetooth TX operations are arbitrated (rows 1 and 2)
- Wi-Fi 2.4 GHz RX and Bluetooth RX operations are simultaneous, using the optional path for simultaneous receive (Section 1.8) (row 3)
- Wi-Fi 5 GHz TX/RX and Bluetooth RX or TX operations are simultaneous (rows 1 and 4)

5.2 Central hardware packet traffic arbiter

The central hardware packet traffic arbiter arbitrates the transmit and/or receive operations between the on-chip Wi-Fi and Bluetooth radios as per the supported hardware configuration. See Section 5.1.

The central hardware packet traffic arbiter has the following features:

- Supports simultaneous Wi-Fi and Bluetooth transmissions to optimize output transmit power levels and performance
- Supports simultaneous receive for all on-chip radios

In addition to the on-chip radios, the central hardware packet traffic arbiter arbitrates one external radio. Refer to Section 5.3.

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5.3 Coexistence with an external radio

WCI-2 and PTA external coexistence interfaces are used for the coexistence with an external radio.

WCI-2 external coexistence interface

WCI-2 is the two-wire wireless coexistence interface 2 protocol defined in the Bluetooth Core Specification (Vol 7 Part C).

Figure 12 illustrates the hardware coexistence interface between the central hardware packet traffic arbiter and the external radio. In the figure, Wireless SoC is IW611.

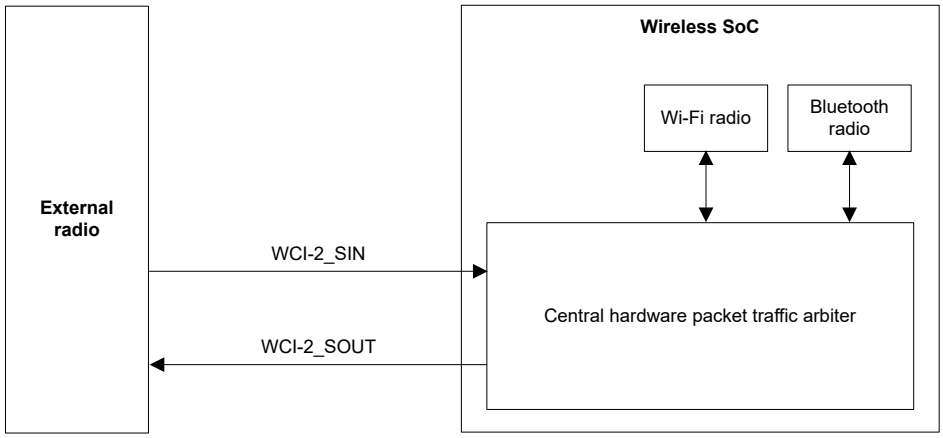

Figure 12. Hardware coexistence interface – WCI-2 coexistence interface

Note: *Refer to Section 6.7.10 for the description of WCI-2 coexistence interface signals.*

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PTA external coexistence interface

Figure 13 illustrates the hardware coexistence interface between the central hardware packet traffic arbiter and the external radio. In the figure, Wireless SoC is IW611.

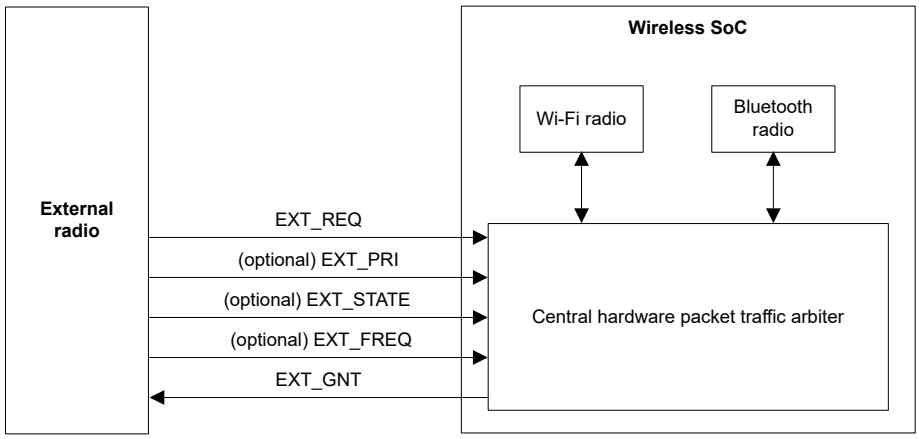

Figure 13. Hardware coexistence interface – PTA external coexistence interface

Note: *Refer to:*

- *Section 6.7.9 for the description of PTA external coexistence interface signals*
- *The application note Coexistence Overview for AW611/IW611 (AN13375) for more information on the coexistence feature*

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6 Pin information

6.1 Signal diagram

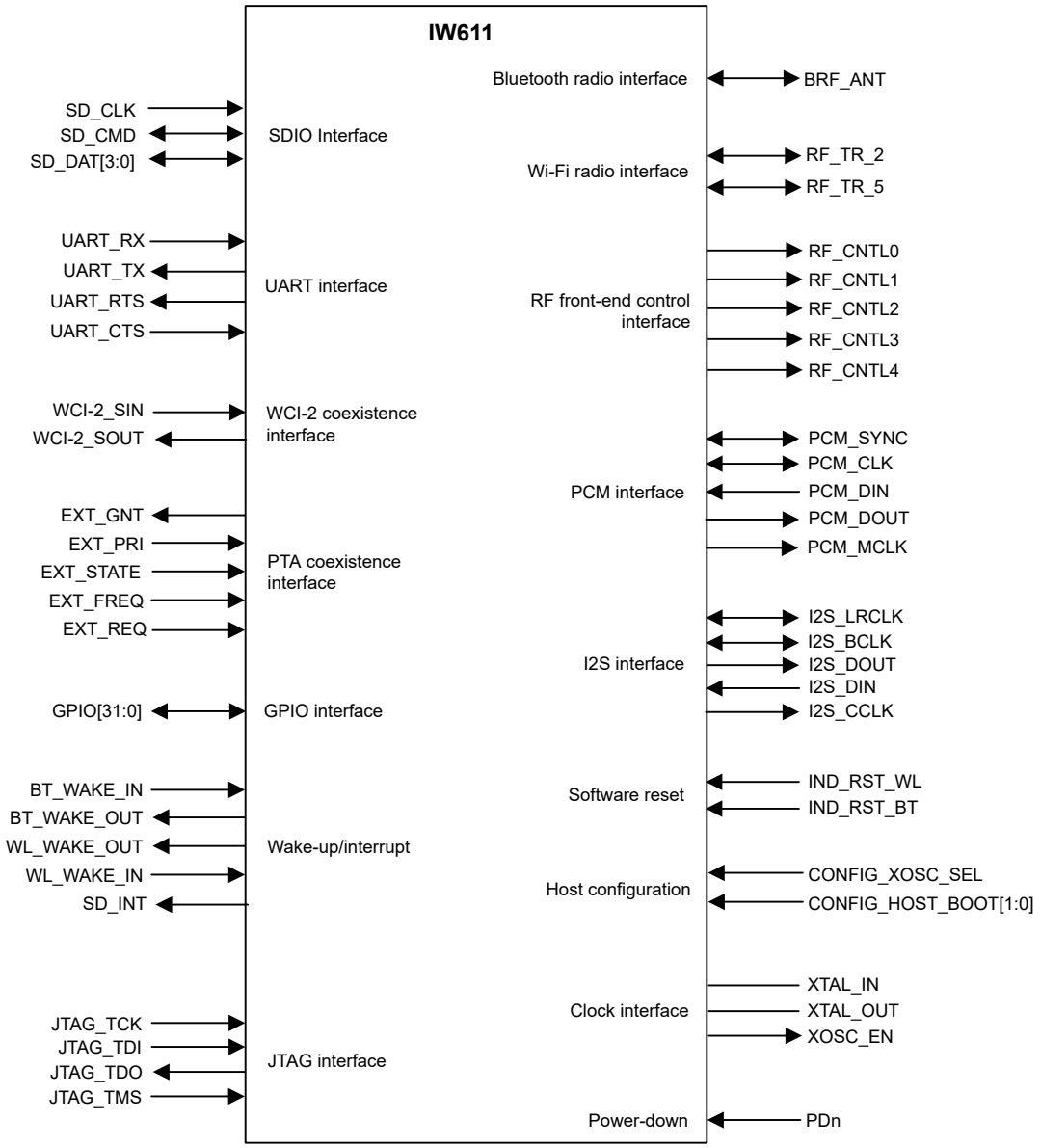

Figure 14. IW611 signal diagram

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6.2 Pin assignment - HVQFN package

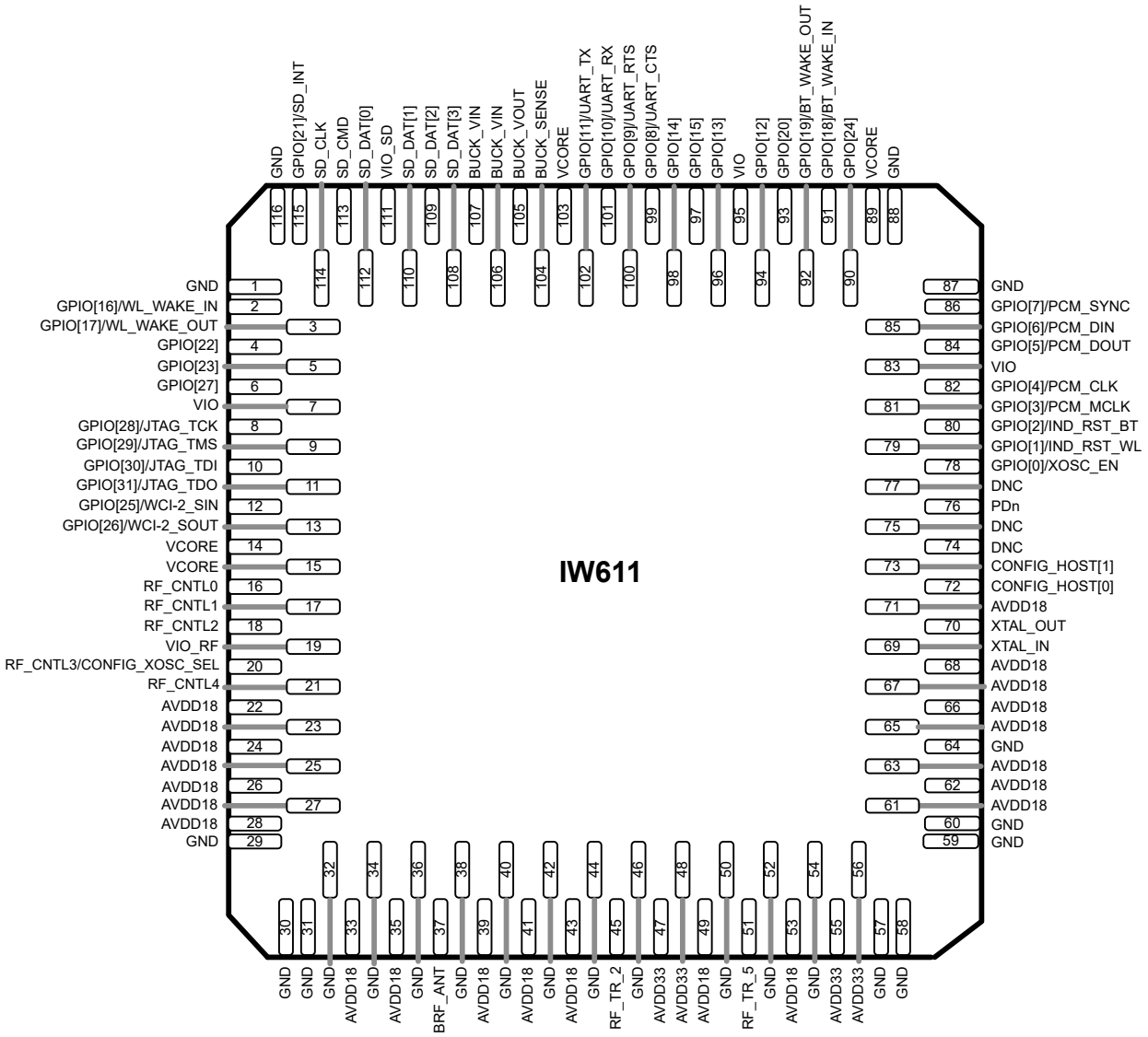

Figure 15. IW611 pin assignment - HVQFN116 package

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6.3 Pin list – HVQFN package

Table 5. Pin list by number

Pin number	Pin name	Power	Type
1	GND	—	Power
2	GPIO[16]/WL_WAKE_IN	VIO	I/O
3	GPIO[17]/WL_WAKE_OUT	VIO	I/O
4	GPIO[22]	VIO	I/O
5	GPIO[23]	VIO	I/O
6	GPIO[27]	VIO	I/O
7	VIO	—	Power
8	GPIO[28]/JTAG_TCK	VIO	I/O
9	GPIO[29]/JTAG_TMS	VIO	I/O
10	GPIO[30]/JTAG_TDI	VIO	I/O
11	GPIO[31]/JTAG_TDO	VIO	I/O
12	GPIO[25]/WCI-2_SIN	VIO	I/O
13	GPIO[26]/WCI-2_SOUT	VIO	I/O
14	VCORE	—	Power
15	VCORE	—	Power
16	RF_CNTL0	VIO_RF	O
17	RF_CNTL1	VIO_RF	O
18	RF_CNTL2	VIO_RF	O
19	VIO_RF	—	Power
20	RF_CNTL3/CONFIG_XOSC_SEL	VIO_RF	I/O
21	RF_CNTL4	VIO_RF	I/O
22	AVDD18	—	Power
23	AVDD18	—	Power
24	AVDD18	—	Power
25	AVDD18	—	Power
26	AVDD18	—	Power
27	AVDD18	—	Power
28	AVDD18	—	Power
29	GND	—	Power
30	GND	—	Power
31	GND	—	Power
32	GND	—	Power
33	AVDD18	—	Power
34	GND	—	Power
35	AVDD18	—	Power

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Table 5. Pin list by number...*continued*

Pin number	Pin name	Power	Type
36	GND	—	Power
37	BRF_ANT	—	A, I/O
38	GND	—	Power
39	AVDD18	—	Power
40	GND	—	Power
41	AVDD18	—	Power
42	GND	—	Power
43	AVDD18	—	Power
44	GND	—	Power
45	RF_TR_2	—	A, I/O
46	GND	—	Power
47	AVDD33	—	Power
48	AVDD33	—	Power
49	AVDD18	—	Power
50	GND	—	Power
51	RF_TR_5	—	A, I/O
52	GND	—	Power
53	AVDD18	—	Power
54	GND	—	Power
55	AVDD33	—	Power
56	AVDD33	—	Power
57	GND	—	Power
58	GND	—	Power
59	GND	—	Power
60	GND	—	Power
61	AVDD18	—	Power
62	AVDD18	—	Power
63	AVDD18	—	Power
64	GND	—	Power
65	AVDD18	—	Power
66	AVDD18	—	Power
67	AVDD18	—	Power
68	AVDD18	—	Power
69	XTAL_IN	AVDD18	A, I
70	XTAL_OUT	AVDD18	A, O
71	AVDD18	—	Power

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Table 5. Pin list by number...*continued*

Pin number	Pin name	Power	Type
72	CONFIG_HOST_BOOT[0]	AVDD18	I
73	CONFIG_HOST_BOOT[1]	AVDD18	I
74	DNC	—	Do not connect
75	DNC	—	Do not connect
76	PDn	AVDD18	I
77	DNC	—	Do not connect
78	GPIO[0]/XOSC_EN	VIO	I/O
79	GPIO[1]/IND_RST_WL	VIO	I/O
80	GPIO[2]/IND_RST_BT	VIO	I/O
81	GPIO[3]/PCM_MCLK	VIO	I/O
82	GPIO[4]/PCM_CLK	VIO	I/O
83	VIO	—	Power
84	GPIO[5]/PCM_DOUT	VIO	I/O
85	GPIO[6]/PCM_DIN	VIO	I/O
86	GPIO[7]/PCM_SYNC	VIO	I/O
87	GND	—	Power
88	GND	—	Power
89	VCORE	—	Power
90	GPIO[24]	VIO	I/O
91	GPIO[18]/BT_WAKE_IN	VIO	I/O
92	GPIO[19]/BT_WAKE_OUT	VIO	I/O
93	GPIO[20]	VIO	I/O
94	GPIO[12]	VIO	I/O
95	VIO	—	Power
96	GPIO[13]	VIO	I/O
97	GPIO[15]	VIO	I/O
98	GPIO[14]	VIO	I/O
99	GPIO[8]/UART_CTS	VIO	I/O
100	GPIO[9]/UART_RTS	VIO	I/O
101	GPIO[10]/UART_RX	VIO	I/O
102	GPIO[11]/UART_TX	VIO	I/O
103	VCORE	—	Power
104	BUCK_SENSE	—	Power
105	BUCK_VOUT	—	Power
106	BUCK_VIN	—	Power
107	BUCK_VIN	—	Power

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Table 5. Pin list by number*...continued*

Pin number	Pin name	Power	Type
108	SD_DAT[3]	VIO_SD	I/O
109	SD_DAT[2]	VIO_SD	I/O
110	SD_DAT[1]	VIO_SD	I/O
111	VIO_SD	—	Power
112	SD_DAT[0]	VIO_SD	I/O
113	SD_CMD	VIO_SD	I/O
114	SD_CLK	VIO_SD	I
115	GPIO[21]/SD_INT	VIO	I/O
116	GND	—	Power

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6.4 Bump locations – WLCSP package

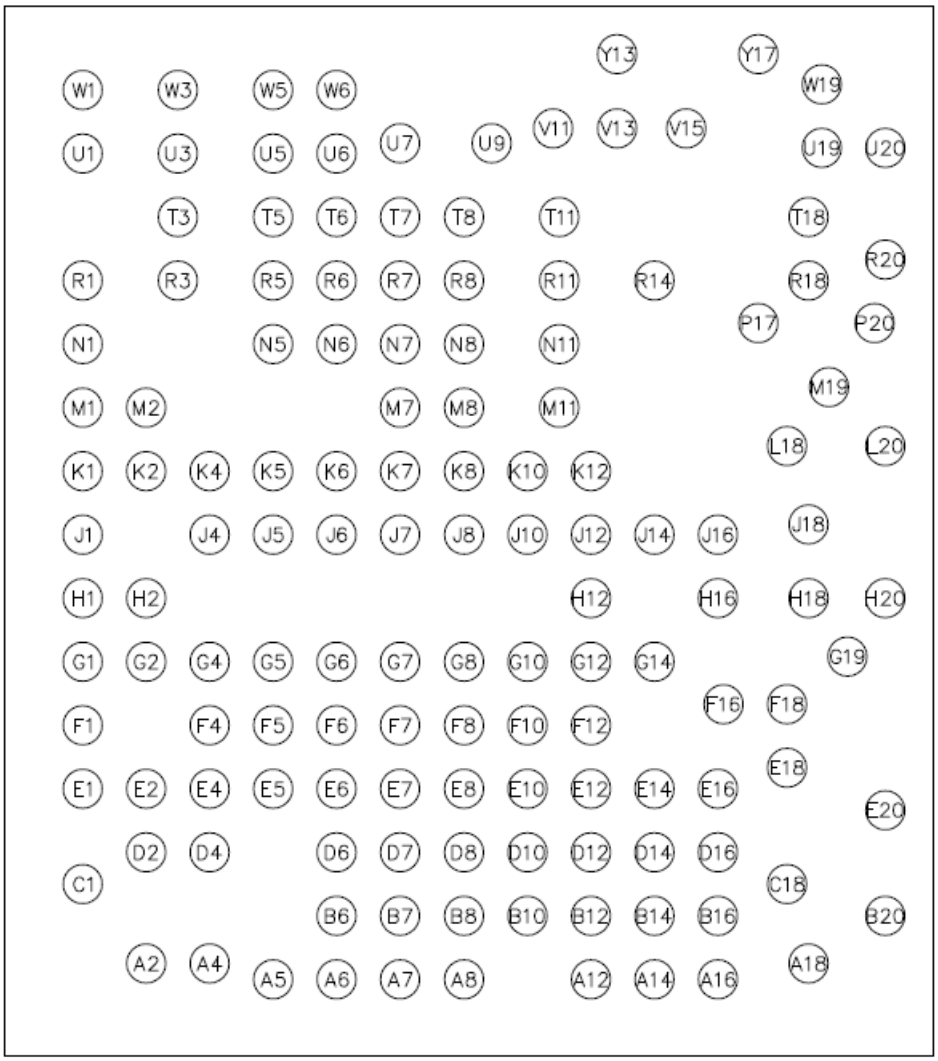

Figure 16. Bump locations – WLCSP package bottom bump view

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6.5 Bump positions relative to die center

Table 6. Bump names and locations on WLCSP140 bottom bump view

Bump count	Alpha-numeric designation	Signal name	Bump location relative to die center (bottom bump view)	
			X (µm)	Y (µm)
1	A2	VIO	-1525.002	-2044.500
2	A4	GPIO[30]/JTAG_TDI	-1225.002	-2044.500
3	A5	GND	-925.001	-2119.500
4	A6	VCORE	-625.001	-2119.500
5	A7	GND	-325.000	-2119.500
6	A8	RF_CNTL0	-24.999	-2119.500
7	A12	AVDD18	575.002	-2119.500
8	A14	AVDD18	875.003	-2119.500
9	A16	AVDD18	1175.003	-2119.500
10	A18	AVDD18	1601.999	-2044.500
11	B6	GPIO[25]/WCI-2_SIN	-625.001	-1819.499
12	B7	GPIO[26]/WCI-2_SOUT	-325.000	-1819.499
13	B8	RF_CNTL1	-24.999	-1819.499
14	B10	VIO_RF	275.001	-1819.499
15	B12	AVDD18	575.002	-1819.499
16	B14	GND	875.003	-1819.499
17	B16	AVDD18	1175.003	-1819.499
18	B20	GND	1965.805	-1819.499
19	C1	VIO_SD	-1825.003	-1669.499
20	C18	GND	1502.004	-1669.499
21	D2	GND	-1525.002	-1519.499
22	D4	SD_CLK	-1225.002	-1519.499
23	D6	GPIO[28]/JTAG_TCK	-625.001	-1519.499
24	D7	GPIO[31]/JTAG_TDO	-325.000	-1519.499
25	D8	RF_CNTL2	-24.999	-1519.499
26	D10	RF_CNTL3/CONFIG_XOSC_SEL	275.001	-1519.499
27	D12	GND	575.002	-1519.499
28	D14	GND	875.003	-1519.499
29	D16	GND	1175.003	-1519.499
30	E1	BUCK_VIN	-1825.003	-1219.498
31	E2	BUCK_VIN	-1525.002	-1219.498
32	E4	SD_DAT[1]	-1225.002	-1219.498

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Table 6. Bump names and locations on WLCSP140 bottom bump view *...continued*

Bump count	Alpha-numeric designation	Signal name	Bump location relative to die center (bottom bump view)	
			X (µm)	Y (µm)
33	E5	SD_CMD	-925.001	-1219.498
34	E6	GPIO[17]/WL_WAKE_OUT	-625.001	-1219.498
35	E7	GPIO[29]/JTAG_TMS	-325.000	-1219.498
36	E8	GND	-24.999	-1219.498
37	E10	RF_CNTL4	275.001	-1219.498
38	E12	GND	575.002	-1219.498
39	E14	GND	875.003	-1219.498
40	E16	GND	1175.003	-1219.498
41	E18	AVDD18	1502.004	-1119.498
42	E20	BRF_ANT	1965.805	-1319.498
43	F1	BUCK_VOUT	-1825.003	-919.498
44	F4	SD_DAT[3]	-1225.002	-919.498
45	F5	GPIO[21]/SD_INT	-925.001	-919.498
46	F6	GPIO[22]	-625.001	-919.498
47	F7	GPIO[23]	-325.000	-919.498
48	F8	VCORE	-24.999	-919.498
49	F10	GND	275.001	-919.498
50	F12	GND	575.002	-919.498
51	F16	GND	1202.003	-819.498
52	F18	GND	1502.004	-819.498
53	G1	GND	-1825.003	-619.497
54	G2	BUCK_VOUT	-1525.002	-619.497
55	G4	SD_DAT[2]	-1225.002	-619.497
56	G5	SD_DAT[0]	-925.001	-619.497
57	G6	GPIO[16]/WL_WAKE_IN	-625.001	-619.497
58	G7	GPIO[27]	-325.000	-619.497
59	G8	VCORE	-24.999	-619.497
60	G10	GND	275.001	-619.497
61	G12	GND	575.002	-619.497
62	G14	GND	875.003	-619.497
63	G19	AVDD18	1785.804	-594.497
64	H1	GND	-1825.003	-319.496
65	H2	BUCK_SENSE	-1525.002	-319.496
66	H12	GND	575.002	-319.496
67	H16	GND	1175.003	-319.496

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Table 6. Bump names and locations on WLCSP140 bottom bump view *...continued*

Bump count	Alpha-numeric designation	Signal name	Bump location relative to die center (bottom bump view)	
			X (µm)	Y (µm)
68	H18	GND	1601.999	-319.496
69	H20	AVDD18	1965.805	-319.496
70	J1	VCORE	-1825.003	-19.496
71	J4	GND	-1225.002	-19.496
72	J5	GPIO[12]	-925.001	-19.496
73	J6	GPIO[15]	-625.001	-19.496
74	J7	GPIO[14]	-325.000	-19.496
75	J8	VCORE	-24.999	-19.496
76	J10	GND	275.001	-19.496
77	J12	GND	575.002	-19.496
78	J14	GND	875.003	-19.496
79	J16	GND	1175.003	-19.496
80	J18	AVDD18	1601.999	30.505
81	K1	GPIO[8]/UART_CTS	-1825.003	280.505
82	K2	GPIO[11]/UART_TX	-1525.002	280.505
83	K4	GPIO[20]	-1225.002	280.505
84	K5	GPIO[24]	-925.001	280.505
85	K6	GPIO[18]/BT_WAKE_IN	-625.001	280.505
86	K7	GPIO[19]/BT_WAKE_OUT	-325.000	280.505
87	K8	VCORE	-24.999	280.505
88	K10	GND	275.001	280.505
89	K12	GND	575.002	280.505
90	L18	GND	1502.004	400.505
91	L20	RF_TR_2	1965.805	400.505
92	M1	GPIO[10]/UART_RX	-1825.003	580.505
93	M2	GPIO[13]	-1525.002	580.505
94	M7	GPIO[6]/PCM_DIN	-325.000	580.505
95	M8	GPIO[7]/PCM_SYNC	-24.999	580.505
96	M11	GND	425.002	580.505
97	M19	GND	1700.000	679.190
98	N1	GPIO[9]/UART_RTS	-1825.003	880.506
99	N5	GPIO[3]/PCM_MCLK	-925.001	880.506
100	N6	GPIO[2]/IND_RST_BT	-625.001	880.506
101	N7	GND	-325	880.506
102	N8	GPIO[5]/PCM_DOUT	-24.999	880.506

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Table 6. Bump names and locations on WLCSP140 bottom bump view *...continued*

Bump count	Alpha-numeric designation	Signal name	Bump location relative to die center (bottom bump view)	
			X (µm)	Y (µm)
103	N11	GND	425.002	880.506
104	P17	GND	1367.003	980.506
105	P20	AVDD33	1915.805	980.506
106	R1	VIO	-1825.003	1180.507
107	R3	GND	-1375.002	1180.507
108	R5	DNC	-925.001	1180.507
109	R6	CONFIG_HOST[1]	-625.001	1180.507
110	R7	PDn	-325.000	1180.507
111	R8	GPIO[1]/IND_RST_WL	-24.999	1180.507
112	R11	GND	425.002	1180.507
113	R14	GND	875.003	1180.507
114	R18	GND	1601.999	1180.507
115	R20	AVDD18	1965.805	1280.507
116	T3	GPIO[4]/PCM_CLK	-1375.002	1480.507
117	T5	AVDD18	-925.001	1480.507
118	T6	GND	-625.001	1480.507
119	T7	CONFIG_HOST[0]	-325.000	1480.507
120	T8	DNC	-24.999	1480.507
121	T11	GND	425.002	1480.507
122	T18	GND	1601.999	1480.507
123	U1	VIO	-1825.003	1780.508
124	U3	GPIO[0]/XOSC_EN	-1375.002	1780.508
125	U5	XTAL_OUT	-925.001	1780.508
126	U6	GND	-625.001	1780.508
127	U7	GND	-325.000	1830.508
128	U9	AVDD18	106.001	1830.508
129	U19	GND	1665.805	1807.030
130	U20	RF_TR_5	1965.805	1807.030
131	V11	GND	398.002	1900.508
132	V13	GND	698.002	1900.508
133	V15	GND	1025.003	1900.508
134	W1	VIO	-1825.003	2080.508
135	W3	DNC	-1375.002	2080.508
136	W5	XTAL_IN	-925.001	2080.508
137	W6	AVDD18	-625.001	2080.508

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Table 6. Bump names and locations on WLCSP140 bottom bump view *...continued*

Bump count	Alpha-numeric designation	Signal name	Bump location relative to die center (bottom bump view)	
			X (µm)	Y (µm)
138	W19	AVDD33	1665.805	2107.031
139	Y13	AVDD18	698.002	2250.000
140	Y17	AVDD18	1367.003	2250.000

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6.6 Pin types

Table 7. Pin types

Pin type	Description
I/O	Digital input/output
I	Digital input
O	Digital output
A, I	Analog input
A, O	Analog output
A, I/O	Analog input/output
NC	No connect
DNC	Do not connect
Power	Power
Ground	Ground

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6.7 Pin description

6.7.1 Pin states

The pin states information provided in the tables includes:

- **No Pad Power State** indicates the state when there is no power
- **PwrDwn State** denotes the power-down state in default configuration. Many pads have programmable power-down values, which can be set by firmware.
- **Reset State** is the state after the power-on-reset state and before the hardware state (HW State)
- **HW State** (hardware state) is the state after boot code finishes and before firmware download begins (firmware may change the pin state). HW State may differ based on the pin muxing/strap setting. For example, for UART_RTSn and UART_SOUT, the boot code will enable the UART interface when the device is in SDIO-UARTmode, making the HW states output high and output low, respectively.
- **PwrDwn Prog** indicates if the power-down state can be programmed
- **Internal PU/PD** columns indicates the following:
  - Type of PU/PD (weak vs nominal)
  - The polarity (PU vs. PD)

  The internal pull-up or pull-down applies when the pin is in input mode
- **PU** denotes whether the pull-up can be programmed or not
- **PD** denotes whether the pull-down can be programmed or not
- Pull-up and pull-down are only effective when the pad is in input mode
- After firmware is downloaded, the pads (GPIO, RF control, and so on) are programmed in functional mode per the functionality of the pins

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6.7.2 General purpose I/O (GPIO) (MFP)

Table 8. General purpose I/O (MFP)

Pins may be Multi-Functional Pins (MFP).

Pin name	Supply	No pad power state[1]	Reset state	HW state	PwrDwn state	PwrDwn prog.	Internal PU/PD	PU	PD
GPIO[31]/JTAG_TDO	VIO	tristate	input	input	tristate	yes	weak PU	yes	yes
GPIO mode: GPIO[31] (input/output) **JTAG mode:** JTAG_TDO - JTAG test data signal (output). See Section 6.7.17 "JTAG interface".									
GPIO[30]/JTAG_TDI	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[30] (input/output) **JTAG mode:** JTAG_TDI - JTAG test data signal (input). See Section 6.7.17 "JTAG interface".									
GPIO[29]/JTAG_TMS	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[29] (input/output) **JTAG mode:** JTAG_TMS - JTAG controller select (input). See Section 6.7.17 "JTAG interface".									
GPIO[28]/JTAG_TCK	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[28] (input/output) **JTAG mode:** JTAG_TCK - JTAG test clock signal (input). See Section 6.7.17 "JTAG interface".									
GPIO[27]	VIO	tristate	input	input	tristate	yes	weak PU	yes	yes
GPIO mode: GPIO[27] (input/output) **BLE ISOC trigger mode**: BLE_HOST_TRIG2 - Host_Trigger pin 2 (input/output) for Bluetooth LE and host									
GPIO[26]/WCI-2_SOUT	VIO	tristate	input	input	drive low	yes	nominal PU	yes	yes
GPIO mode: GPIO[26] (input/output) **WCI-2 coexistence mode**: WCI-2_SOUT - Transmit signal to external radio (output). See Section 6.7.10 "WCI-2 coexistence interface".									
GPIO[25]/WCI-2_SIN	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[25] (input/output) **WCI-2 coexistence mode**: WCI-2_SIN - Receive signal from external radio (input). See Section 6.7.10 "WCI-2 coexistence interface".									
GPIO[24]	VIO	tristate	output low	output high	tristate	yes	weak PU	yes	yes
GPIO mode: GPIO[24] (input/output)									
GPIO[23]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[23] (input/output) **BLE ISOC trigger mode**: BLE_HOST_TRIG1 - Host_Trigger pin 1 (input/output) for Bluetooth LE and host									
GPIO[22]	VIO	tristate	output high	output low	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[22] (input/output)									

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Table 8. General purpose I/O (MFP)*...continued*

Pins may be Multi-Functional Pins (MFP).

Pin name	Supply	No pad power state[1]	Reset state	HW state	PwrDwn state	PwrDwn prog.	Internal PU/PD	PU	PD
GPIO[21]/SD_INT	VIO	tristate	output high	output low	drive low	yes	nominal PU	yes	yes
GPIO mode: GPIO[21] (input/output) **SDIO mode**: SD_INT - SDIO interrupt signal (output). See Section 6.7.12 "Wake-up/interrupt".									
GPIO[20]	VIO	tristate	input	input	drive low	yes	nominal PU	yes	yes
GPIO mode: GPIO[20] (input/output) **PTA coexistence mode**: EXT_FREQ - External radio frequency input signal. See Section 6.7.9 "PTA coexistence interface ".									
GPIO[19]	VIO	tristate	input	input	drive low	yes	nominal PU	yes	yes
GPIO mode: GPIO[19] (input/output) **Wake-up/interrupt mode**: BT_WAKE_OUT - Bluetooth wake-up signal (output). See Section 6.7.12 "Wake-up/interrupt".									
GPIO[18]/BT_WAKE_IN	VIO	tristate	input	input	tristate	yes	weak PU	yes	yes
GPIO mode: GPIO[18] (input/output) **Wake-up/interrupt mode**: BT_WAKE_IN - Bluetooth wake-up signal (input). See Section 6.7.12 "Wake-up/interrupt".									
GPIO[17]/WL_WAKE_OUT	VIO	tristate	input	input	drive low	yes	nominal PU	yes	yes
GPIO mode: GPIO[17] (input/output) **Wake-up/interrupt mode**: WL_WAKE_OUT - Wi-Fi radio wake-up signal (output). See Section 6.7.12 "Wake-up/interrupt".									
GPIO[16]/WL_WAKE_IN	VIO	tristate	input	input	tristate	yes	weak PU	yes	yes
GPIO mode: GPIO[16] (input/output) **Wake-up/interrupt mode**: WL_WAKE_IN - Wi-Fi radio wake-up signal (input). See Section 6.7.12 "Wake-up/interrupt".									
GPIO[15]	VIO	tristate	output low	output low	drive low	yes	nominal PU	yes	yes
GPIO mode: GPIO[15] (input/output) **PTA coexistence mode**: EXT_PRI - External radio priority input signal. See Section 6.7.9 "PTA coexistence interface ".									
GPIO[14]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[14] (input/output) **PTA coexistence mode**: EXT_GNT - External radio grant output signal. See Section 6.7.9 "PTA coexistence interface ".									
GPIO[13]	VIO	tristate	input	input	drive high	yes	nominal PU	yes	yes
GPIO mode: GPIO[13] (input/output) **PTA coexistence mode**: EXT_REQ - External radio request input signal. See Section 6.7.9 "PTA coexistence interface ".									
GPIO[12]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[12] (input/output) **PTA coexistence mode**: EXT_STATE - External radio state input signal. See Section 6.7.9 "PTA coexistence interface ".									

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Table 8. General purpose I/O (MFP)*...continued*

Pins may be Multi-Functional Pins (MFP).

Pin name	Supply	No pad power state[1]	Reset state	HW state	PwrDwn state	PwrDwn prog.	Internal PU/PD	PU	PD
GPIO[11]/UART_TX	VIO	tristate	output high	output high	drive low	yes	nominal PU	yes	yes
GPIO mode: GPIO[11] (input/output) **UART interface mode**: UART_TX - UART serial output signal. See Section 6.7.7 "UART host interface".									
GPIO[10]/UART_RX	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[10] (input/output) **UART interface mode**: UART_RX - UART serial input signal. See Section 6.7.7 "UART host interface".									
GPIO[9]/UART_RTS	VIO	tristate	output high	output high	drive high	yes	nominal PU	yes	yes
GPIO mode: GPIO[9] (input/output) **UART interface mode**: UART_RTS - UART request-to-send output signal (active low). See Section 6.7.7 "UART host interface".									
GPIO[8]/UART_CTS	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[8] (input/output) **UART interface mode**: UART_CTS - UART clear-to-send input signal (active low). See Section 6.7.7 "UART host interface".									
GPIO[7]/PCM_SYNC	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[7] (input/output) **Bluetooth PCM mode**: PCM_SYNC - PCM frame sync (output if master, input if slave). See Section 6.7.8 "Digital audio interface". **Bluetooth I2S mode**: I2S_LRCLK - I2S left/right clock (output if master, input if slave). See Section 6.7.8 "Digital audio interface".									
GPIO[6]/PCM_DIN	VIO	tristate	input	input	tristate	yes	weak PU	yes	yes
GPIO mode: GPIO[6] (input/output) **Bluetooth PCM mode**: PCM_DIN - PCM receive data signal (input). See Section 6.7.8 "Digital audio interface". **Bluetooth I2S mode**: I2S_DIN - I2S receive data signal (input). See Section 6.7.8 "Digital audio interface".									
GPIO[5]/PCM_DOUT	VIO	tristate	input	input	tristate	yes	weak PU	yes	yes
GPIO mode: GPIO[5] (input/output) **Bluetooth PCM mode**: PCM_DOUT - PCM transmit data signal (output). See Section 6.7.8 "Digital audio interface". **Bluetooth I2S mode**: I2S_DOUT - I2S transmit data signal (output). See Section 6.7.8 "Digital audio interface".									
GPIO[4]/PCM_CLK	VIO	tristate	input	input	tristate	yes	weak PU	yes	yes
GPIO mode: GPIO[4] (input/output) **Bluetooth PCM mode**: PCM_CLK - PCM data clock (output if master, input if slave). See Section 6.7.8 "Digital audio interface". **Bluetooth I2S mode**: I2S_BCLK - I2S bit clock (output if master, input if slave). See Section 6.7.8 "Digital audio interface".									

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Table 8. General purpose I/O (MFP)*...continued*

Pins may be Multi-Functional Pins (MFP).

Pin name	Supply	No pad power state[1]	Reset state	HW state	PwrDwn state	PwrDwn prog.	Internal PU/PD	PU	PD
GPIO[3]/PCM_MCLK	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[3] (input/output) **Bluetooth PCM mode**: PCM_MCLK - PCM clock output signal (optional). See Section 6.7.8 "Digital audio interface". **Bluetooth I2S mode**: I2S_CCLK - I2S clock output signal (optional). See Section 6.7.8 "Digital audio interface".									
GPIO[2]/IND_RST_BT	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[2] (input/output) **Software reset mode**: IND_RST_BT - Independent software reset for Bluetooth (input). See Section 6.7.13 "Software reset ".									
GPIO[1]/IND_RST_WL	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO mode: GPIO[1] (input/output) **Software reset mode**: IND_RST_WL - Independent software reset for Wi-Fi (input). See Section 6.7.13 "Software reset ".									
GPIO[0]/XOSC_EN	VIO	tristate	output high	output high	drive low	yes	nominal PU	yes	yes
GPIO mode: GPIO[0] (input/output) **Oscillator enable mode**: XOSC_EN - Oscillator enable (output). See Section 6.7.14 "Clock interface"									

[1] Maximum input voltage is 0.4V when VIO has no power (or in uncertain situations).

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6.7.3 RF front-end control interface

Note: *This interface is used to control RF front-end components such as switches or FEMs.*

Table 9. RF front-end control interface[1]

Pin name	Supply	No pad power state	Reset state	HW state	PwrDwn state	PwrDwn prog.	Internal PU/ PD	PU	PD
RF_CNTL0	VIO_RF	tristate	output low	output low	drive low	yes	nominal PU	no	no
RF control 0 — RF control line 0									
RF_CNTL1	VIO_RF	tristate	output high	output high	drive high	yes	weak PU	no	no
RF control 1 — RF control line 1									
RF_CNTL2	VIO_RF	tristate	output low	output low	drive low	yes	nominal PU	no	no
RF control 2 — RF control line 2									
RF_CNTL3/ CONFIG_ XOSC_SEL	VIO_RF	tristate	input	input	drive high	yes	weak PU	no	no
RF control 3 — RF control line 3 CONFIG_XOSC_SEL: see Section 6.8 "Configuration pins"									
RF_CNTL4	VIO_RF	tristate	input	input	drive low	yes	weak PU	no	no
RF control 4 — RF control line 4									

[1] Maximum input voltage is 0.4V when VIO_RF has no power (or in uncertain situations).

6.7.4 Wi-Fi radio interface

Table 10. Wi-Fi radio interface

Pin name	Type	Supply	Description
RF_TR_2	A, I/O	AVDD18	Wi-Fi transmit/receive (2.4 GHz)
RF_TR_5	A, I/O	AVDD18	Wi-Fi transmit/receive (5 GHz)

6.7.5 Bluetooth radio interface

Table 11. Bluetooth radio interface

Pin name	Type	Supply	Description
BRF_ANT	A, I/O	AVDD18	Bluetooth radio transmit/receive interface

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6.7.6 SDIO host interface

Table 12. SDIO host interface (MFP)

Pins may be Multi-Functional Pins (MFP).

Pin name	Supply	No pad power state[1]	Reset state	HW state	PwrDwn state	PwrDwn prog.	Internal PU/PD	PU	PD
SD_CLK	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit mode: Clock input **SDIO 1-bit mode**: Clock input									
SD_CMD	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit mode: Command/response (input/output) **SDIO 1-bit mode**: Command line (input/output)									
SD_DAT[3]	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit mode: Data line bit[3] **SDIO 1-bit mode**: Reserved									
SD_DAT[2]	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit mode: Data line bit[2] or read wait (optional) **SDIO 1-bit mode**: Read wait (optional)									
SD_DAT[1]	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit mode: Data line bit[1] **SDIO 1-bit mode**: Interrupt									
SD_DAT[0]	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit mode: Data line bit[0] **SDIO 1-bit mode**: Data line									

[1] Maximum input voltage is 0.4V when VIO_SD has no power (or in uncertain situations).

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6.7.7 UART host interface

Table 13. UART host interface (MFP)

Pins may be Multi-Functional Pins (MFP).

Pin name	Type	Supply	Description
UART_RX	I	VIO	UART serial input signal Multi-functional pin: GPIO[10] input/output
UART_TX	O	VIO	UART serial output signal Multi-functional pin: GPIO[11] input/output
UART_RTS	O	VIO	UART request-to-send output signal Multi-functional pin: GPIO[9] input/output
UART_CTS	I	VIO	UART clear-to-send input signal Multi-functional pin: GPIO[8] input/output

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6.7.8 Digital audio interface

Table 14. Audio interface pins

Pins may be Multi-Functional Pins (MFP). See pin descriptions for functional modes.

Pin Name	Type	Supply	Description
PCM_DIN	I	VIO	PCM audio codec output data (for recording). GPIO[6] input/output
PCM_DOUT	O	VIO	PCM audio codec input data (for playback). GPIO[5] input/output
PCM_SYNC	I/O	VIO	PCM sync pulse signal. GPIO[7] input/output . Central mode: output . Peripheral mode: input
PCM_CLK	I/O	VIO	PCM clock signal. GPIO[4] input/output . Central mode: output . Peripheral mode: input
PCM_MCLK	I/O	VIO	PCM codec main clock signal (optional). GPIO[3] input/output Optional clock used for some codecs. Derived from PCM_CLK.
I2S_CCLK	O	VIO	I2S codec main clock signal (optional). GPIO[3] input/output Optional clock used for some codecs. Derived from I2S_BCLK.
I2S_DIN	I	VIO	I2S audio codec output data (for recording). GPIO[6] input/output
I2S_DOUT	O	VIO	I2S audio codec input data (for playback). GPIO[5] input/output
I2S_BCLK	I/O	VIO	I2S audio bit clock. GPIO[4] input/output . Central mode: output . Peripheral mode: input
I2S_LRCLK	I/O	VIO	I2S audio left-right clock. GPIO[7] input/output . Central mode: output . Peripheral mode: input

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6.7.9 PTA coexistence interface

Table 15. PTA coexistence interface (MFP)

Pins may be Multi-Functional Pins (MFP). See pin descriptions for functional modes.

Pin Name	Type	Supply	Description
EXT_STATE	I	VIO	External radio state input signal - muxed with GPIO[12] External radio traffic direction (TX/RX): • 1: Tx • 0: rx
EXT_GNT	O	VIO	External radio grant output signal - muxed with GPIO[14]
EXT_FREQ	I	VIO	External radio frequency input signal - muxed with GPIO[20] Frequency overlap between external radio and Wi-Fi : • 1: overlap • 0: non-overlap This signal is useful when the external radio is a frequency hopping device.
EXT_PRI	I	VIO	External radio input priority signal - muxed with GPIO[15] Priority of the request from the external radio. Can support 1 bit priority (sample once) and 2 bit priority (sample twice). Can also have Tx/Rx info following the priority info if EXT_STATE is not used.
EXT_REQ	I	VIO	Request from the external radio - muxed with GPIO[13]

6.7.10 WCI-2 coexistence interface

Table 16. WCI-2 coexistence interface (MFP)

Pins may be Multi-Functional Pins (MFP).

Pin name	Type	Supply	Description
WCI-2_SIN	I	VIO	Input signal from external radio. Multi-functional pin: GPIO[25] input/output
WCI-2_SOUT	O	VIO	Output signal to external radio. Multi-functional pin: GPIO[26] input/output

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6.7.11 Host configuration

Table 17. Host configuration

Pin name	Supply	No pad power state	Reset state	HW state	PwrDwn state	PwrDwn prog.	Internal PU/PD	PU	PD
CONFIG_ HOST_BOOT[0]	AVDD18	tristate	input	input	tristate	no	weak PU	yes	yes
CONFIG_HOST_BOOT[0]: see Section 6.8 "Configuration pins"									
CONFIG_ HOST_BOOT[1]	AVDD18	tristate	input	input	tristate	no	weak PU	yes	yes
CONFIG_HOST_BOOT[1]: see Section 6.8 "Configuration pins"									

6.7.12 Wake-up/interrupt

Table 18. Wake-up/interrupt pins (MFP)

Pins may be Multi-Functional Pins (MFP).

Pin name	Type	Supply	Description
BT_WAKE_OUT	O	VIO	Bluetooth wake-up output signal. Multi-functional pin: GPIO[19] input/output
BT_WAKE_IN	I	VIO	Bluetooth wake-up input signal. Multi-functional pin: GPIO[18] input/output
WL_WAKE_OUT	O	VIO	Wi-Fi radio wake-up output signal. Multi-functional pin: GPIO[17] input/output
WL_WAKE_IN	I	VIO	Wi-Fi radio wake-up input signal. Multi-functional pin: GPIO[16] input/output
SD_INT	O	VIO	SDIO interrupt output signal. Multi-functional pin: GPIO[21] input/output

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6.7.13 Software reset

Table 19. Software reset pins (MFP)

Pins may be Multi-Functional Pins (MFP).

Pin Name	Type	Supply	Description
IND_RST_BT	I	VIO	Independent software reset for Bluetooth Multi-functional pin: GPIO[2] input/output
IND_RST_WL	I	VIO	Independent software reset for Wi-Fi Multi-functional pin: GPIO[1] input/output

6.7.14 Clock interface

Table 20. Clock interface

Pin name	Supply	No pad power state[1]	Reset state	HW state	PwrDwn state	PwrDwn prog.	Internal PU/ PD	PU	PD
XTAL_IN	AVDD18	--	--	--	--	--	--	--	--
Reference clock input. The reference clock signal frequency must be 40 MHz from an external crystal. The power consumption in sleep mode is lower with an external crystal compared to an external crystal oscillator when an external sleep clock is not used.									
XTAL_OUT	AVDD18	--	--	--	--	--	--	--	--
Reference clock output. Connect this pin to an external crystal when an external crystal is used. When an external crystal oscillator is used, connect this pin to ground with resistance less than 100 Ω.									
XOSC_EN	VIO	tristate	output	output high	drive low	yes	nominal PU	yes	yes
Oscillator Enable (output) (active high) Used to enable an external oscillator. XOSC_EN signal can be used ONLY when an external oscillator clock is used. • 0 = disable external oscillator • 1 = enable external oscillator ***Note:*** *Muxed with GPIO[0].*									

[1] Maximum input voltage is 0.4V when VIO has no power (or in uncertain situations).

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6.7.15 Power down pin

Table 21. Power down pin

Pin name	Supply	No pad power state	Reset state	HW state	PwrDwn state	PwrDwn prog.	Internal PU/ PD	PU	PD
PDn	AVDD18	--	--	--	--	--	weak PD	--	--
Full Power-down (input) (active low) 0 = full power-down mode 1 = normal mode • PDn can accept an input of 1.8V to 4.5V • PDn may be driven by the host • PDn must be high for normal operation No internal pull-up on this pin. This pin has an always-on internal weak pull-down.									

6.7.16 Power supply and ground pins

Table 22. Power supply and ground pins

Pin name	Type	Description
VCORE	Power	1.05 V core power supply
VIO	Power	1.8V/3.3V digital I/O power supply
VIO_SD	Power	1.8V/3.3V digital I/O SDIO power supply
VIO_RF	Power	1.8V/3.3V digital I/O RF power supply
AVDD18	Power	1.8V analog power supply
AVDD33	Power	3.3V analog power supply
BUCK_VIN	Power	Internal buck voltage input See Section 7.2 "Internal buck regulator"
BUCK_VOUT	Power	Internal buck voltage output See Section 7.2 "Internal buck regulator"
BUCK_SENSE	Power	Internal buck voltage sense This pin senses the output voltage of the internal Buck.
GND	Ground	Ground
NC	NC	No connect Do not connect these pins. Leave these pins floating.

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6.7.17 JTAG interface

Table 23. JTAG interface pins (MFP)

Pins may be Multi-Functional Pins (MFP).

Pin Name	Type	Supply	Description
JTAG_TDO	O	VIO	JTAG test data output signal. GPIO[31] input/output
JTAG_TDI	I	VIO	JTAG test data input signal. GPIO[30] input/output
JTAG_TMS	I	VIO	JTAG test mode select input signal. GPIO[29] input/output
JTAG_TCK	I	VIO	JTAG test clock input signal. GPIO[28] input/output

6.8 Configuration pins

The following table shows the pins used as configuration inputs to set parameters following a reset. The definition of these pins changes immediately after reset to their usual function.

To set a configuration bit to 0, attach a 51 kΩ resistor from the pin to ground. No external circuitry is required to set a configuration bit to 1.

Table 24. Configuration pins

Configuration bits	Pin name	Configuration function
CON[7]	RF_CNTL4	Reserved. Set to 1.
CON[5]	RF_CNTL3/CONFIG_XOSC_SEL	Reference clock frequency select 1 = 40 MHz
CON[1:0]	CONFIG_HOST_BOOT[1:0]	Host configuration options. Selects the host interface used for Wi-Fi and Bluetooth. 11 = (default). See the table below.

Table 25. Host configuration options

CONFIG_HOST[1:0]	Wi-Fi	Bluetooth/Bluetooth LE
11	SDIO	UART
Others	Reserved	Reserved

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7 Power information

7.1 Power-up sequence

The IW611 does not have power-up sequence requirements. The power-down pin (PDn) must be held low (asserted) until all external clock and power supply rails are stable. See Figure 17.

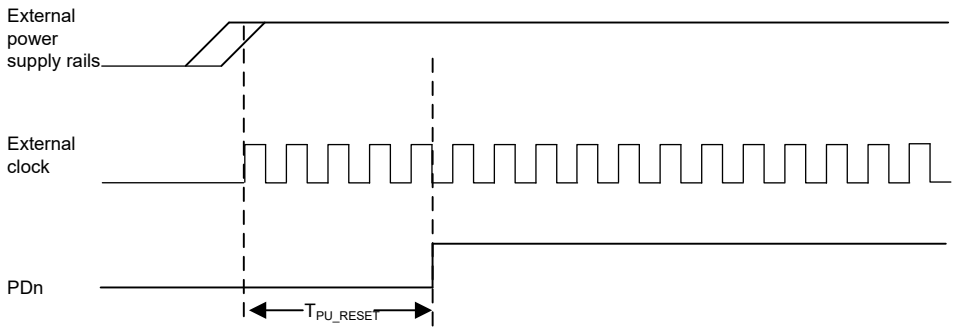

Figure 17. PDn held low (asserted) [1]

[1] T_{PU_RESET} is defined in Section 11.9.1.

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7.2 Internal buck regulator

VCORE pins must be supplied by the internal Buck regulator. The following figure shows the application circuit for VCORE supply using the internal Buck regulator. The power inductor in the application is chosen to maximize the internal Buck efficiency.

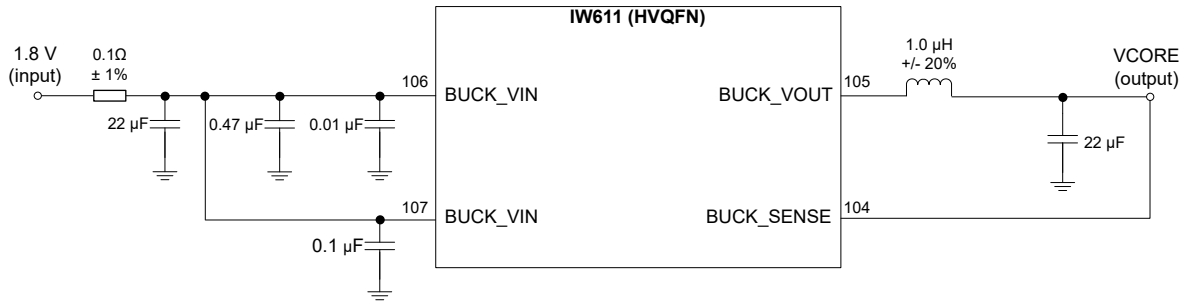

Figure 18. Internal buck connections - HVQFN package

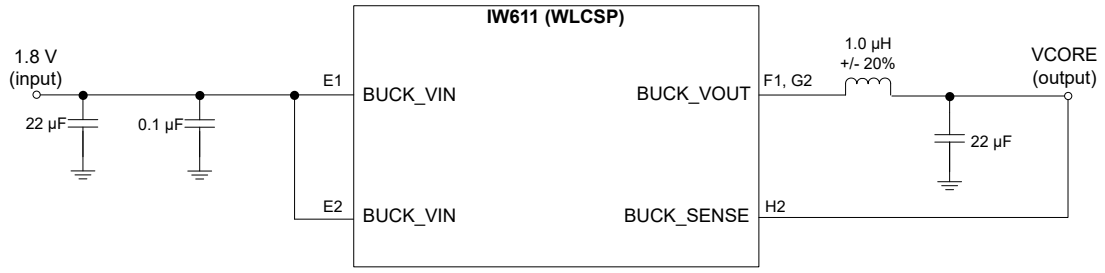

Figure 19. Internal buck connections - WLCSP package

Deep-sleep mode

When the internal Buck is used to supply VCORE, the VCORE level can be reduced to approximately 0.8 V to reduce power consumption in deep sleep mode.

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8 Absolute maximum ratings

CAUTION: The absolute maximum ratings table defines the limitations for electrical and thermal stresses. These limits prevent permanent damage to the device. Exposure to conditions at or beyond these ratings is not guaranteed and can damage the device.

Table 26. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
VCORE[1]	1.05 V core power supply	—	1.21	V
VIO	1.8 V/3.3 V digital I/O power supply	—	2.16	V
		—	3.96	V
VIO_SD	1.8 V/3.3 V digital I/O power supply	—	2.16	V
		—	3.96	V
VIO_RF	1.8 V/3.3 V digital I/O power supply	—	2.16	V
		—	3.96	V
AVDD18	1.8 V analog power supply	—	2.16	V
AVDD33	3.3 V analog power supply	—	3.96	V
BUCK_VIN	Buck input power supply	—	2.16	V
$T_{STORAGE}$	Storage Temperature	-55	+125	°C

[1] VCORE must be powered from the internal buck as illustrated in Section 7.2 "Internal buck regulator"

Table 27. Limiting values

Symbol	Parameter	Condition	Min	Max	Unit
V_{ESD}	Electrostatic discharge	human body model (HBM)[1]	-2	+2	kV
		charged device model (CDM)[2]	-500	+500	V

[1] According to ANSI/ESDA/JEDEC JS-001.
[2] According to ANSI/ESDA/JEDEC JS-002

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9 Recommended operating conditions

Note: *Operation beyond the recommended operating conditions is neither recommended nor guaranteed.*

Table 28. Recommended operating conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCORE [1]	1.05 V core power supply	—	0.99	1.05	1.155	V
VIO	1.8V/3.3V digital I/O power supply	—	1.71	1.8	1.89	V
			3.14	3.3	3.46	V
VIO_SD	1.8V/3.3V digital I/O SDIO power supply	—	1.71	1.8	1.89	V
			3.14	3.3	3.46	V
VIO_RF	1.8V/3.3V digital I/O power supply	—	1.71	1.8	1.89	V
			3.14	3.3	3.46	V
AVDD18	1.8V analog power supply	—	1.71	1.8	1.89	V
AVDD33	3.3V analog power supply	—	3.14	3.3	3.46	V
BUCK_VIN	Buck input power supply	—	1.71	1.8	1.89	V
T_A	Ambient operating temperature	Commercial	0	—	70	°C
		Industrial	-40	—	85	°C
T_J	Maximum junction temperature	—	—	—	125	°C

[1] VCORE must be powered by the internal Buck as illustrated in Section 7.2 "Internal buck regulator".

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10 Radio specifications

10.1 Wi-Fi radio specifications

10.1.1 Wi-Fi radio performance measurement

The Wi-Fi transmit/receive performance is measured either at the antenna port or at the chip port with Wi-Fi radio interface pins. In Figure 20, the Wireless SoC is IW611.

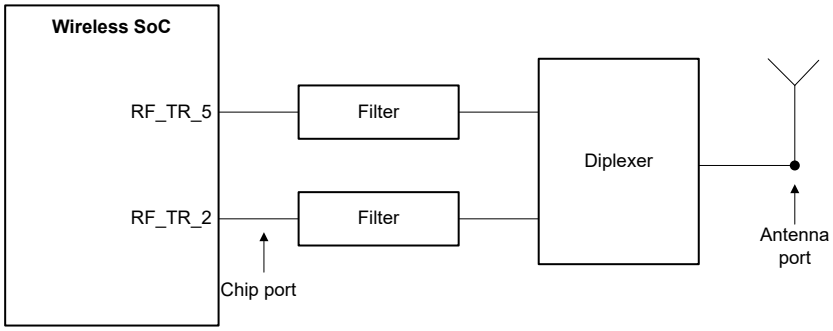

Figure 20. RF performance measurement points

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10.1.2 2.4 GHz Wi-Fi receiver performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at RF_TR_2 pin.*

Table 29. 2.4 GHz Wi-Fi receiver performance

Parameter	Condition	Min	Typ	Max	Unit
RF frequency range	2.4 GHz	2400	—	2483.5	MHz
Rx input IP3 at RF high gain (in-band)	Rx input IP3 when LNA in high gain mode at chip input	—	-15	—	dBm
Receiver sensitivity					
Receiver sensitivity 802.11b	20 MHz 1 Mbps	—	-99.5	—	dBm
Receiver sensitivity 802.11b	20 MHz 11 Mbps	--	-91.2	--	dBm
Receiver sensitivity 802.11g	20 MHz 6 Mbps	—	-94.2	—	dBm
Receiver sensitivity 802.11g	20 MHz 54 Mbps	—	-77.5	—	dBm
Receiver sensitivity 802.11n	20 MHz MCS0 Nss1 BCC	—	-93.5	—	dBm
Receiver sensitivity 802.11n	20 MHz MCS7 Nss1 BCC	—	-74.2	—	dBm
Receiver sensitivity 802.11n	40 MHz MCS0 Nss1 BCC	—	-90.5	—	dBm
Receiver sensitivity 802.11n	40 MHz MCS7 Nss1 BCC	—	-71.5	—	dBm
Receiver sensitivity 802.11ax	20 MHz MCS0 Nss1 LDPC[1]	—	-93.9	—	dBm
Receiver sensitivity 802.11ax	20 MHz MCS11 Nss1 LDPC[1]	—	-64.5	—	dBm
Receiver sensitivity 802.11ax	40 MHz MCS0 Nss1 LDPC[1]	—	-90.5	—	dBm
Receiver sensitivity 802.11ax	40 MHz MCS11 Nss1 LDPC[1]	—	-62.5	—	dBm
Receiver maximum input level (MIL)					
Receiver maximum input level DSSS[2]	802.11b DSSS MIL	—	0.47	—	dBm
Receiver maximum input level DSSS[2]	802.11b CCK MIL	—	0.47	—	dBm
Receiver maximum input level OFDM	OFDM MIL	—	-9.7	—	dBm
Receiver adjacent channel interference (ACI)					
Receiver ACI 802.11b	20 MHz 1 Mbps	—	53	—	dB
Receiver ACI 802.11b	20 MHz 11 Mbps	—	47.7	—	dB
Receiver ACI 802.11g	20 MHz 6 Mbps	—	30.3	—	dB
Receiver ACI 802.11g	20 MHz 54 Mbps	—	27.3	—	dB
Receiver ACI 802.11n	20 MHz MCS0 Nss1 BCC	—	41	—	dB
Receiver ACI 802.11n	20 MHz MCS7 Nss1 BCC	—	27.3	—	dB
Receiver ACI 802.11ax	20 MHz MCS0 Nss1 LDPC[1]	—	30.3	—	dB
Receiver ACI 802.11ax	20 MHz MCS11 Nss1 LDPC[1]	—	7	—	dB

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Table 29. 2.4 GHz Wi-Fi receiver performance*...continued*

Parameter	Condition	Min	Typ	Max	Unit
Receiver alternate adjacent channel interference (AACI)					
Receiver AACI 802.11b	20 MHz 1 Mbps	—	53	—	dB
Receiver AACI 802.11b	20 MHz 11 Mbps	—	49	—	dB
Receiver AACI 802.11g	20 MHz 6 Mbps	—	49	—	dB
Receiver AACI 802.11g	20 MHz 54 Mbps	—	33.3	—	dB
Receiver AACI 802.11n	20 MHz MCS0 Nss1 BCC	—	49.7	—	dB
Receiver AACI 802.11n	20 MHz MCS7 Nss1 BCC	—	32.3	—	dB
Receiver AACI 802.11ax	20 MHz MCS0 Nss1 LDPC[1]	—	48.7	—	dB
Receiver AACI 802.11ax	20 MHz MCS11 Nss1 LDPC[1]	—	23.3	—	dB

[1] 4x long training field (LTF), guard time = 3.2 µs
[2] The measurements for 2.4 GHz IEEE 802.11b DSSS/CCK MIL are limited by the test setup capability.

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10.1.3 5 GHz Wi-Fi receiver performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at RF_TR_5 pin.*

Table 30. 5 GHz Wi-Fi receiver performance

Parameter	Condition	Min	Typ	Max	Unit
RF frequency range	5 GHz	5170	—	5895	MHz
Rx input IP3 at RF high gain (in-band)	—	—	-16	—	dBm
Receiver sensitivity					
Receiver sensitivity 802.11a	20 MHz 6 Mbps	—	-93.3	—	dBm
Receiver sensitivity 802.11a	20 MHz 54 Mbps	--	-76.6	--	dBm
Receiver sensitivity 802.11n	20 MHz MCS0 Nss1 BCC	—	-92.6	—	dBm
Receiver sensitivity 802.11n	20 MHz MCS7 Nss1 BCC	—	-72.9	—	dBm
Receiver sensitivity 802.11n	40 MHz MCS0 Nss1 BCC	—	-89.5	—	dBm
Receiver sensitivity 802.11n	40 MHz MCS7 Nss1 BCC	—	-70.5	—	dBm
Receiver sensitivity 802.11ac	20 MHz MCS0 Nss1 LDPC	—	-93.3	—	dBm
Receiver sensitivity 802.11ac	20 MHz MCS7 Nss1 LDPC	—	-75.6	—	dBm
Receiver sensitivity 802.11ac	20 MHz MCS8 Nss1 LDPC	—	-71.8	—	dBm
Receiver sensitivity 802.11ac	40 MHz MCS0 Nss1 LDPC	—-	-89.9	—	dBm
Receiver sensitivity 802.11ac	40 MHz MCS7 Nss1 LDPC	—	-73	—	dBm
Receiver sensitivity 802.11ac	40 MHz MCS9 Nss1 LDPC	—	-67.3	—	dBm
Receiver sensitivity 802.11ac	80 MHz MCS0 Nss1 LDPC	—	-86.6	—	dBm
Receiver sensitivity 802.11ac	80 MHz MCS7 Nss1 LDPC	—	-69.8	—	dBm
Receiver sensitivity 802.11ac	80 MHz MCS9 Nss1 LDPC	—	-64.3	—	dBm
Receiver sensitivity 802.11ax	20 MHz MCS0 Nss1 LDPC [1]	—	-93.3	—	dBm
Receiver sensitivity 802.11ax	20 MHz MCS11 Nss1 LDPC[1]	—	-63.1	—	dBm
Receiver sensitivity 802.11ax	40 MHz MCS0 Nss1 LDPC[1]	—	-89.7	—	dBm
Receiver sensitivity 802.11ax	40 MHz MCS11 Nss1 LDPC[1]	—	-61.2	—	dBm
Receiver sensitivity 802.11ax	80 MHz MCS0 Nss1 LDPC[1]	—	-85.7	—	dBm
Receiver sensitivity 802.11ax	80 MHz MCS11 Nss1 LDPC[1]	—	-57.7	—	dBm

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Table 30. 5 GHz Wi-Fi receiver performance*...continued*

Parameter	Condition	Min	Typ	Max	Unit
Receiver adjacent channel interference (ACI)					
Receiver ACI 802.11a	20 MHz 6 Mbps	—	23	—	dB
Receiver ACI 802.11a	20 MHz 54 Mbps	—	15.7	—	dB
Receiver ACI 802.11n	20 MHz MCS0 Nss1 BCC	—	28	—	dB
Receiver ACI 802.11n	20 MHz MCS7 Nss1 BCC	—	10	—	dB
Receiver ACI 802.11n	40 MHz MCS0 Nss1 BCC	—	27.3	—	dB
Receiver ACI 802.11n	40 MHz MCS7 Nss1 BCC	—	13	—	dB
Receiver ACI 802.11ac	20 MHz MCS0 Nss1 LDPC	—	31.3	—	dB
Receiver ACI 802.11ac	20 MHz MCS8 Nss1 LDPC	—	15	—	dB
Receiver ACI 802.11ac	40 MHz MCS0 Nss1 LDPC	—	29.7	—	dB
Receiver ACI 802.11ac	40 MHz MCS9 Nss1 LDPC	—	12.3	—	dB
Receiver ACI 802.11ac	80 MHz MCS0 Nss1 LDPC	—	25	—	dB
Receiver ACI 802.11ac	80 MHz MCS9 Nss1 LDPC	—	13	—	dB
Receiver ACI 802.11ax	20 MHz MCS0 Nss1 LDPC[1]	—	30.7	—	dB
Receiver ACI 802.11ax	20 MHz MCS11 Nss1 LDPC[1]	—	7	—	dB
Receiver ACI 802.11ax	40 MHz MCS0 Nss1 LDPC[1]	—	29	—	dB
Receiver ACI 802.11ax	40 MHz MCS11 Nss1 LDPC[1]	—	4	—	dB
Receiver ACI 802.11ax	80 MHz MCS0 Nss1 LDPC[1]	—	26	—	dB
Receiver ACI 802.11ax	80 MHz MCS11 Nss1 LDPC[1]	—	3	—	dB

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Table 30. 5 GHz Wi-Fi receiver performance*...continued*

Parameter	Condition	Min	Typ	Max	Unit
Receiver alternate adjacent channel interference (AACI)					
Receiver AACI 802.11a	20 MHz 6 Mbps	—	47.3	—	dB
Receiver AACI 802.11a	20 MHz 54 Mbps	—	27.7	—	dB
Receiver AACI 802.11n	20 MHz MCS0 Nss1 BCC	—	46.3	—	dB
Receiver AACI 802.11n	20 MHz MCS7 Nss1 BCC	—	30	—	dB
Receiver AACI 802.11n	40 MHz MCS0 Nss1 BCC	—	45	—	dB
Receiver AACI 802.11n	40 MHz MCS7 Nss1 BCC	—	27	—	dB
Receiver AACI 802.11ac	20 MHz MCS0 Nss1 LDPC	—	45.7	—	dB
Receiver AACI 802.11ac	20 MHz MCS8 Nss1 LDPC	—	29.3	—	dB
Receiver AACI 802.11ac	40 MHz MCS0 Nss1 LDPC	—	44.7	—	dB
Receiver AACI 802.11ac	40 MHz MCS9 Nss1 LDPC	—	23	—	dB
Receiver AACI 802.11ac	80 MHz MCS0 Nss1 LDPC	—	43.3	—	dB
Receiver AACI 802.11ac	80 MHz MCS9 Nss1 LDPC	—	24	—	dB
Receiver AACI 802.11ax	20 MHz MCS0 Nss1 LDPC[1]	—	48	—	dB
Receiver AACI 802.11ax	20 MHz MCS11 Nss1 LDPC[1]	—	21.3	—	dB
Receiver AACI 802.11ax	40 MHz MCS0 Nss1 LDPC[1]	—	45	—	dB
Receiver AACI 802.11ax	40 MHz MCS11 Nss1 LDPC[1]	—	19.7	—	dB
Receiver AACI 802.11ax	80 MHz MCS0 Nss1 LDPC[1]	—	44	—	dB
Receiver AACI 802.11ax	80 MHz MCS11 Nss1 LDPC[1]	—	18.3	—	dB

[1] 4x long training field (LTF), guard time = 3.2 µs

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10.1.4 2.4 GHz Wi-Fi transmitter performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at RF_TR_2 pin.*

Table 31. 2.4 GHz Wi-Fi transmitter performance

Parameter	Condition	Min	Typ	Max	Units
RF frequency range	2.4 GHz	2400	—	2483.5	MHz
Transmit power					
TX power (EVM and mask compliant) 20 MHz	802.11b DSSS, CCK	—	21	—	dBm
TX power (EVM and mask compliant) 20 MHz	OFDM 64-QAM (MCS7)	—	19	—	dBm
TX power (EVM and mask compliant) 20 MHz	OFDM 256-QAM (MCS8)	—	19	—	dBm
TX power (EVM and mask compliant) 20 MHz	OFDM 1024-QAM (MCS11)	—	17.5	—	dBm
TX power (EVM and mask compliant) 40 MHz	OFDM 64-QAM (MCS7)	—	19	—	dBm
TX power (EVM and mask compliant) 40 MHz	OFDM 256-QAM (MCS9)	—	18	—	dBm
TX power (EVM and mask compliant) 40 MHz	OFDM 1024-QAM (MCS11)	—	17.5	—	dBm
General TX parameters					
Transmit output power control step	—	—	1	—	dB
Transmit output power level control range	—	—	0 - 22	—	dBm
Transmit output power accuracy	With manufacturing time per board calibration	—	±1.5	—	dB
Transmit carrier suppression	—	—	37	—	dBc
Transmit frequency error	With manufacturing time per board calibration	—	±3	—	ppm

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10.1.5 5 GHz Wi-Fi transmitter performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at RF_TR_5 pin.*

Table 32. 5 GHz Wi-Fi transmitter performance

Parameter	Condition	Min	Typ	Max	Units
RF frequency range	5 GHz	5170	—	5895	MHz
Transmit power					
TX power (EVM and mask compliant) 20 MHz	OFDM 64-QAM (MCS7)	—	19.5	—	dBm
TX power (EVM and mask compliant) 20 MHz	OFDM 256-QAM (MCS8)	—	18	—	dBm
TX power (EVM and mask compliant) 20 MHz	OFDM 1024-QAM (MCS11)	—	15	—	dBm
TX power (EVM and mask compliant) 40 MHz	OFDM 64-QAM (MCS7)	—	19	—	dBm
TX power (EVM and mask compliant) 40 MHz	OFDM 256-QAM (MCS9)	—	17	—	dBm
TX power (EVM and mask compliant) 40 MHz	OFDM 1024-QAM (MCS11)	—	15	—	dBm
TX power (EVM and mask compliant) 80 MHz	OFDM 64-QAM (MCS7)	—	18	—	dBm
TX power (EVM and mask compliant) 80 MHz	OFDM 256-QAM (MCS9)	—	15.5	—	dBm
TX power (EVM and mask compliant) 80 MHz	OFDM 1024-QAM (MCS11)	—	12.5	—	dBm
General TX parameters					
Transmit output power control step	—	—	1	—	dB
Transmit output power level control range	—	—	0 - 22	—	dBm
Transmit output power accuracy	With manufacturing time per board calibration	—	±2	—	dB
Transmit carrier suppression	—	—	33	—	dBc
Transmit frequency error	With manufacturing time per board calibration	—	±3	—	ppm

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10.2 Bluetooth radio specifications

10.2.1 Bluetooth/Bluetooth LE receiver performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at BRF_ANT pin.*

Table 33. Bluetooth/Bluetooth LE receiver performance [1]

Parameter	Conditions	Min	Typ.	Max	Unit
Frequency range	—	2400	—	2483.5	MHz
Receiver sensitivity					
BDR 1 Mbps	—	—	-97.2	—	dBm
EDR 2 Mbps	—	—	-95.9	—	dBm
EDR 3 Mbps	—	—	-89.3	—	dBm
Bluetooth LE 1 Mbps	—	—	-98.5	—	dBm
Bluetooth LE 2 Mbps	—	—	-96.2	—	dBm
Bluetooth LR 125 Kbps	—	—	-106.6	—	dBm
Bluetooth LR 500 Kbps	—	—	-100	—	dBm
Receiver maximum input level (MIL)					
BDR 1 Mbps	—	—	-3[2]	—	dBm
EDR 2 Mbps	—	—	-6[3]	—	dBm
EDR 3 Mbps	—	—	-6[4]	—	dBm
Bluetooth LE 1 Mbps	—	—	-3[5]	—	dBm
Bluetooth LE 2 Mbps	—	—	-3[6]	—	dBm
Bluetooth LR 125 Kbps	—	—	-3[7]	—	dBm
Bluetooth LR 500 Kbps	—	—	-3[8]	—	dBm
Receiver adjacent channel interference (ACI)/CCI performance					
BDR 1 Mbps					
Receiver ACI @ -5 MHz (image -1)	BDR 1 Mbps	—	-38	—	dB
Receiver ACI @ -4 MHz (image)	BDR 1 Mbps	—	-26	—	dB
Receiver ACI @ -3 MHz (image +1)	BDR 1 Mbps	—	-41	—	dB
Receiver ACI @ -2 MHz	BDR 1 Mbps	—	-46	—	dB
Receiver ACI @ -1 MHz	BDR 1 Mbps	—	-9	—	dB
Receiver CCI	BDR 1 Mbps	—	11	—	dB
Receiver ACI @ +1 MHz	BDR 1 Mbps	—	-11	—	dB
Receiver ACI @ +2 MHz	BDR 1 Mbps	—	-49	—	dB
Receiver ACI @ +3 MHz	BDR 1 Mbps	—	-52	—	dB
EDR 2 Mbps					
Receiver ACI @ -5 MHz (image -1)	EDR 2 Mbps	—	-42	—	dB
Receiver ACI @ -4 MHz (image)	EDR 2 Mbps	—	-28	—	dB
Receiver ACI @ -3 MHz (image +1)	EDR 2 Mbps	—	-41	—	dB

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Table 33. Bluetooth/Bluetooth LE receiver performance [1] *...continued*

Parameter	Conditions	Min	Typ.	Max	Unit
Receiver ACI @ -2 MHz	EDR 2 Mbps	—	-46	—	dB
Receiver ACI @ -1 MHz	EDR 2 Mbps	—	-9	—	dB
Receiver CCI	EDR 2 Mbps	—	10	—	dB
Receiver ACI @ +1 MHz	EDR 2 Mbps	—	-11	—	dB
Receiver ACI @ +2 MHz	EDR 2 Mbps	—	-49	—	dB
Receiver ACI @ +3 MHz	EDR 2 Mbps	—	-52	—	dB
BDR 3 Mbps					
Receiver ACI @ -5 MHz (image -1)	EDR 3 Mbps	—	-38	—	dB
Receiver ACI @ -4 MHz (image)	EDR 3 Mbps	—	-20	—	dB
Receiver ACI @ -3 MHz (image +1)	EDR 3 Mbps	—	-38	—	dB
Receiver ACI @ -2 MHz	EDR 3 Mbps	—	-41	—	dB
Receiver ACI @ -1 MHz	EDR 3 Mbps	—	-8	—	dB
Receiver CCI	EDR 3 Mbps	—	16	—	dB
Receiver ACI @ +1 MHz	EDR 3 Mbps	—	-8	—	dB
Receiver ACI @ +2 MHz	EDR 3 Mbps	—	-42	—	dB
Receiver ACI @ +3 MHz	EDR 3 Mbps	—	-48	—	dB
Bluetooth LE 1 Mbps					
Receiver ACI @ -5 MHz (image -1)	Bluetooth LE 1 Mbps	—	-39	—	dB
Receiver ACI @ -4 MHz (image)	Bluetooth LE 1 Mbps	—	-28	—	dB
Receiver ACI @ -3 MHz (image +1)	Bluetooth LE 1 Mbps	—	-38	—	dB
Receiver ACI @ -2 MHz	Bluetooth LE 1 Mbps	—	-45	—	dB
Receiver ACI @ -1 MHz	Bluetooth LE 1 Mbps	—	-3	—	dB
Receiver CCI	Bluetooth LE 1 Mbps	—	9	—	dB
Receiver ACI @ +1 Mbps	Bluetooth LE 1 Mbps	—	-9	—	dB
Receiver ACI @ +2 Mbps	Bluetooth LE 1 Mbps	—	-50	—	dB
Receiver ACI @ +3 Mbps	Bluetooth LE 1 Mbps	—	-52	—	dB
Bluetooth LE 2 Mbps					
Receiver ACI @ -6 MHz (image -2)	Bluetooth LE 2 Mbps	—	-51	—	dB
Receiver ACI @ -4 MHz (image)	Bluetooth LE 2 Mbps	—	-29	—	dB
Receiver ACI @ -2 MHz	Bluetooth LE 2 Mbps	—	-19	—	dB
Receiver CCI	Bluetooth LE 2 Mbps	—	8	—	dB
Receiver ACI @ +2 Mbps	Bluetooth LE 2 Mbps	—	-29	—	dB
Receiver ACI @ +4 Mbps	Bluetooth LE 2 Mbps	—	-51	—	dB
Receiver ACI @ +6 Mbps	Bluetooth LE 2 Mbps	—	-55	—	dB

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Table 33. Bluetooth/Bluetooth LE receiver performance [1] *...continued*

Parameter	Conditions	Min	Typ.	Max	Unit
Bluetooth LR 125 Kbps					
Receiver ACI @ -5 MHz (image -1)	Bluetooth LR 125 Kbps	—	-41	—	dB
Receiver ACI @ -4 MHz (image)	Bluetooth LR 125 Kbps	—	-28	—	dB
Receiver ACI @ -3 MHz (image +1)	Bluetooth LR 125 Kbps	—	-39	—	dB
Receiver ACI @ -2 MHz	Bluetooth LR 125 Kbps	—	-49	—	dB
Receiver ACI @ -1 MHz	Bluetooth LR 125 Kbps	—	-5	—	dB
Receiver CCI	Bluetooth LR 125 Kbps	—	9	—	dB
Receiver ACI @ +1 Mbps	Bluetooth LR 125 Kbps	—	-12	—	dB
Receiver ACI @ +2 Mbps	Bluetooth LR 125 Kbps	—	-55	—	dB
Receiver ACI @ +3 Mbps	Bluetooth LR 125 Kbps	—	-60	—	dB
Bluetooth LR 500 Kbps					
Receiver ACI @ -5 MHz (image -1)	Bluetooth LR 500 Kbps	—	-40	—	dB
Receiver ACI @ -4 MHz (image)	Bluetooth LR 500 Kbps	—	-28	—	dB
Receiver ACI @ -3 MHz (image +1)	Bluetooth LR 500 Kbps	—	-38	—	dB
Receiver ACI @ -2 MHz	Bluetooth LR 500 Kbps	—	-48	—	dB
Receiver ACI @ -1 MHz	Bluetooth LR 500 Kbps	—	-5	—	dB
Receiver CCI	Bluetooth LR 500 Kbps	—	9	—	dB
Receiver ACI @ +1 Mbps	Bluetooth LR 500 Kbps	—	-11	—	dB
Receiver ACI @ +2 Mbps	Bluetooth LR 500 Kbps	—	-51	—	dB
Receiver ACI @ +3 Mbps	Bluetooth LR 500 Kbps	—	-55	—	dB

[1] Bluetooth/Bluetooth LE receiver refers to Dirty Tx. That is, the transmitter has impairments as specified by the Bluetooth SIG standard.
[2] De-sense of 2.7 dB at 2440 MHz, 0.5 dB at 2480 MHz
[3] De-sense of 3.4 dB at 2440 MHz, 1.2 dB at 2480 MHz
[4] De-sense of 3.6 dB at 2440 MHz, 1.1 dB at 2480 MHz
[5] De-sense of 3.8 dB at 2440 MHz, 0.8 dB at 2480 MHz
[6] De-sense of 2.1 dB at 2440 MHz, 0.6 dB at 2480 MHz
[7] De-sense of 3.4 dB at 2440 MHz, 0.6 dB at 2480 MHz
[8] De-sense of 5.3 dB at 2440 MHz, 1 dB at 2480 MHz

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10.2.2 Bluetooth/Bluetooth LE transmitter performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at BRF_ANT pin.*

Table 34. Bluetooth/Bluetooth LE transmitter performance

Parameter	Conditions	Min	Typ.	Max	Unit
Frequency range	—	2400	—	2483.5	MHz
BDR maximum transmit power	Mask compliant	—	18.7[1]	—	dBm
EDR maximum transmit power	EVM and mask compliant	—	9.7	—	dBm
Bluetooth LE maximum transmit power	—	—	19[1][2][3]	—	dBm
Out-of band noise floor at different operation standard frequency range Tx at 13 dBm with 100% duty cycle	—	—	-140	-130	dBm/Hz
Transmit frequency error	—	—	-3	—	kHz
Transmit output power accuracy (BDR/ Bluetooth LE)	—	—	±2	—	dB
Transmit output power control step (BDR/ Bluetooth LE)	—	—	0.5	—	dB
Transmit output power level control range (BDR)	—	—	-19 to +20	—	dBm
Transmit output power accuracy (EDR)	—	—	±2	—	dB
Transmit output power control step (EDR)	—	—	0.5	—	dB
Transmit output power level control range (EDR)	—	—	-23 to +10	—	dBm

[1] Meets the Bluetooth SIG requirement of maximum power difference between GFSK and QPSK portions of the EDR packet to less than 10 dB.
[2] The maximum TX power is limited to 14 dBm for Bluetooth LE Long Range packets.
[3] The maximum TX power is 18 dBm for Bluetooth LE 2 Mbps and 2480 MHz channel.

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10.3 Current consumption

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and typical value with SDIO 2.0 25 MHz clock (4-bit mode).*

Table 35. Current consumption values

Mode	Conditions	1.8V	3.3V	VIO (3.3V)	Unit
Power down					
Power down	—	0.019	0.084	0.005	mA
Sleep mode					
Bluetooth only in deep sleep mode	—	0.25	0.02	0.12	mA
Wi-Fi only in deep sleep mode	SDIO 2.0 25 MHz	0.36	0.02	0.06	mA
	SDIO 3.0 200 MHz[1], VIO = 1.8 V	1.8	0	0.02	mA
Wi-Fi and Bluetooth in deep sleep mode	—	0.41	0.02	0.12	mA
Bluetooth LE current consumption (Wi-Fi not enabled, SDIO host interface not connected)					
Bluetooth LE advertise	Interval = 1.28 s	0.32	0.02	0.12	mA
Bluetooth LE scan	Interval = 1.28 s window = 11.25 ms	0.56	0.02	0.12	mA
Bluetooth LE link	Interval=1.28 s	0.98	0.97	0.12	mA
Bluetooth LE peak transmit[2]	1 Mbps @ 0 dBm	43	0.11	0.22	mA
Bluetooth LE peak transmit [2]	1 Mbps @ 4 dBm	48	0.11	0.22	mA
Bluetooth LE peak transmit [2]	1 Mbps @ 10 dBm	89	0.11	0.22	mA
Bluetooth LE peak transmit [2]	1 Mbps @ 13 dBm	110	0.11	0.22	mA
Bluetooth LE peak transmit [2]	1 Mbps @ 19 dBm	287	0.11	0.22	`mA
Bluetooth LE peak receive[3][4]	1 Mbps	39	0.11	0.22	mA

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Table 35. Current consumption values...*continued*

Mode	Conditions	1.8V	3.3V	VIO (3.3V)	Unit
Bluetooth current consumption (Wi-Fi not enabled, SDIO host interface not connected, Bluetooth TX power = 0 dBm if not mentioned)					
Bluetooth idle	—	9.8	0.11	0.22	mA
Bluetooth SCO HV3 peak transmit	@ 0 dBm	43	0.11	0.22	mA
Bluetooth SCO HV3 peak transmit	@ 5 dBm	48	0.11	0.22	mA
Bluetooth SCO HV3 peak transmit	@ 10 dBm	89	0.11	0.22	mA
Bluetooth SCO HV3 peak transmit	@ 13 dBm	110	0.11	0.22	mA
Bluetooth SCO HV3 peak receive	—	39	0.11	0.22	mA
Bluetooth peak transmit[5]	@ 0 dBm, DH5	43	0.11	0.22	mA
Bluetooth peak transmit[5]	@ 4 dBm, DH5	48	0.11	0.22	mA
Bluetooth peak transmit[5]	@ 10 dBm, DH5	89	0.11	0.22	mA
Bluetooth peak transmit[5]	@ 13 dBm, DH5	110	0.11	0.22	mA
Bluetooth peak transmit[5]	@ 19 dBm, DH5	287	0.11	0.22	mA
Bluetooth peak receive[3][6]	BDR, DH5	39	0.11	0.22	mA
Bluetooth ACL	Data pump, DH1	24.8	0.11	0.22	mA
Bluetooth ACL	Data pump, 2-DH3	32.7	0.11	0.22	mA
Bluetooth ACL	Data pump, 3-DH5	35.5	0.11	0.22	mA
Bluetooth ACL link	Central sniff mode interval=1.28s	0.52	0.02	0.12	mA
Bluetooth ACL link	Central sniff mode interval = 500 ms	0.89	0.02	0.12	mA
Bluetooth page scan	—	0.66	0.02	0.12	mA
Bluetooth page and inquiry scan	—	0.97	0.02	0.12	mA

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Table 35. Current consumption values...*continued*

Mode	Conditions	1.8V	3.3V	VIO (3.3V)	Unit
IEEE power save mode - receive (Bluetooth not enabled, beacon interval = 102.4 ms))[7]					
DTIM 1 IEEE-PS 2.4 GHz	2.4 G basic rate for beacon transmit: 1 Mbps SDIO 2.0, 50 MHz	1.93	0	0.02	mA
DTIM 3 IEEE-PS 2.4 GHz		0.89	0	0.02	mA
DTIM 5 IEEE-PS 2.4 GHz		0.67	0	0.02	mA
DTIM 10 IEEE-PS 2.4 GHz		0.57	0	0.02	mA
DTIM 1 IEEE-PS 5 GHz	5 GHz basic rate for beacon transmit: 6 Mbps SDIO 2.0, 50 MHz	1.56	0	0.02	mA
DTIM 3 IEEE-PS 5 GHz		0.78	0	0.02	mA
DTIM 5 IEEE-PS 5 GHz		0.63	0	0.02	mA
DTIM 10 IEEE-PS 5 GHz		0.54	0	0.02	mA
DTIM 1 IEEE-PS 2.4 GHz	2.4 G basic rate for beacon transmit: 1 Mbps SDIO 3.0, 200 MHz[1], VIO = 1.8 V	3.25	0	0.02	mA
DTIM 3 IEEE-PS 2.4 GHz		2.2	0	0.02	mA
DTIM 5 IEEE-PS 2.4 GHz		1.98	0	0.02	mA
DTIM 10 IEEE-PS 2.4 GHz		1.87	0	0.02	mA
DTIM 1 IEEE-PS 5 GHz	5 GHz basic rate for beacon transmit: 6 Mbps SDIO 3.0, 200 MHz[1], VIO = 1.8 V	3.0	0	0.02	mA
DTIM 3 IEEE-PS 5 GHz		2.22	0	0.02	mA
DTIM 5 IEEE-PS 5 GHz		2.1	0	0.02	mA
DTIM 10 IEEE-PS 5 GHz		1.97	0	0.02	mA
IEEE 802.11ax target wake-up time (TWT)[8]					
TWT 1 min	2.4 GHz, SDIO-3.0, 200 MHz	1.96	0	0.02	mA
TWT 5 min		1.83	0	0.02	mA
TWT 10 min		1.82	0	0.02	mA
TWT 20 min		1.82	0	0.02	mA
TWT 30 min		1.81	0	0.02	mA
TWT 1 min	5 GHz, SDIO-3.0, 200 MHz	1.99	0	0.02	mA
TWT 5 min		1.86	0	0.02	mA
TWT 10 min		1.83	0	0.02	mA
TWT 20 min		1.82	0	0.02	mA
TWT 30 min		1.81	0	0.02	mA
2.4 GHz Wi-Fi receive idle mode (Bluetooth not enabled)					
2.4 GHz, 802.11b, 11 Mbps	—	94	0.13	0.17	mA
2.4 GHz, 802.11g, 54 Mbps	—	94	0.13	0.17	mA
2.4 GHz, 802.11n, 20 MHz, MCS7	—	96	0.13	0.17	mA
2.4 GHz, 802.11n, 40 MHz, MCS7	—	110	0.13	0.17	mA
2.4 GHz, 802.11ax, 20 MHz, MCS11	—	95	0.13	0.17	mA
2.4 GHz, 802.11ax, 40 MHz, MCS11	—	111	0.13	0.17	mA

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Table 35. Current consumption values...*continued*

Mode	Conditions	1.8V	3.3V	VIO (3.3V)	Unit
5 GHz Wi-Fi receive idle mode (Bluetooth not enabled)					
5 GHz, 802.11a, 54 Mbps	—	113	0.13	0.17	mA
5 GHz, 802.11n, 20 MHz, MCS7	—	115	0.13	0.17	mA
5 GHz, 802.11n, 40 MHz, MCS7	—	130	0.13	0.17	mA
5 GHz, 802.11ac, 20 MHz, MCS8	—	115	0.13	0.17	mA
5 GHz, 802.11ac, 40 MHz, MCS9	—	130	0.13	0.17	mA
5 GHz, 802.11ac, 80 MHz, MCS9	—	159	0.13	0.17	mA
5 GHz, 802.11ax, 20 MHz, MCS11	—	113	0.13	0.17	mA
5 GHz, 802.11ax, 40 MHz, MCS11	—	130	0.13	0.17	mA
5 GHz, 802.11ax, 80 MHz, MCS11	—	159	0.13	0.17	mA
2.4 GHz Wi-Fi receive active mode (Bluetooth not enabled)					
2.4 GHz, 802.11b, 11 Mbps	—	91	0.13	0.17	mA
2.4 GHz, 802.11g, 54 Mbps	—	101	0.13	0.17	mA
2.4 GHz, 802.11n, 20 MHz, MCS7	—	116	0.13	0.17	mA
2.4 GHz, 802.11n, 40 MHz, MCS7	—	126	0.13	0.17	mA
2.4 GHz, 802.11ax, 20 MHz, MCS11	—	108	0.13	0.17	mA
2.4 GHz, 802.11ax, 40 MHz, MCS11	—	128	0.13	0.17	mA
5 GHz Wi-Fi receive active mode (Bluetooth not enabled)					
5 GHz, 802.11a, 54 Mbps	—	116	0.13	0.17	mA
5 GHz, 802.11n, 20 MHz, MCS7	—	125	0.13	0.17	mA
5 GHz, 802.11n, 40 MHz, MCS7	—	139	0.13	0.17	mA
5 GHz, 802.11ac, 20 MHz, MCS8	—	121	0.13	0.17	mA
5 GHz, 802.11ac, 40 MHz, MCS9	—	140	0.13	0.17	mA
5 GHz, 802.11ac, 80 MHz, MCS9,	—	177	0.13	0.17	mA
5 GHz, 802.11ax, 20 MHz, MCS11	—	127	0.13	0.17	mA
5 GHz, 802.11ax, 40 MHz, MCS11	—	142	0.13	0.17	mA
5 GHz, 802.11ax, 80 MHz, MCS11	—	180	0.13	0.17	mA

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Table 35. Current consumption values...*continued*

Mode	Conditions	1.8V	3.3V	VIO (3.3V)	Unit
2.4 GHz Wi-Fi transmit (Bluetooth not enabled, transmit referred to pin)					
2.4 GHz, 802.11b, 11 Mbps @ 21 dBm	—	152	256	0.17	mA
2.4 GHz, 802.11b, 11 Mbps @ 20 dBm	—	150	204	0.17	mA
2.4 GHz, 802.11g, 54 Mbps @ 20 dBm	—	155	209	0.17	mA
2.4 GHz, 802.11n, 20 MHz, MCS0 @ 20 dBm	—	157	207	0.17	mA
2.4 GHz, 802.11n, 20 MHz, MCS7 @ 20 dBm	—	157	206	0.17	mA
2.4 GHz, 802.11n, 40 MHz, MCS0 @ 20 dBm	—	165	215	0.17	mA
2.4 GHz, 802.11n, 40 MHz, MCS7 @ 20 dBm	—	166	215	0.17	mA
2.4 GHz, 802.11ax, 20 MHz, MCS0 @ 20 dBm	—	156	215	0.17	mA
2.4 GHz, 802.11ax, 20 MHz, MCS11 @ 20 dBm	—	157	209	0.17	mA
2.4 GHz, 802.11ax, 40 MHz, MCS0 @ 20 dBm	—	165	210	0.17	mA
2.4 GHz, 802.11ax, 40 MHz, MCS11 @ 20 dBm	—	166	210	0.17	mA
5 GHz Wi-Fi transmit (Bluetooth not enabled, transmit referred to pin)					
5 GHz, 802.11a, 6 Mbps @ 19 dBm	—	218	279	0.17	mA
5 GHz, 802.11a, 54 Mbps @ 19 dBm	—	218	279	0.17	mA
5 GHz, 802.11n, 20 MHz, MCS0 @ 19 dBm	—	221	272	0.17	mA
5 GHz, 802.11n, 20 MHz, MCS7 @ 19 dBm	—	220	270	0.17	mA
5 GHz, 802.11n, 40 MHz, MCS0 @ 17 dBm	—	225	229	0.17	mA
5 GHz, 802.11n, 40 MHz, MCS7 @ 17 dBm	—	225	226	0.17	mA
5 GHz, 802.11ac, 20 MHz, MCS0 @ 19 dBm	—	219	268	0.17	mA
5 GHz, 802.11ac, 20 MHz, MCS8 @ 19 dBm	—	219	270	0.17	mA
5 GHz, 802.11ac, 40 MHz, MCS0 @ 17 dBm	—	225	229	0.17	mA
5 GHz, 802.11ac, 40 MHz, MCS9 @ 17 dBm	—	226	228	0.17	mA
5 GHz, 802.11ac, 80 MHz, MCS0 @ 15 dBm	—	227	190	0.17	mA
5 GHz, 802.11ac, 80 MHz, MCS9 @ 15 dBm	—	223	192	0.17	mA
5 GHz, 802.11ax, 20 MHz, MCS0 @ 19 dBm	—	219	268	0.17	mA
5 GHz, 802.11ax, 20 MHz, MCS11 @ 19 dBm	—	219	273	0.17	mA
5 GHz, 802.11ax, 40 MHz, MCS0 @ 17 dBm	—	220	224	0.17	mA
5 GHz, 802.11ax, 40 MHz, MCS11 @ 17 dBm	—	222	225	0.17	mA
5 GHz, 802.11ax, 80 MHz, MCS0 @ 15 dBm	—	226	190	0.17	mA
5 GHz, 802.11ax, 80 MHz, MCS11 @ 15 dBm	—	222	187	0.17	mA

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Table 35. Current consumption values*...continued*

Mode	Conditions	1.8V	3.3V	VIO (3.3V)	Unit
Peak current					
Peak current during device initialization	—	497	368	0.17	mA
5 GHz 802.11ax 80 MHz, MCS11 receive + Bluetooth LE transmit at 21 dBm[9]	At 85°C	644[10]	0.2[10]	0.23	mA
5 GHz 802.11ax, 20 MHz, MCS11 transmit + Bluetooth LE transmit at 21 dBm[9]	At 85°C	752[10]	303[10]	0.23	mA

[1] SDIO host interface connected
[2] The peak transmit current remains the same across all Bluetooth LE data rates at the same transmit power level
[3] Dual antenna configuration
[4] The peak receive current remains the same across all Bluetooth LE data rates
[5] The peak transmit current remains the same across all Bluetooth data rates at the same transmit power level
[6] The peak receive current remains the same across all Bluetooth data rates
[7] Frame length in IEEE-PS current measurement: 5 GHz: 1000 µsecond, 2.4 GHz: 1000 µsecond
[8] Nominal TWT receive window duration: 50 ms
[9] Absolute maximum output power that the device can support. Operating maximum output power limited for regulatory compliance.
[10] Maximum value

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11 Electrical specifications

11.1 GPIO interface specifications

11.1.1 DC characteristics

11.1.1.1 1.8V operation

Table 36. DC electricals—1.8V operation (VIO)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions".

Symbol	Parameter	Condition	Min	Typ	Max	Units
VIO	I/O pad supply voltage	—	1.71	1.8	1.89	V
V_{IH}	Input high voltage	—	0.7*VIO	—	VIO+0.4	V
V_{IL}	Input low voltage	—	-0.4	—	0.3*VIO	V
V_{HYS}	Input hysteresis	—	100	—	—	mV
V_{OH}	Output high voltage	—	VIO-0.4	—	—	V
V_{OL}	Output low voltage	—	—	—	0.4	V

11.1.1.2 3.3V operation

Table 37. DC electricals—3.3V operation (VIO)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIO	I/O pad supply voltage	—	3.14	3.3	3.46	V
V_{IH}	Input high voltage	—	0.7*VIO	—	VIO+0.4	V
V_{IL}	Input low voltage	—	-0.4	—	0.3*VIO	V
V_{HYS}	Input hysteresis	—	100	—	—	mV
V_{OH}	Output high voltage	—	VIO-0.4	—	—	V
V_{OL}	Output low voltage	—	—	—	0.4	V

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11.2 RF front-end control interface specifications

11.2.1 DC characteristics

11.2.1.1 1.8V operation

Table 38. DC electricals—1.8V operation (VIO_RF)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input high voltage	—	0.7*VIO_RF	—	VIO_RF+0.4	V
V_{IL}	Input low voltage	—	-0.4	—	0.3*VIO_RF	V
V_{HYS}	Input hysteresis	—	100	—	—	mV
V_{OH}	Output high voltage	—	VIO_RF-0.4	—	—	V
V_{OL}	Output low voltage	—	—	—	0.4	V

11.2.1.2 3.3V operation

Table 39. DC electricals—3.3V operation (VIO_RF)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input high voltage	—	0.7*VIO_RF	—	VIO_RF+0.4	V
V_{IL}	Input low voltage	—	-0.4	—	0.3*VIO_RF	V
V_{HYS}	Input hysteresis	—	100	—	—	mV
V_{OH}	Output high voltage	—	VIO_RF-0.4	—	—	V
V_{OL}	Output low voltage	—	—	—	0.4	V

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11.3 SDIO host interface specifications

The SDIO host interface pins are supplied by VIO_SD voltage supply.

The SDIO electrical specifications are identical for 4-bit SDIO and 1-bit SDIO modes.

11.3.1 DC characteristics

11.3.1.1 1.8V operation

Table 40. DC electricals—1.8V operation (VIO_SD)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input high voltage	—	0.7*VIO_SD	—	VIO_SD+0.4	V
V_{IL}	Input low voltage	—	-0.4	—	0.3*VIO_SD	V
V_{HYS}	Input hysteresis	—	100	—	—	mV
V_{OH}	Output high voltage	—	VIO_SD-0.4	—	—	V
V_{OL}	Output low voltage	—	—	—	0.4	V

11.3.1.2 3.3V operation

Table 41. DC electricals—3.3V operation (VIO_SD)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input high voltage	—	0.7*VIO_SD	—	VIO_SD+0.4	V
V_{IL}	Input low voltage	—	-0.4	—	0.3*VIO_SD	V
V_{HYS}	Input hysteresis	—	100	—	—	mV
V_{OH}	Output high voltage	—	VIO_SD-0.4	—	—	V
V_{OL}	Output low voltage	—	—	—	0.4	V

11.3.2 Default speed, high-speed modes

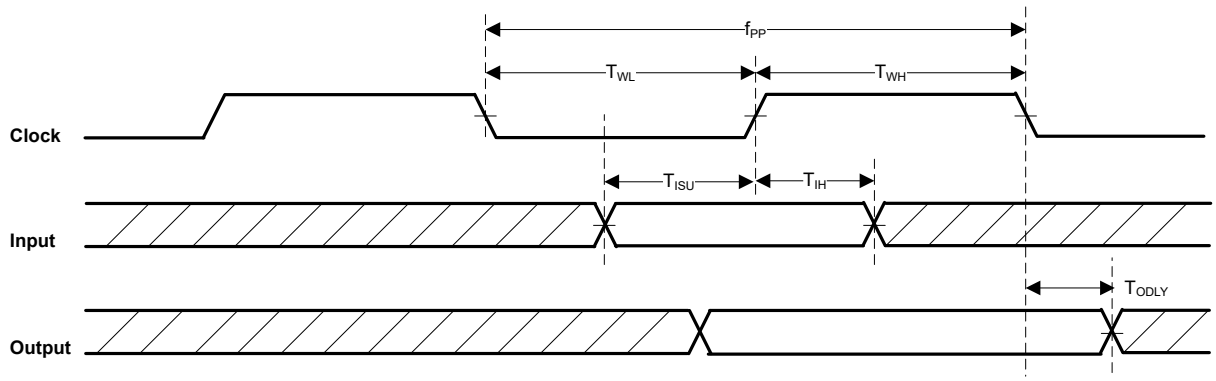

Figure 21. SDIO protocol timing diagram—Default speed mode

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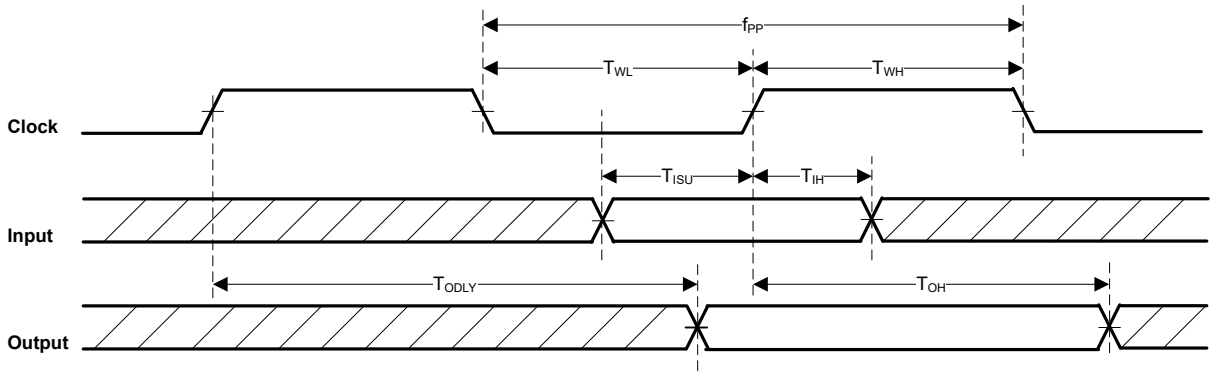

Figure 22. SDIO protocol timing diagram—High-speed mode

Table 42. SDIO timing data —Default speed, high-speed modes

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PP}	Clock frequency	Normal	0	—	25	MHz
		High-speed	0	—	50	MHz
T_{WL}	Clock low time	Normal	10	—	—	ns
		High-speed	7	—	—	ns
T_{WH}	Clock high time	Normal	10	—	—	ns
		High-speed	7	—	—	ns
T_{ISU}	Input setup time	Normal	5	—	—	ns
		High-speed	6	—	—	ns
T_{IH}	Input hold time	Normal	5	—	—	ns
		High-speed	2	—	—	ns
T_{ODLY}	Output delay time	Normal	—	—	14	ns
	CL ≤ 40 pF (1 card)	High-speed	—	—	14	ns
T_{OH}	Output hold time	High-speed	2.5	—	—	ns

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11.3.3 SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8V)

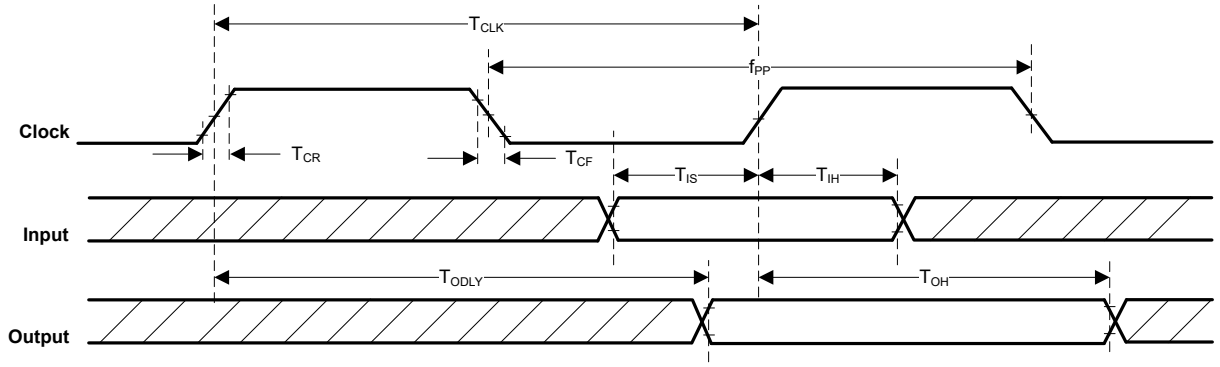

Figure 23. SDIO protocol timing diagram—SDR12, SDR25, SDR50 Modes (up to 100 MHz) (1.8V)

Table 43. SDIO timing data——SDR12, SDR25, SDR50 Modes (up to 100 MHz) (1.8 V)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PP}	Clock frequency	SDR12	0	—	25	MHz
		SDR25	0	—	50	MHz
		SDR50	0	—	100	MHz
T_{IS}	Input setup time	SDR12	3	—	—	ns
		SDR25	3	—	—	ns
		SDR50	3	—	—	ns
T_{IH}	Input hold time	SDR12	0.8	—	—	ns
		SDR25	0.8	—	—	ns
		SDR50	0.8	—	—	ns
T_{CLK}	Clock time	SDR12	40	—	40	ns
		SDR25	10	—	20	ns
		SDR50	10	—	10	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 2 ns (max) at 100 MHz C_{CARD} = 10 pF	SDR12	—	—	$0.2*T_{CLK}$	ns
	Rise time, fall time T_{CR}, T_{CF} < 2 ns (max) at 100 MHz C_{CARD} = 10 pF	SDR25	—	—	$0.2*T_{CLK}$	ns
	Rise time, fall time T_{CR}, T_{CF} < 2 ns (max) at 100 MHz C_{CARD} = 10 pF	SDR50	—	—	$0.2*T_{CLK}$	ns

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Table 43. SDIO timing data——SDR12, SDR25, SDR50 Modes (up to 100 MHz) (1.8 V)*...continued*

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{ODLY}	Output delay time C_L ≤ 30 pF	SDR12	—	—	14	ns
		SDR25	—	—	14	ns
		SDR50	—	—	7.5	ns
T_{OH}	Output hold time C_L = 15 pF	SDR12	1.5	—	—	ns
	Output hold time C_L = 15 pF	SDR25	1.5	—	—	ns
	Output hold time C_L = 15 pF	SDR50	1.5	—	—	ns

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11.3.4 SDR104 mode (208 MHz) (1.8V)

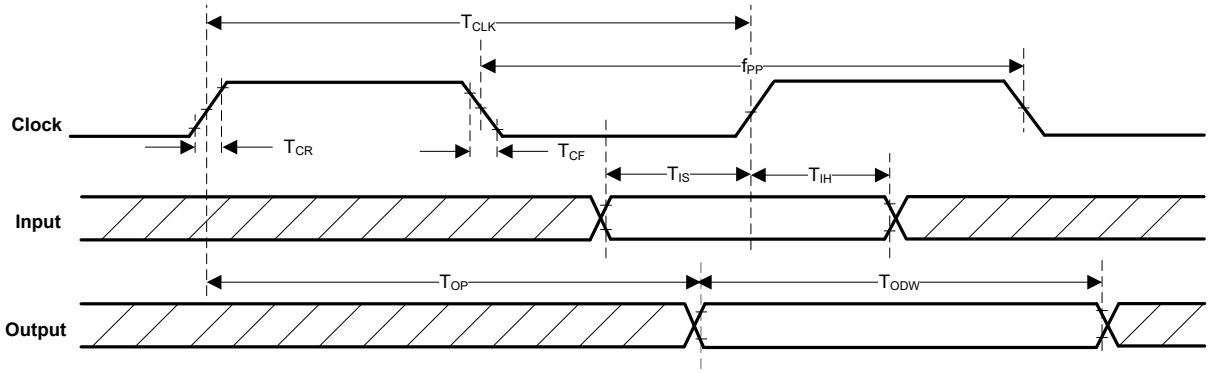

Figure 24. SDIO protocol timing diagram—SDR104 mode (208 MHz)

Table 44. SDIO timing data—SDR104 mode (208 MHz)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PP}	Clock frequency	SDR104	0	—	208	MHz
T_{IS}	Input setup time	SDR104	1.4	—	—	ns
T_{IH}	Input hold time	SDR104	0.8	—	—	ns
T_{CLK}	Clock time	SDR104	4.8	—	—	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 0.96 ns (max) at 208 MHz C_{CARD} = 10 pF	SDR104	—	—	$0.2*T_{CLK}$	ns
T_{OP}	Card output phase	SDR104	0	—	2	T_{CLK}
T_{ODW}	Output timing of variable data window	SDR104	2.88	—	—	ns

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11.3.5 DDR50 mode (50 MHz) (1.8V)

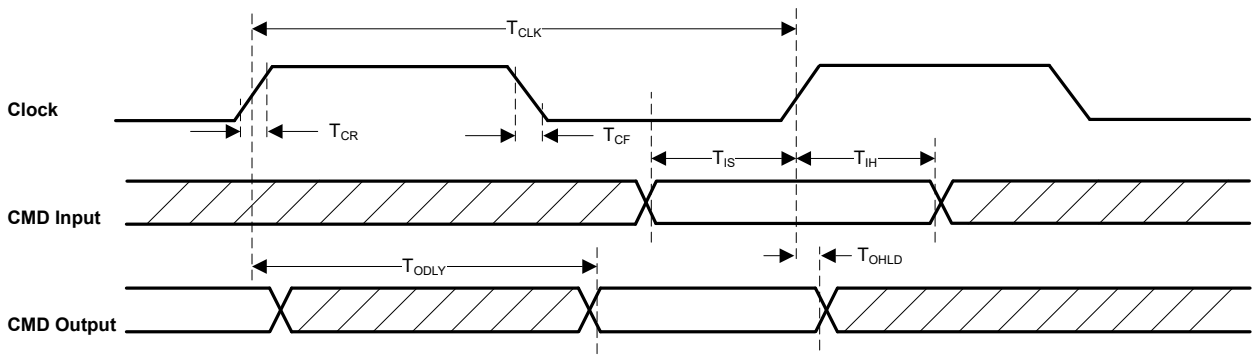

Figure 25. SDIO CMD timing diagram—DDR50 mode (50 MHz)

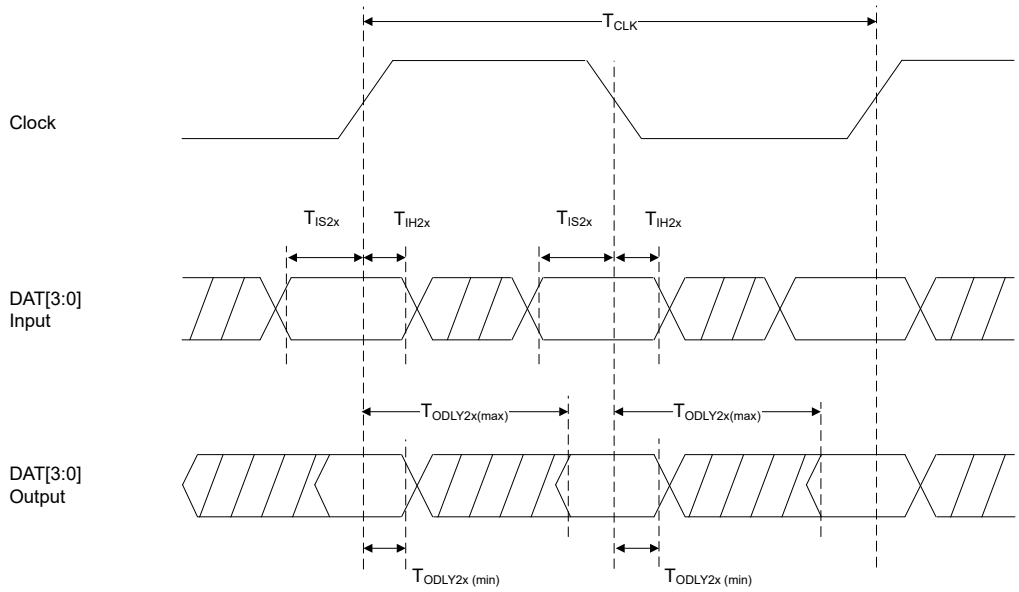

Figure 26. SDIO DAT[3:0] timing diagram—DDR50 mode[1] (50 MHz)

[1] In DDR50 mode, DAT[3:0] lines are sampled on both edges of the clock (not applicable for CMD line).

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Table 45. SDIO timing data—DDR50 mode (50 MHz)

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Clock						
T_{CLK}	Clock time 50 MHz (max) between rising edges	DDR50	20	—	—	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 4.00 ns (max) at 50 MHz C_{CARD} = 10 pF	DDR50	—	—	0.2*T_{CLK}	ns
Clock Duty	—	DDR50	45	—	55	%
CMD Input (referenced to clock rising edge)						
T_{IS}	Input setup time C_{CARD} ≤ 10 pF (1 card)	DDR50	6	—	—	ns
T_{IH}	Input hold time C_{CARD} ≤ 10 pF (1 card)	DDR50	0.8	—	—	ns
CMD Output (referenced to clock rising edge)						
T_{ODLY}	Output delay time during data transfer mode C_L ≤ 30 pF (1 card)	DDR50	—	—	13.7	ns
T_{OHLD}	Output hold time C_L ≥ 15 pF (1 card)	DDR50	1.5	—	—	ns
DAT[3:0] Input (referenced to clock rising and falling edges)						
T_{IS2x}	Input setup time C_{CARD} ≤ 10 pF (1 card)	DDR50	3	—	—	ns
T_{IH2x}	Input hold time C_{CARD} ≤ 10 pF (1 card)	DDR50	0.8	—	—	ns
DAT[3:0] Output (referenced to clock rising and falling edges)						
$T_{ODLY2x\ (max)}$	Output delay time during data transfer mode C_L ≤ 25 pF (1 card)	DDR50	—	—	7.0	ns
$T_{ODLY2x\ (min)}$	Output hold time C_L ≥ 15 pF (1 card)	DDR50	1.5	—	—	ns

11.3.6 SDIO internal pull-up/pull-down specifications

Table 46. SDIO internal pull-up/pull-down specifications

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
Internal nominal pull-up/pull-down resistance	—	70	100	140	kΩ

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11.4 UART interface specifications

The UART Tx and Rx pins are powered from the VIO voltage supply.

See Section 11.1.1 "DC characteristics" for DC specifications.

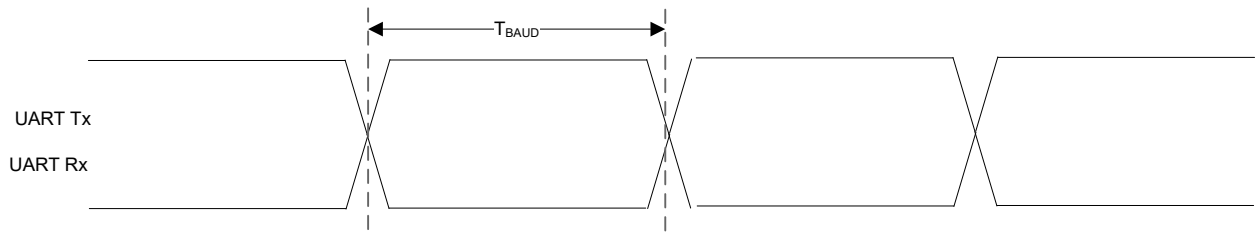

Figure 27. UART timing diagram

Table 47. UART timing data[1] [2]

Over full range of values specified in Section 9 "Recommended operating conditions" unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{BAUD}	Baud time	40 MHz input clock	250	—	—	ns

[1] The acceptable deviation from the UART Rx target baud rate is ±3%.
[2] UART Tx baud rate deviation is determined by the external crystal accuracy. See Section 11.8.1.

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11.5 Audio interface specifications

11.5.1 I2S interface specifications

The I2S pins are powered by VIO voltage supply. See Section 11.1.1 "DC characteristics" for specifications.

Central mode

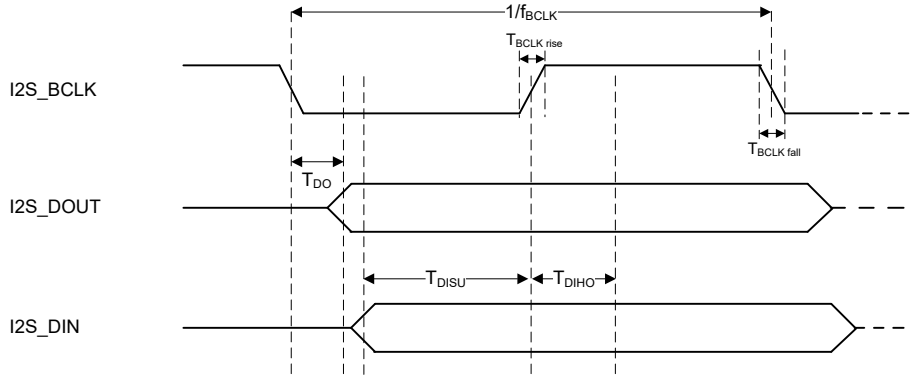

Figure 28. I2S timing specification diagram for data signals—Central mode

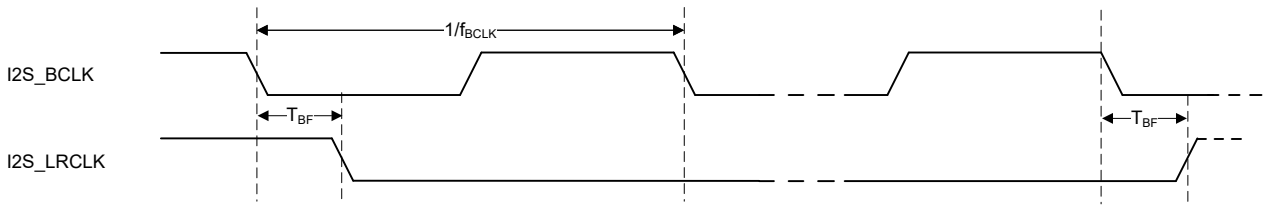

Figure 29. I2S timing specification diagram for clock signals—Central mode

Table 48. I2S timing specification data—Central mode

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{BCLK}	Bit clock frequency	—	1.024	2/2.048	4.096	MHz
Duty $Cycle_{BCLK}$	Bit clock duty cycle	—	45	50	55	%
$T_{BCLK\ rise/fall}$	I2S_BCLK rise/fall time	—	—	3	—	ns
T_{DO}	Delay from I2S_BCLK falling edge to I2S_DOUT rising edge	—	—	—	40	ns
T_{DISU}	Setup time for I2S_DIN before I2S_BCLK rising edge	—	10	—	—	ns
T_{DIHO}	Hold time for I2S_DIN after I2S_BCLK rising edge	—	0	—	—	ns
T_{BF}	Delay from I2S_BCLK falling edge to I2S_LRCLK falling edge	—	—	—	40	ns

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Peripheral mode

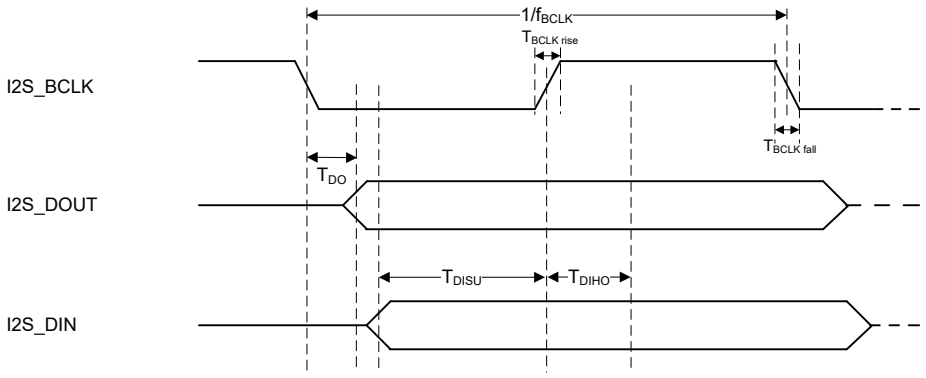

Figure 30. I2S timing specification diagram for data signals—Peripheral mode

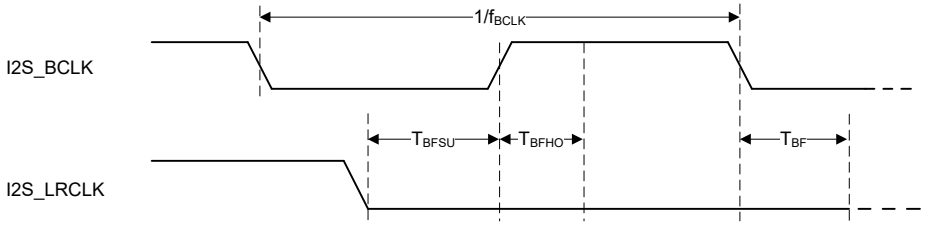

Figure 31. I2S timing specification diagram for clock signal—Peripheral mode

Table 49. I2S timing specification data—Peripheral mode

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{BCLK}	Bit clock frequency	—	1.024	2/2.048	4.096	MHz
Duty $Cycle_{BCLK}$	Bit clock duty cycle	—	45	50	55	%
$T_{BCLK\ rise/fall}$	I2S_CLK rise/fall time	—	—	3	—	ns
T_{DO}	Delay from I2S_BCLK falling edge to I2S_DOUT rising edge	—	—	—	40	ns
T_{DISU}	Setup time for I2S_DIN before I2S_BCLK rising edge	—	10	—	—	ns
T_{DIHO}	Hold time for I2S_DIN after I2S_BCLK rising edge	—	0	—	—	ns
T_{BFSU}	Setup time for I2S_LRCLK before I2S_BCLK rising edge	—	40	—	—	ns
T_{BFHO}	Hold time for I2S_LRCLK after I2S_BCLK rising edge	—	0	—	—	ns

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11.5.2 PCM interface specifications

The PCM pins are powered by VIO voltage supply. See Section 11.1.1 "DC characteristics" for specifications.

Central mode

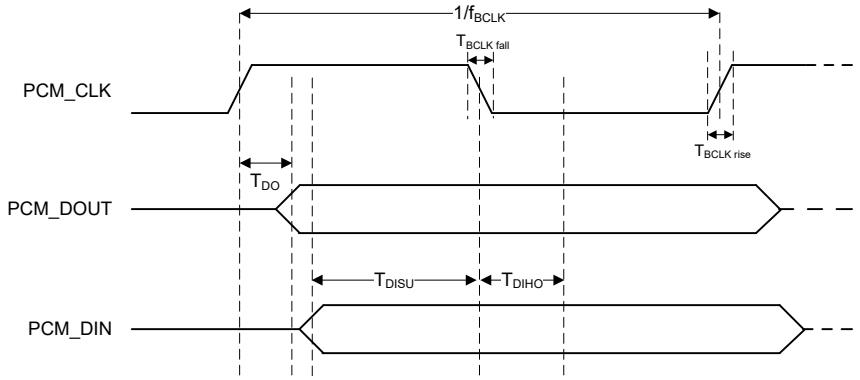

Figure 32. PCM timing specification diagram for data signals—Central mode

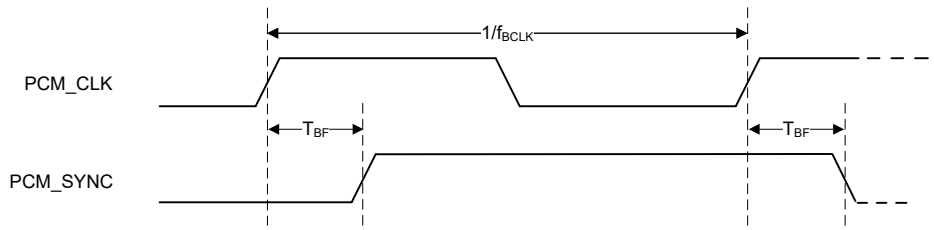

Figure 33. PCM timing specification diagram for PCM_SYNC signal—Central mode

Table 50. PCM timing specification data—Central mode

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{BCLK}	Bit clock frequency	—	2	2/2.048	2.048	MHz
Duty $Cycle_{BCLK}$	Bit clock duty cycle	—	0.4	0.5	0.6	—
$T_{BCLK\ rise/fall}$	PCM_CLK rise/fall time	—	—	3	—	ns
T_{DO}	Delay from PCM_CLK rising edge to PCM_DOUT rising edge	—	—	—	15	ns
T_{DISU}	Setup time for PCM_DIN before PCM_CLK falling edge	—	20	—	—	ns
T_{DIHO}	Hold time for PCM_DIN after PCM_CLK falling edge	—	15	—	—	ns
T_{BF}	Delay from PCM_CLK rising edge to PCM_SYNC rising edge	—	—	—	15	ns

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Peripheral mode

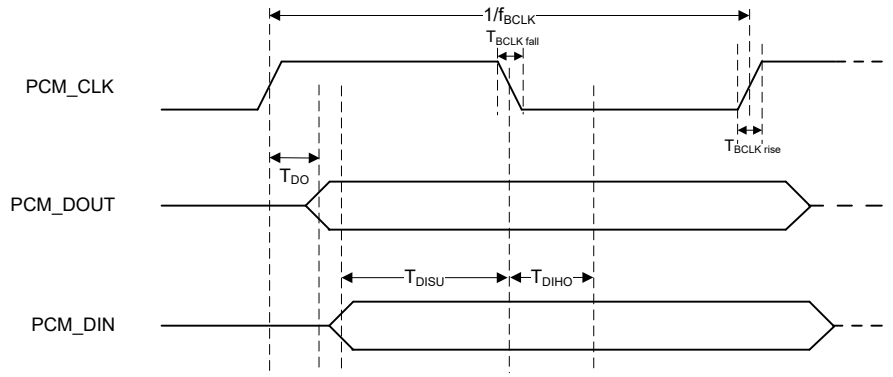

Figure 34. PCM timing specification diagram for data signals—Peripheral mode

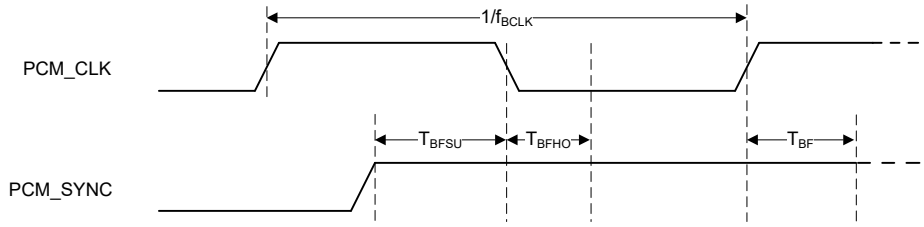

Figure 35. PCM timing specification diagram for PCM_SYNC signal—Peripheral mode

Table 51. PCM timing specification data—Peripheral mode

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{BCLK}	Bit clock frequency	—	0.512[1]	2/2.048	4	MHz
Duty $Cycle_{BCLK}$	Bit clock duty cycle	—	0.4	0.5	0.6	—
$T_{BCLK\ rise/fall}$	PCM_CLK rise/fall time	—	—	3	—	ns
T_{DO}	Delay from PCM_CLK rising edge to PCM_DOUT rising edge	—	—	—	30	ns
T_{DISU}	Setup time for PCM_DIN before PCM_CLK falling edge	—	15	—	—	ns
T_{DIHO}	Hold time for PCM_DIN after PCM_CLK falling edge	—	10	—	—	ns
T_{BFSU}	Setup time for PCM_SYNC before PCM_CLK falling edge	—	15	—	—	ns
T_{BFHO}	Hold time for PCM_SYNC after PCM_CLK falling edge	—	10	—	—	ns

[1] For applications that support dual-WBS (Wide Band Speech) capabilities over Bluetooth, a minimum PCM clock rate of 1.024 MHz is required due to bandwidth considerations. A single–WBS link or dual-NBS link configuration can be supported using a 0.512 MHz PCM clock rate.

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11.6 External radio coexistence interface specifications

11.6.1 WCI-2 coexistence interface specifications

11.6.1.1 WCI-2 interface

WCI-2 is a simplified 2-wire UART interface defined in Bluetooth Core Spec Vol 7 Part C.

Figure 36 shows UART waveform.

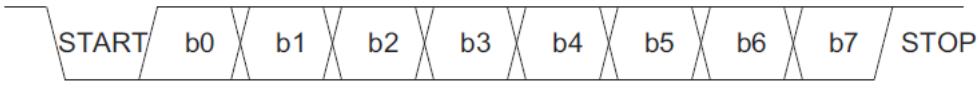

Figure 36. UART waveform

Figure 37 illustrates WCI-2 hardware coexistence interface between IW611 (Wireless SoC) and the external radio.

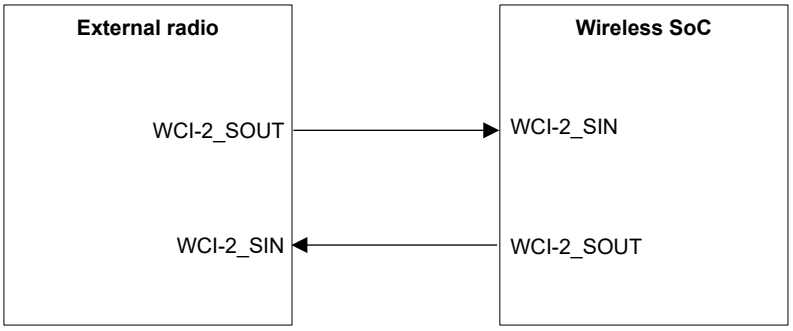

Figure 37. WCI-2 coexistence interface

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11.6.1.2 WCI-2 messages

WCI-2 coexistence interface supports the messages defined in Bluetooth Core Specification Vol 7 Part C for request and grant, where:

- The real time message from the external radio to IW611 indicates the request to operate (Figure 38)
  - MWS_Rx=1 indicates an external radio request to Rx
  - MWS_Tx=1 indicates an external radio request to Tx

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
0	0	0	FRAME_SYNC	MWS_RX	MWS_TX	MWS_PATTERN[0]	MWS_PATTERN[1]

Figure 38. Type 0: Real time signaling message - external radio to IW611

- The external radio can send an optional second message following the real time message to indicate the traffic priority using the vendor specific message (Figure 39). Otherwise, the priority is set via a BCA register.

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
1	1	1	0	MWS_TX_PRI[0]	MWS_TX_PRI[1]	MWS_RX_PRI[0]	MWS_RX_PRI[1]

Figure 39. Type 7: Vendor specific message - external radio to IW611

- The real time message from IW611 to the external radio indicates the arbitration results (Figure 40):
  - BT_Rx_Pri = 1: the Bluetooth radio Rx wins the arbitration and is in operation
  - BT_Tx_On = 1: the Bluetooth radio Tx wins the arbitration and is in operation
  - 802_Rx_Pri = 1: Wi-Fi Rx wins the arbitration and is in operation
  - 802_Tx_On = 1: Wi-Fi Tx wins the arbitration and is in operation
  - Otherwise, the external radio is granted

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
0	0	0	BT_RX_PRI	BT_TX_ON	802_RX_PRI	802_TX_ON	RFU

Figure 40. Type 0: Real time signaling message - IW611 to external radio

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WCI-2 coexistence interface supports the messages defined in Bluetooth Core Specification Vol 7 Part C for other purposes, such as:

- Transport control message from IW611 to the external radio to request real time message upon wake up (Figure 41)

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
0	0	1	Resend_real_time	RFU	RFU	RFU	RFU

Figure 41. Type 1: Transport control message time signaling message - IW611 to external radio

- MWS inactivity duration message from the external radio to IW611 indicates the inactivity duration to IW611 before going to sleep (Figure 42)

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
0	1	1	Duration[0]	Duration[1]	Duration[2]	Duration[3]	Duration[4]

Figure 42. MWS inactivity duration message

- MWS scan frequency message from the external radio to IW611 indicates the external radio scan frequency to IW611 (Figure 43)

Type(0)	Type(1)	Type(2)	MSG(0)	MSG(1)	MSG(2)	MSG(3)	MSG(4)
1	0	0	Freq[0]	Freq[1]	Freq[2]	Freq[3]	Freq[4]

Figure 43. Type 5: MWS scan frequency message

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11.6.1.3 WCI-2 signal waveform format

The messaging is based on a standard UART format.

Figure 44 shows the waveform for the transmit signal (UART_SOUT to UART_SIN).

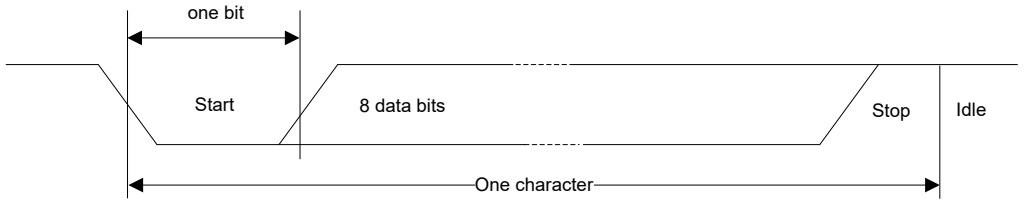

Figure 44. WCI-2 transmit signal waveform

Table 52. WCI-2 interface transport settings

Parameter	Range	Note
Baud rate	921600 ~ 4000000	Baud
Data bits	8	LSB first
Parity bits	0	No parity
Stop bit	1	One stop bit
Flow control	No	No flow control

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11.6.2 PTA interface coexistence specifications

This section illustrates how the central hardware packet traffic arbiter samples the interface signals. The sampling is based on which interface signals are being used.

Figure 45 shows PTA coexistence interface signal timing diagram for the example where:

- Input: request, 1-bit priority
  - Priority ready at Request signal assertion
- Output: grant

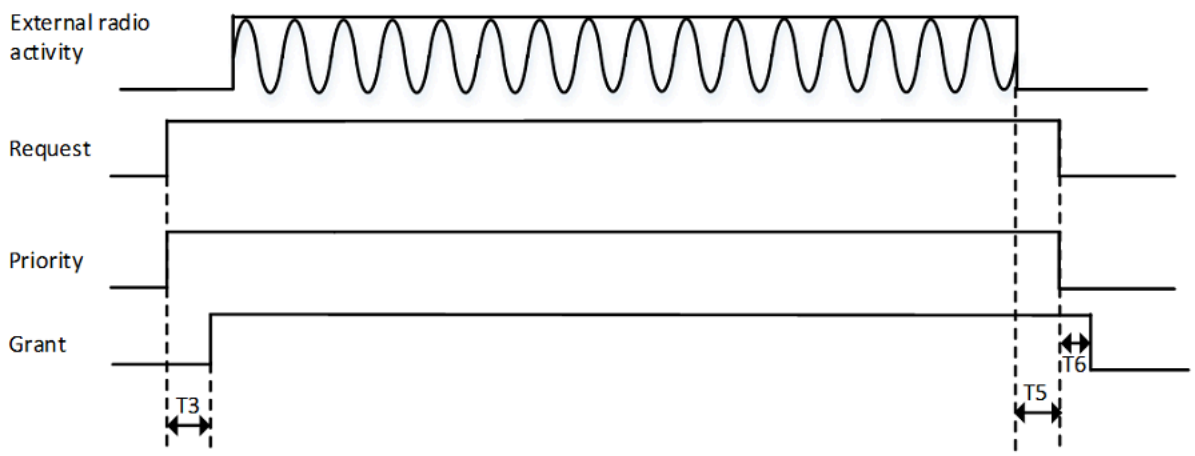

Figure 45. PTA coexistence interface timing diagram - Example 1

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Figure 46 shows PTA coexistence interface timing diagram for the example where:

- Input: request, 1-bit priority, state
  - Priority signal and State signal are ready at Request signal assertion
- Output: grant

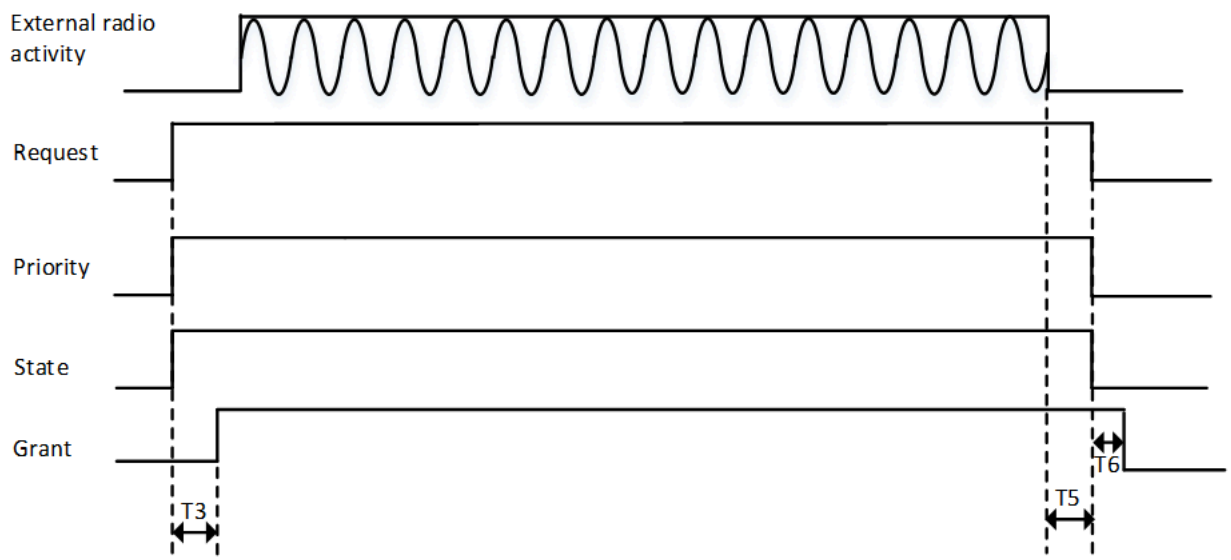

Figure 46. PTA coexistence interface timing diagram - Example 2

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Figure 47 shows PTA coexistence interface timing diagram for the example where:

- Input: request, 1-bit priority, frequency, state
  - Priority, State, and Frequency ready at Request assertion
- Output: grant

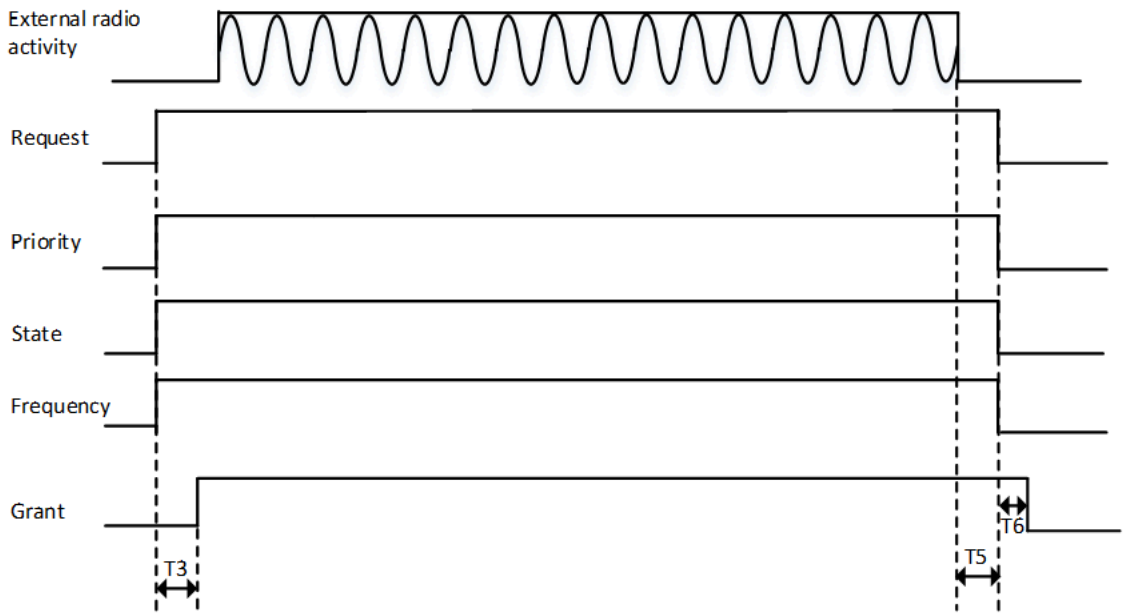

Figure 47. PTA coexistence interface timing diagram - Example 3

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Figure 48 shows PTA coexistence interface timing diagram for the example where:

- Input: request, 1-bit priority
  - Priority signal is ready at Request signal assertion
- Output: grant
  - Grant signal is de-asserted before Request signal de-assertion due to a traffic abort caused by other traffic with higher priority

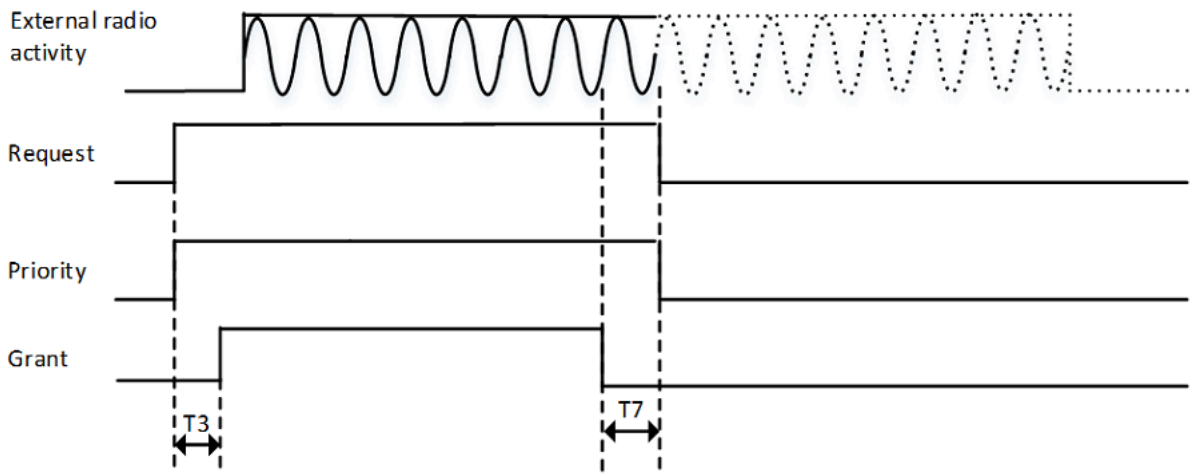

Figure 48. PTA coexistence interface timing diagram - Example 4

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Figure 49 shows PTA coexistence interface timing diagram for the example where:

- Input: request and priority
  - Priority pin is sampled three times to obtain two priority bits and Tx/Rx info. No input from State pin.
- Output: grant

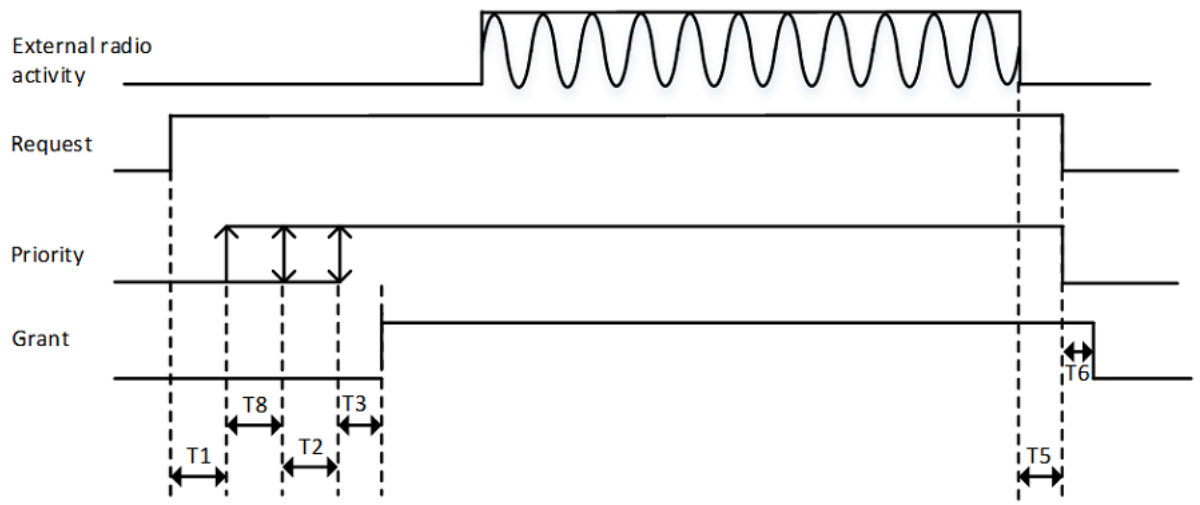

Figure 49. PTA coexistence interface timing diagram - Example 5

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Table 53 provides the timing specifications for PTA coexistence interface signals.

Table 53. PTA coexistence interface signal timing data

Paramete	Conditions	Min	Typ.	Max	Unit
T1[1]	Priority[0] is sampled on Priority pin at T1 from Request assertion.	0	—	100	µs
T8[1]	Optional: priority[1], if present on Priority pin, is sampled at T1+T8 from Request assertion.	0.025	—	100	µs
T2[1]	Optional: Tx/Rx Info, if present on Priority pin, is sampled at T1+T2 (one priority bit on Priority pin) or T1+T8+T2 (two priority bits on Priority pin) from Request assertion.	0.025	—	100	µs
T3[2]	Time from all information available to BCA to grant decision ready	0.1	—	0.4	µs
T5[2]	The Request signal de-asserts T5 after the last symbol is done	—	—	—	µs
T6[2]	The Grant signal de-asserts T6 after the Request de-assertion	0.1	—	0.3	µs
T7[2]	The Request signal de-asserts T7 after the grant de-assertion due to a traffic abort.	—	—	—	µs

[1] Valid for serially sampled Priority pin
[2] Valid for all implementations

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11.7 Host configuration specifications

For a list of configuration pins, see Section 6.8 "Configuration pins".

Table 54. Configuration pin specifications[1]

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Units
Internal weak pull-up resistance	Around 1 ms following any reset	--	800	--	kΩ
Internal nominal pull-up resistance	Around 1 ms following any reset	--	100	--	kΩ

[1] After approximately 1 ms, the configuration pins become functional pins.

11.8 Reference clock specifications

11.8.1 External crystal specifications

Table 55. External crystal specifications

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
Fundamental frequencies	—	—	40	—	MHz
Resonance mode	—	—	A1, Fundamental	—	—
Equivalent differential load capacitance	—	7	8	9	pF
Shunt capacitance	—	—	2	—	pF
Frequency tolerance	Over process at 25ºC	—	±10	—	ppm
Frequency stability	Over operating temperature	—	±10	—	ppm
Aging	—	—	±2	—	ppm/ 5 years
Series resistance (ESR)	40 MHz	—	—	40	Ω
Insulation resistance	at DC 100V	500	—	—	MΩ
Maximum drive level	—	120	—	—	µW

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11.8.2 External crystal oscillator specifications

The reference clock from the external crystal oscillator requires a CMOS input signal or a clipped sinusoidal signal.

Table 56. Clock DC specifications[1]

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
Single-ended high-level voltage	—	—	—	1.8	V
Single-ended low-level voltage	—	0	—	—	V
Clock amplitude (pk-pk)[2]	—	0.5	—	1	V
Mid-point slope	—	125	—	—	MV/s

[1] AC-coupling capacitor is integrated into the SoC.
[2] Minimum 0.8V for clipped sinusoidal signal.

Table 57. 40 MHz clock timing

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
XO40 period	—	25.00 - 20 ppm	25.00	25.00 + 20 ppm	ns
XO40 rise time	—	—	—	2.00	ns
XO40 fall time	—	—	—	2.00	ns
XO40 duty cycle	—	47	50	53	%

Table 58. Phase noise

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Parameter	Test Conditions	Min	Typ	Max	Unit
Fref = 40 MHz	Offset = 1 kHz	—	—	-130	dBc/Hz
	Offset = 10 kHz	—	—	-145	dBc/Hz
	Offset = 100 kHz	—	—	-155	dBc/Hz
	Offset > 1 MHz	—	—	-162	dBc/Hz

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11.9 Power-down specifications

11.9.1 PDn asserted low—Power supplies remain high

The following table and figure show the specifications for the PDn signal when it is asserted (low) while all power supplies to the device are high. After PDn is deasserted (high), the device takes 20 ms to get ready for SDIO enumeration.

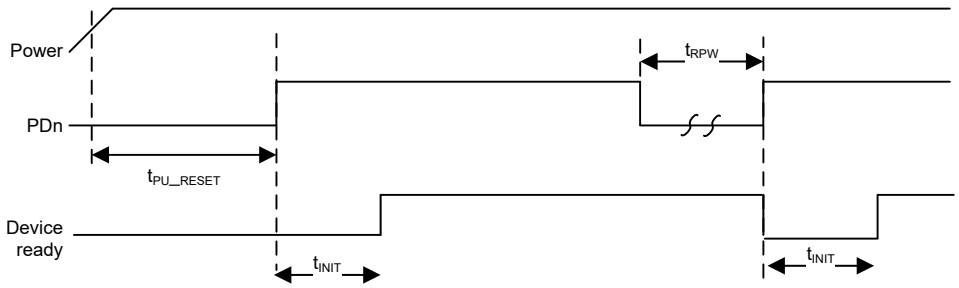

Figure 50. PDn Pin (Power-down) timing—Power remains high at PDn assertion

Table 59. PDn pin (Power-down) specifications—Power remains high at PDn assertion

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_{PU_RESET}	Valid power to PDn de-asserted	—	0	—	—	ms
t_{RPW}	PDn pulse width	—	1[1]	—	—	µs
t_{INIT}	From PDn de-assertion to device ready (SDIO bus enumeration)	—	20	—	—	ms
V_{IH}	Input high voltage	—	1.4	—	4.5	V
V_{IL}	Input low voltage	—	-0.4	—	0.5	V

[1] Minimum value guaranteed for a valid reset. Smaller values may put the device in an undefined state.

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11.10 JTAG interface specifications

The test interface pins are powered by VIO voltage supply.

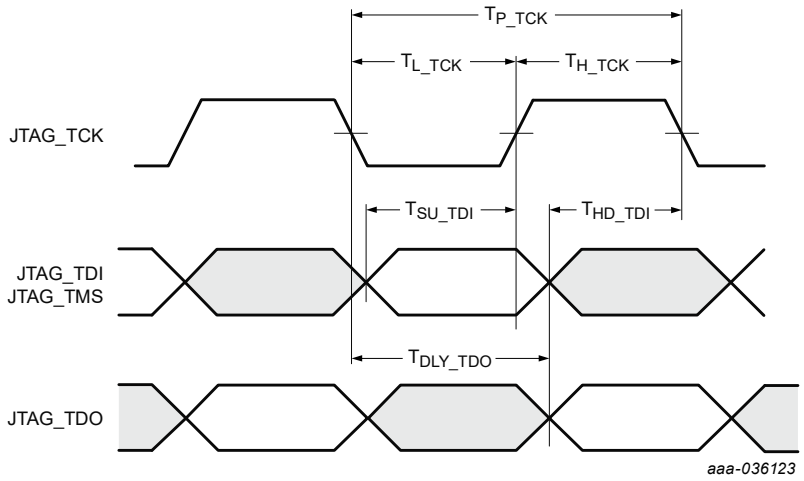

Figure 51. JTAG timing diagram

Table 60. JTAG interface protocol timing[1]

Unless otherwise specified, the values apply per Section 9 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_TCK}	TCK period	—	25	—	—	ns
T_{H_TCK}	TCK high	—	12	—	—	ns
T_{L_TCK}	TCK low	—	12	—	—	ns
T_{SU_TDI}	TDI, TMS to TCK setup time	—	5	—	—	ns
T_{HD_TDI}	TDI, TMS to TCK hold time	—	5	—	—	ns
T_{DLY_TDO}	TCK to TDO delay	—	0	—	7.5	ns

[1] Does not apply to JTAG enabled by the JTAG_TMS pin.

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12 Package information

12.1 Package thermal conditions

12.1.1 HVQFN116 thermal conditions

Table 61. Package thermal conditions—HVQFN116

Symbol	Rating	Board type[1]	Value	Unit
Rthj-a/θja	Junction to ambient thermal resistance[2]	JESD51-7, 2s2p board		°C/W
Psij-top/Ψj-top	Junction to top of package thermal characterization parameter[2]	JESD51-7, 2s2p board		°C/W
Rthj-c/θjc	Junction to case thermal resistance[2]	JESD51-7, 1s board		°C/W

[1] The thermal test board meets JEDEC specification for this package (JESD51-7).
[2] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

12.1.2 WLCSP140 thermal conditions

Table 62. Package thermal conditions—WLCSP140

Symbol	Rating	Board type[1]	Value	Unit
Rthj-a/θja	Junction to ambient thermal resistance[2]	JESD51-9, 2s2p board	37.5	°C/W
Psij-top/Ψj-top	Junction to top of package thermal characterization parameter[2]	JESD51-9, 2s2p board	0.1	°C/W
Rthj-c/θjc	Junction to case thermal resistance[2]	JESD51-9, 1s board	10.0	°C/W

[1] The thermal test board meets JEDEC specification for this package (JESD51-9).
[2] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

12.2 WLCSP underfill

To meet NXP board level reliability (BLR) requirements of 500 temperature cycles between -40°C to +125°C (Ta), and prevent WLCSP reliability issues, it is mandatory to select a molded underfill (for molded module application) or capillary underfill material (for unmolded module applications). The molded underfill or capillary underfill material must have less than 20 ppm halide like chloride as per the material supplier specifications.

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12.3 Package mechanical drawing

Table 63. Package information

Package name	Link to package information on NXP website
HVQFN116	SOT2086-1
WLCSP140	SOT2126-1

Table 64. Packing information

Package name	Link to packing information on NXP website
HVQFN116 (tray)	SOT2086-1_557
HVQFN116 (tape and reel)	SOT2086-1_528
WLCSP140 (tape and reel)	SOT2126-1_092

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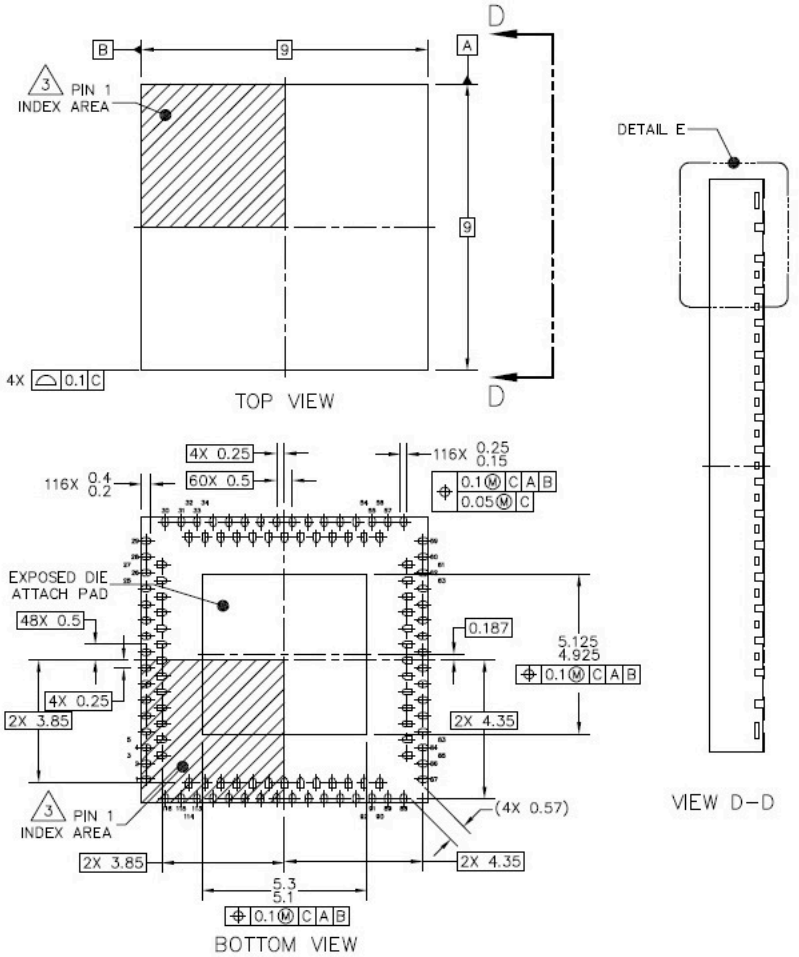
12.3.1 HVQFN mechanical drawing



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH PAD.
5. MIN. METAL GAP FOR LEAD TO EXPOSED PAD SHALL BE 0.2 MM.

Figure 52. HVQFN116 package drawing

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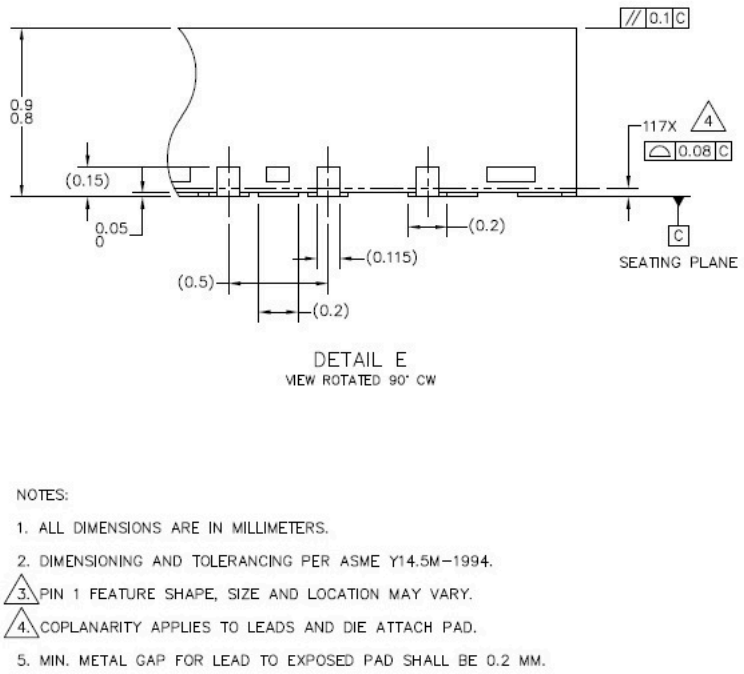

Figure 53. HVQFN116 package drawing - Details E

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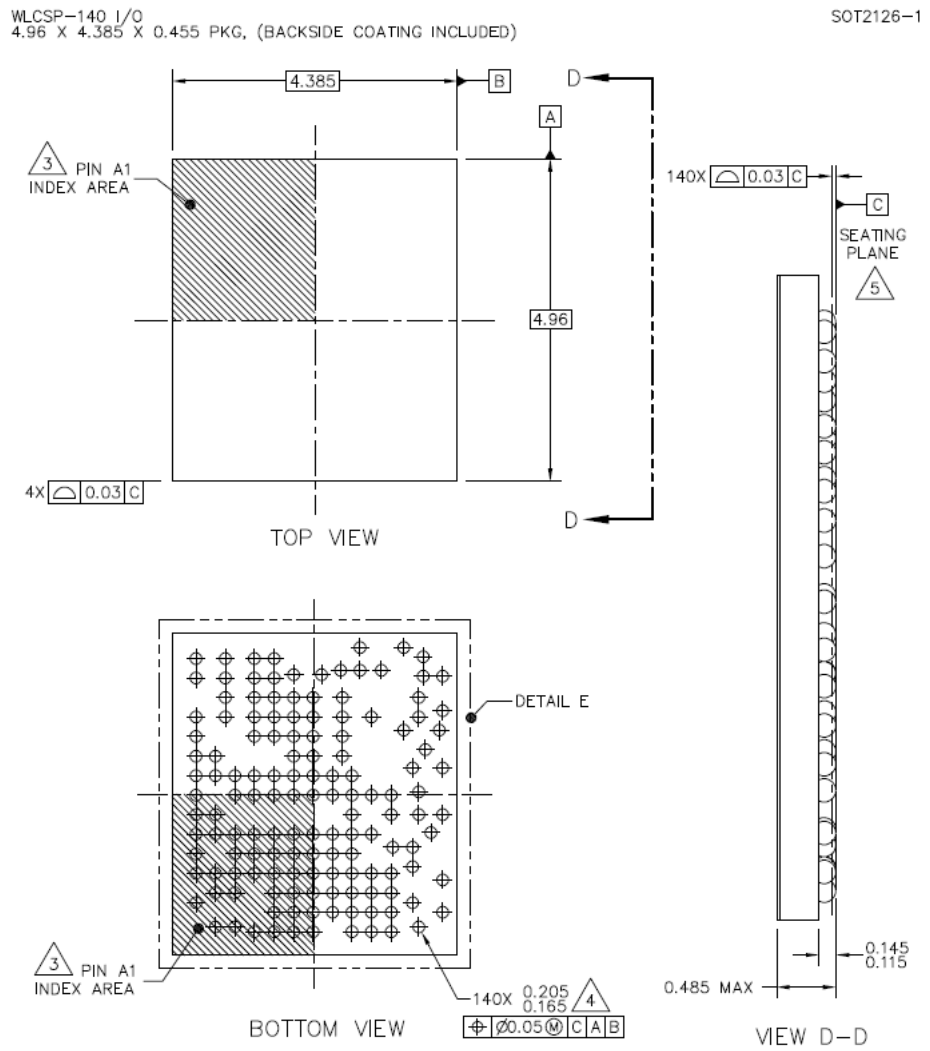
12.3.2 WLCSP mechanical drawing



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

Figure 54. WLCSP140 package drawing

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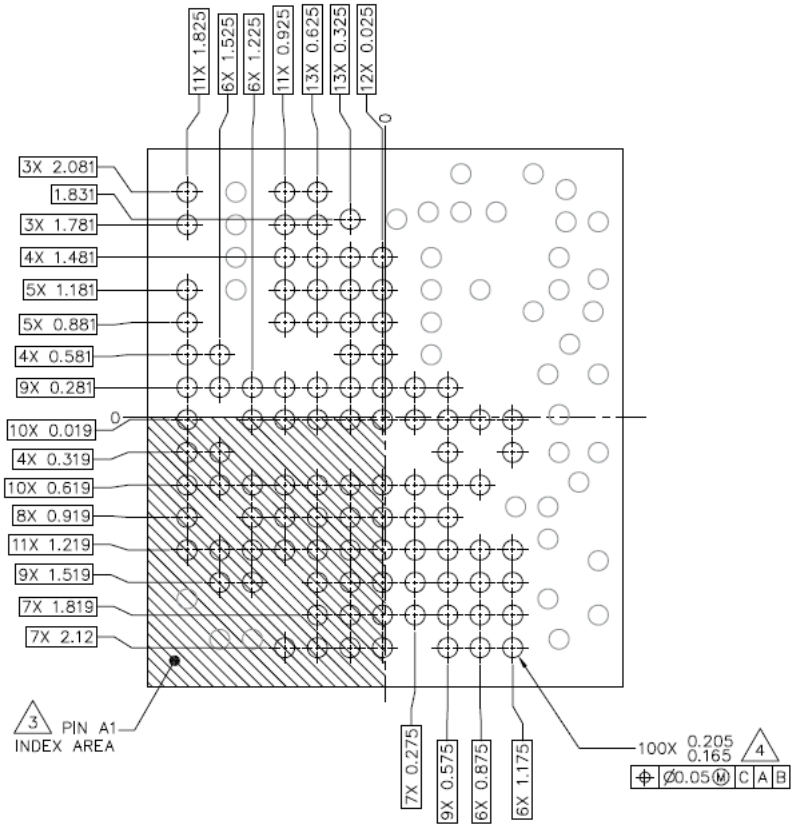

DETAIL E (I)
(ARRAY BUMPS (100X))

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

Figure 55. WLCSP140 package drawing - Details E (I) - Array bumps (not to scale)

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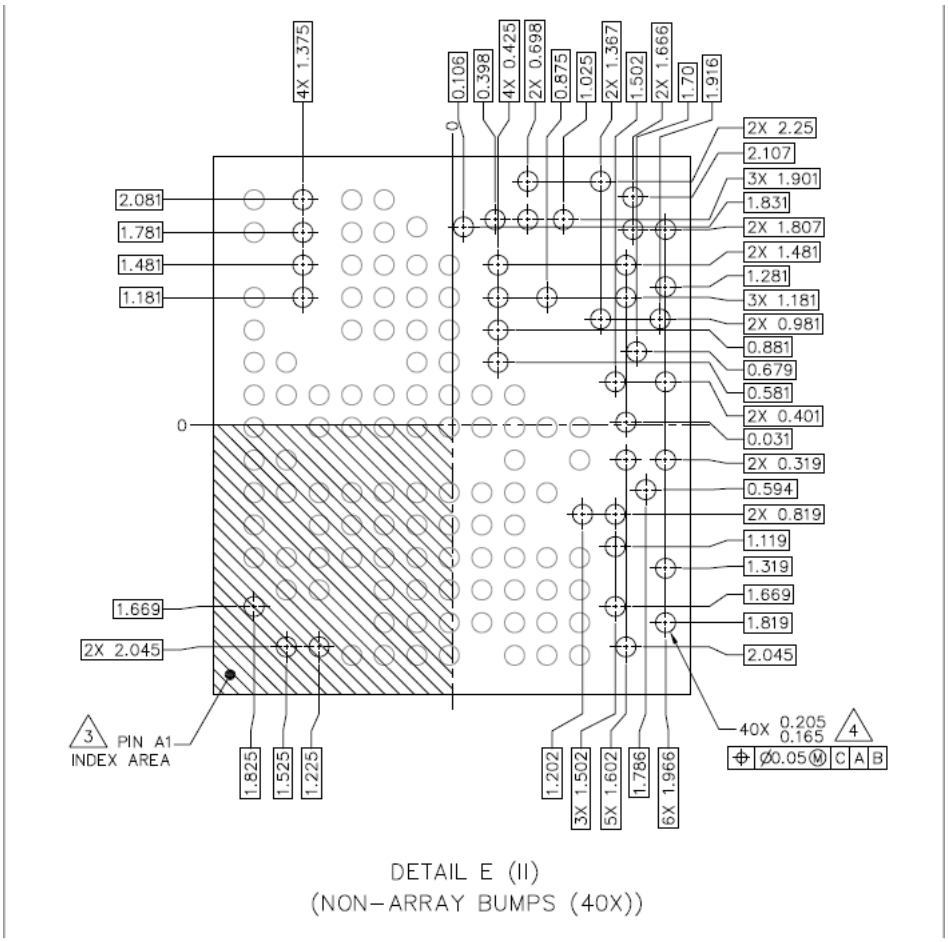

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

Figure 56. WLCSP140 package drawing - Details E (II) - Non-array bumps (not to scale)

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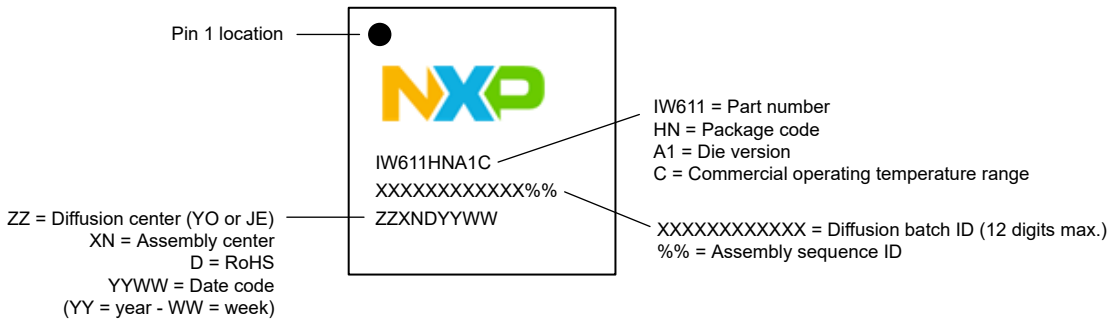
12.4 Package marking

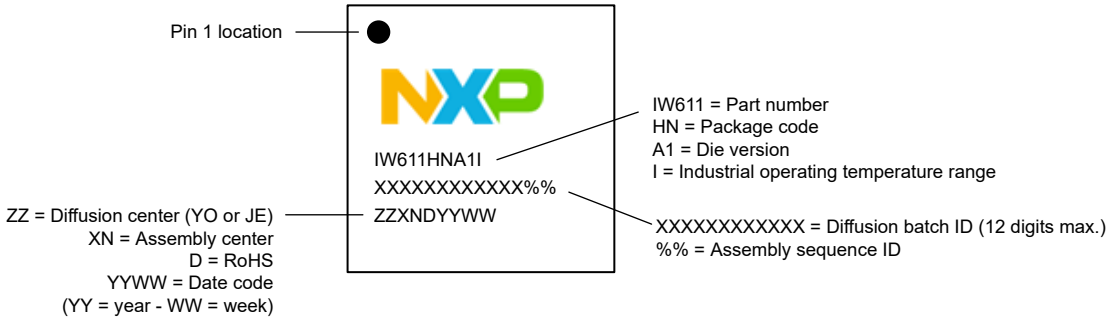
12.4.1 HVQFN marking

Figure 57 and Figure 58 show the location of pin 1 and describe each line of the package marking on HVQFN116.



Note: The above drawing is not drawn to scale. The location of markings is approximate.

Figure 57. IW611 package marking and pin 1 location—HVQFN116, commercial operating temperature



Note: The above drawing is not drawn to scale. The location of markings is approximate.

Figure 58. IW611 package marking and pin 1 location—HVQFN116, industrial operating temperature

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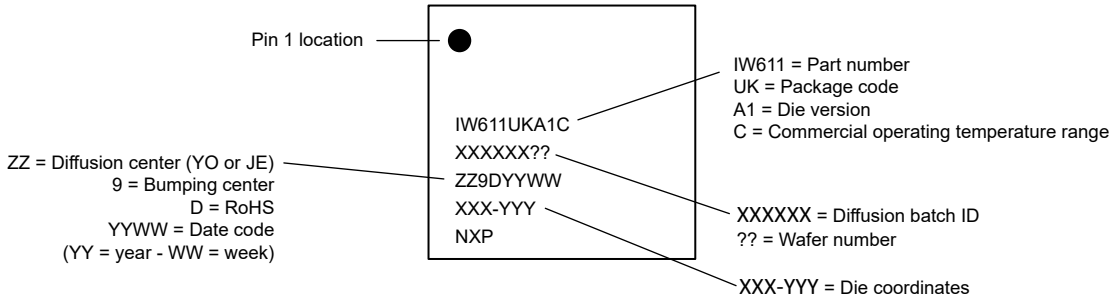
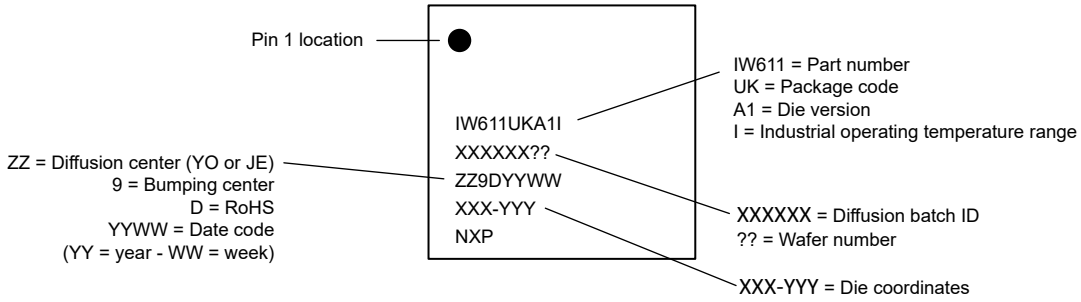
12.4.2 WLCSP marking

Figure 59 and Figure 60 show the location of pin 1 and describe each line of the package marking on WLCSP140.



Note: The above drawing is not drawn to scale. The location of markings is approximate.

Figure 59. IW611 package marking and pin 1 location—WLCSP140, commercial operating temperature



Note: The above drawing is not drawn to scale. The location of markings is approximate.

Figure 60. IW611 package marking and pin 1 location—WLCSP140, industrial operating temperature

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13 Abbreviations

Table 65. Abbreviations

Abbreviation	Definition
A2DP	Advanced audio distribution profiles
ACK	Acknowledgment
ADC	Analog-to-digital converter
AES	Advanced encryption standard
AFH	Adaptive frequency hopping
AGC	Automatic gain control
AP	Access point
Arm	Advanced RISC machine
BDR	Basic data rate
BOM	Bill of materials
BRF	Bluetooth RF unit
BSS	Basic service set
BTM	BSS transition management
CBC	Cipher block chaining
CCA	Clear channel assessment
CCK	Complementary code keying
CCMP	Counter mode CBC-MAC protocol
CMD	Command
CRC	Cyclic redundancy check
CTS	Clear to send
DAC	Digital-to-analog converter
DCF	Distributed coordination function
DFS	Dynamic frequency selection
DMA	Direct memory access
DPD	Digital pre distortion
DQPSK	Differential quadrature phase shift keying
DTIM	Delivery traffic indication message
EAP	Extensible authentication protocol
ED	Energy detect
EDCA	Enhanced distributed channel access
FIFO	First in first out
GATT	Generic attribute profile
GCMP	Galois/counter mode protocol
GI	Guard interval

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Table 65. Abbreviations...*continued*

Abbreviation	Definition
GPIO	General purpose input/output
HID	Human interface device
HT	High throughput
HVQFN	Thermal enhanced very thin quad flat package
HW	Hardware
I/F	Interface
I/Q	In-phase/quadrature
IEEE	Institute of electrical and electronics engineers
JEDEC	Joint electronic device engineering council
JTAG	Joint test action group
LC3	Low complexity communication codec
LDPC	Low density parity check
LE	Low energy
LED	Light emitting diode
LNA	Low noise amplifier
LSB	Least significant byte
LTE	Long term evolution
MAC	Media/medium access controller
MCS	Modulation and coding scheme
MFP	Multi functional pin
MIMO	Multiple input multiple output
MPDU	MAC protocol data unit
MSb	Most significant bit
MSB	Most significant byte
MU-MIMO	Multi user MIMO
MU-PPDU	Multi user PPDU
MWS	Mobile wireless system Multimedia wireless system
NAV	Network allocation vector
NBS	Narrow band speech
NDP	Null data packet
Nsts	Number of space time streams
OFDM	Orthogonal frequency division multiplexing
OFDMA	Orthogonal frequency division multiple access
OTP	One time programmable
OTT	Over-the-top (device)

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Table 65. Abbreviations...*continued*

Abbreviation	Definition
PA	Power amplifier
PCI	Peripheral component interconnect
PCM	Pulse code modulation
PDn	Power down
PHY	Physical layer
POS	Point of sale
PPDU	PHY protocol data unit
PSK	Pre shared keys
PTA	Packet traffic arbitration
QAM	Quadrature amplitude modulation
QFN	Quad flat non-leaded package
RF	Radio frequency
RIFS	Reduced inter frame space
RISC	Reduced instruction set computer
RSSI	Receiver signal strength indication
RTC	Real time clock
RTS	Request to send
SISO	Single input single output
SoC	System-on-chip
SPDT	Single pole double throw
SPI	Serial peripheral interface
STA	Station
TA	Transmitter address
TCP/IP	Transmission control protocol/internet protocol
TKIP	Temporal key integrity protocol
TWT	Target wait time
UART	Universal asynchronous receiver/transmitter
UDP	User datagram protocol
VHT	Very high throughput
WAP	Wireless application protocol
WBS	Wide band speech
WCI-2	Wireless coexistence interface 2
WEP	Wired equivalent privacy
Wi-Fi	Hardware implementation of IEEE 802.11 for wireless connectivity
WLAN	Wireless local area network
WLCSP	Wafer level chip scale package

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Table 65. Abbreviations*...continued*

Abbreviation	Definition
WPA	Wi-Fi protected access
WPA2	Wi-Fi protected access 2
WPA2-PSK	Wi-Fi protected access 2 - pre shared key
WPA3	Wi-Fi protected access 3
WPA-PSK	Wi-Fi protected access - pre shared key
XOSC	Crystal oscillator

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14 Revision history

Table 66. Revision history

Document ID	Release date	Description
IW611 v.7.0	20 March 2025	Product data sheet. PCN number: 202405001F01. Updated the title. **Radio specifications** • Section 10.1.3 "5 GHz Wi-Fi receiver performance": replaced "20 MHz MCS9 Nss1 LDPC" with "20 MHz MCS8 Nss1 LDPC"for Receiver ACI 802.11ac and for Receiver AACI 802.11ac. • Section 10.1.4 "2.4 GHz Wi-Fi transmitter performance": – Corrected the unit for *Transmit output power level control range* parameter. – Updated the conditions for *Transmit output power accuracy* parameter. – Corrected the unit for *Transmit carrier suppression* parameter. – Updated the conditions for *Transmit frequency error* parameter. • Section 10.1.5 "5 GHz Wi-Fi transmitter performance": – Updated the conditions for *Transmit output power accuracy* parameter. – Corrected the unit for *Transmit carrier suppression* parameter. – Updated the conditions for *Transmit frequency error* parameter. • Section 10.3 "Current consumption ": updated PDn value for 3.3V power rail. **Electrical specifications** • Section 11.3.4 "SDR104 mode (208 MHz) (1.8V)": updated T_{OP} unit. • Section 11.5.1 "I2S interface specifications": updated. • Section 11.8.2 "External crystal oscillator specifications": moved the footnote about the minimum voltage value for clipped sinusoidal signal to *Clock amplitude* parameter. **Package information** • Section 12.4.2 "WLCSP marking": updated the diffusion center.

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Table 66. Revision history...*continued*

Document ID	Release date	Description
IW611 v.6.0	13 September 2024	Product data sheet • Access to the document changed to "Public". **Product overview** • Section 1 "Product overview": updated Bluetooth version to 5.4. • Section 1.3 "Bluetooth key features": updated Bluetooth certified version to 5.4. **Bluetooth subsystem** • Section 4.1 "Bluetooth features": updated the versions of Bluetooth features supported and Bluetooth certified. • Section 4.2 "Bluetooth Low Energy (LE) features": updated the versions of Bluetooth features supported and Bluetooth certified. • Section 4.4.2 "PCM interface": – Removed the support of long frame synchronization. – Removed the support of PCM bit width size of 8 bits. **Wi-Fi subsystem** • Section 3.2 "Wi-Fi MAC": removed the feature "MU Ackowlegment (ACK)". • Section 3.3 "Wi-Fi baseband ": removed *Spectral intelligence"*. • Section 3.5 "RF channels": removed 4.9 GHz channels. **Pin information** • Section 6.1 "Signal diagram": removed the arrows for XTAL_IN and XTAL_OUT signals. • Section 6.7.2 "General purpose I/O (GPIO) (MFP)": added BLE ISOC trigger mode to GPIO[23] and GPIO[27]. • Section 6.7.14 "Clock interface": removed the reference to external crystal oscillator. **Power information** • Figure 18 "Internal buck connections - HVQFN package": added a 0.1 Ω resistance. **Radio specifications** • Section 10.1.2 "2.4 GHz Wi-Fi receiver performance": added a footnote about the measurement of *Receiver maximum input level DSSS* parameter. • Section 10.1.3 "5 GHz Wi-Fi receiver performance": updated the minimum value of RF frequency range. • Section 10.1.4 "2.4 GHz Wi-Fi transmitter performance": corrected the unit of *Transmit output power accuracy*, and remove the table footnotes for transmit output power accuracy. • Section 10.1.5 "5 GHz Wi-Fi transmitter performance": – Updated the minimum value of RF frequency range. – Corrected the unit of *Transmit output power control range* parameter. – Corrected the unit of *Transmit output power accuracy*. • Removed the section *Local oscillator*. • Section 10.2.2 "Bluetooth/Bluetooth LE transmitter performance": – Updated the value and description of *Transmit output power accuracy (BDR)* parameter. – Updated the description of *Transmit output power control step* parameter. – Updated the value of *Transmit output power accuracy (EDR)* parameter. – Updated the value of *Transmit output power level control range (EDR)* parameter. ———— Continues ————

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Table 66. Revision history...*continued*

Document ID	Release date	Description
IW611 v.6.0	13 September 2024	———— Continued ———— **Radio specifications** • Section 10.3 "Current consumption ": – Added the values for Bluetooth LE link mode. – Removed the rows for Bluetooth LE peak transmit at 20 dBm and 21 dBm. – Updated the conditions for Bluetooth current consumption. – Removed the rows for Bluetooth peak transmit at 20 dBm and 21 dBm. – Updated the conditions for 802.15.4 current consumption. – Changed the clock speed to 50 MHz for DTIM IEEE with SDIO 2.0. – Updated the footnote and mode description in IEEE power save mode section. – Updated DTIM values. – Added the values for target wake time (TWT). – Updated the parameter description and values for the last item in the peak current section. – Added a footnote about output power in the peak current section. **Electrical specifications** • Section 11.1.1.2 "3.3V operation": added V_{OH} and V_{OL}. • Section 11.3.3 "SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8V)": – Changed the minimum value of SDR12 and SDR25 input setup time. – Changed the minimum value of SDR12 and SDR25 input hold time. • Section 11.8.1 "External crystal specifications": Renamed "Drive level"as "Maximum drive level". • Section 11.8.2 "External crystal oscillator specifications": – Added *or clipped sinusoidal signal* to the sentence about the table. – Added a table footnote to *Single-ended low-level voltage* parameter. – Changed the maximum value of Fref = 40 MHz, offset = 100 kHz, in the table *Phase noise*. **Acronyms** • Section 13 "Abbreviations": updated.
IW611 v.5.0	30 June 2024	Product data sheet **Package information** • Figure 57 "IW611 package marking and pin 1 location—HVQFN116, commercial operating temperature": updated • Figure 58 "IW611 package marking and pin 1 location—HVQFN116, industrial operating temperature": updated • Figure 59 "IW611 package marking and pin 1 location—WLCSP140, commercial operating temperature": updated • Figure 60 "IW611 package marking and pin 1 location—WLCSP140, industrial operating temperature": updated
IW611 v.4.0	27 February 2023	Product data sheet

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