A6G35S006N

Airfast RF Power GaN Transistor

Rev. 2 — 13 January 2025 **Product data sheet**

1 General description

This 28 dBm average, 10 W peak RF power GaN transistor is designed for cellular base station applications covering the frequency range of 2496 to 5000 MHz.

2 Features and benefits

- High terminal impedances for optimal broadband performance
- Designed for low complexity linearization systems
- Universal broadband driver
- Optimized for massive MIMO active antenna systems for 5G base stations

3 Typical performance

Table 1. 3500 MHz — Typical single-carrier W-CDMA reference circuit performance

V_{DD} = 48 Vdc, I_{DQ} = 18 mA, P_{out} = 28 dBm Avg., input signal PAR = 9.9 dB @ 0.01 % probability on CCDF.[1]

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
3300 MHz	21.1	18.5	9.9	-39.5
3400 MHz	21.1	19.0	9.8	-39.5
3500 MHz	21.0	19.7	9.7	-39.6
3600 MHz	20.6	20.2	9.6	-40.1
3670 MHz	20.4	20.7	9.5	-39.7

[1] All data measured with device soldered to NXP reference circuit.

Table 2. 3900 MHz — Typical single-carrier W-CDMA performance

V_{DD} = 48 Vdc, I_{DQ} = 18 mA, P_{out} = 28 dBm Avg., input signal PAR = 9.9 dB @ 0.01 % probability on CCDF.[1]

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
3670 MHz	19.7	18.5	9.8	-43.1
3700 MHz	20.2	18.8	9.8	-42.8
3800 MHz	20.8	19.4	9.6	-44.0
3900 MHz	20.6	19.9	9.5	-44.3
4000 MHz	20.2	20.7	9.4	-44.2
4100 MHz	20.0	21.7	9.3	-44.8

[1] All data measured with device soldered to circuit.

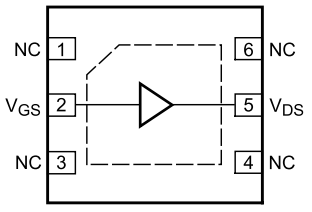
Table 3. 4900 MHz — Typical single-carrier W-CDMA performance

V_{DD} = 48 Vdc, I_{DQ} = 19 mA, P_{out} = 28 dBm Avg., input signal PAR = 9.9 dB @ 0.01 % probability on CCDF.[1]

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
4800 MHz	17.5	17.2	9.3	-44.2
4900 MHz	18.0	17.5	8.7	-46.2
5000 MHz	17.7	17.3	8.6	-48.3

[1] All data measured with device soldered to circuit.

4 Pinning information



(Top view)

Note: Exposed backside of the package is the source terminal for the transistor.

aaa-042956

Figure 1. Pin configuration

5 Ordering information

Table 4. Ordering information

Device	Tape and Reel Information	Package
A6G35S006NT6	T6 Suffix = 5,000 Units, 12 mm Tape Width, 13-inch Reel	DFN 4.5 × 4

6 Product marking

Figure 2. Product marking

Table 5. Product marking trace code

Identifier	Description
AA	Assembly location
L	Wafer lot indicator
YW	Date code
ZZ	Assembly lot

7 Limiting values

Table 6. Limiting values

Symbol	Parameter	Conditions	Value	Unit
V_{DSS}	Drain-source voltage		125	Vdc
V_{GS}	Gate-source voltage		-8, 0	Vdc
V_{DD}	Operating voltage		55	Vdc
I_{GMAX}	Maximum forward gate current	T_C = 25 °C	1.2	mA
T_{stg}	Storage temperature range		-65 to +150	°C
T_{CH}	Maximum channel temperature		225	°C

8 Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Value	Unit
V_{DD}	Operating voltage		48	Vdc

9 Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{\theta SC}$ (IR)	Thermal resistance by infrared measurement, active die surface-to-case	Case temperature 113 °C, $P_{D\text{-}Global}$ = 3.8 W	9.5[1]	°C/W
$R_{\theta CHC}$ (FEA)	Thermal resistance by finite element analysis, channel-to-case	Case temperature 113 °C, P_D = 3.5 W	21.1[1][2]	°C/W

[1] Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to https://www.nxp.com/RF and search for AN1955.
[2] $R_{\theta CHC}$ (FEA) must be used for purposes related to reliability and limitations on maximum channel temperature. MTTF may be estimated by the expression MTTF (hours) = $10^{[A + B/(T + 273)]}$, where T is the channel temperature in degrees Celsius, A = -12.47 and B = 9729.

10 ESD protection characteristics

Table 9. ESD protection characteristics

Test methodology	Class
Human Body Model (per JS-001-2023)	0B
Charge Device Model (per JS-002-2022)	C2A

11 Moisture sensitivity level

Table 10. Moisture sensitivity level

Test methodology	Rating	Package peak temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

12 Electrical characteristics

12.1 DC characteristics — off characteristics

Table 11. DC characteristics — off characteristics

(T_A = 25 °C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{D(BR)}$	Off-state drain leakage	V_{DS} = 150 Vdc, V_{GS} = -8 Vdc	-	-	0.2	mAdc
I_{GLK}	Off-state gate leakage	V_{DS} = 48 Vdc, V_{GS} = -8 Vdc	-0.1	-	-	mAdc

12.2 DC characteristics — on characteristics

Table 12. DC characteristics — on characteristics

(T_A = 25 °C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = 10 Vdc, I_D = 1.1 mAdc	-4.6	-2.4	-1.85	Vdc
$V_{GS(Q)}$	Gate quiescent voltage	V_{DD} = 48 Vdc, I_D = 19 mAdc[1]	-3.2	-2.8	-2.5	Vdc
I_{GSS}	Gate-source leakage current	V_{DS} = 150 Vdc, V_{GS} = -8 Vdc	-0.2	-	-	mAdc

[1] Measured in functional test.

12.3 Functional tests

Table 13. Functional tests

(In NXP production ATE[1] test fixture, T_A = 25 °C unless otherwise noted, 50 ohm system)[2] V_{DD} = 48 Vdc, I_{DQ} = 19 mA, P_{out} = 28 dBm Avg., f = 3670 MHz, 1-tone CW.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_{ps}	Power gain		14.5	16.8	20.0	dB
η_D	Drain efficiency		15.5	17.4	-	%
P_{sat}	Saturated power	Pulsed CW, 5 % duty cycle	38.8	39.4	-	dBm

[1] ATE is a socketed test environment.
[2] Internally unmatched part.

12.4 Wideband ruggedness

Table 14. Wideband ruggedness

(In NXP reference circuit, T_A = 25 °C unless otherwise noted, 50 ohm system)[1] I_{DQ} = 18 mA, f = 3500 MHz, Additive White Gaussian Noise (AWGN) with 10 dB PAR.

Characteristic	Test results
ISBW of 400 MHz at 55 Vdc, 8.7 W Avg. modulated output power (3 dB input overdrive from 1.3 W Avg. modulated output power)	No device degradation

[1] All data measured with device soldered to NXP reference circuit.

12.5 Typical performance

Table 15. Typical performance

(In NXP reference circuit, T_A = 25 °C unless otherwise noted, 50 ohm system)[1] V_{DD} = 48 Vdc, I_{DQ} = 18 mA, 3300–3670 MHz bandwidth.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pulsed CW, 10 % duty cycle						
P_{sat}	Saturated power		-	9.5	-	W
Φ	AM/PM (Phase deviation from rated power to saturated power. Maximum value measured across the 3300–3670 MHz bandwidth.)		-	-13	-	°
ΔG	Gain variation @ Avg. power over temperature	-40 °C to +85 °C	-	0.029	-	dB/°C
ΔP_{sat}	Output power variation @ saturated power over temperature	-40 °C to +85 °C	-	0.002	-	dB/°C
Single-carrier W-CDMA, unclipped						
G_F	Gain flatness	370 MHz bandwidth @ P_{out} = 28 dBm Avg.	-	0.7	-	dB
2-tone CW						
VBW_{res}	VBW resonance[2]		-	300	-	MHz

[1] All data measured with device soldered to NXP reference circuit.
[2] IMD third order inflection point.

Correct biasing sequence for GaN depletion mode transistors

Turning the device ON

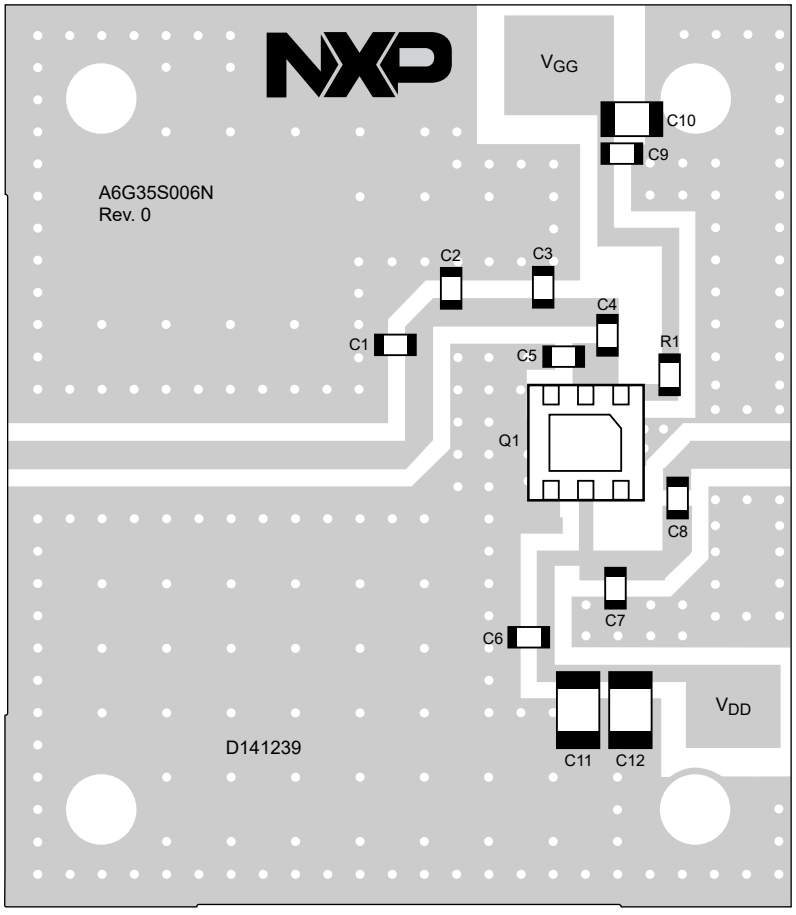
1. Set V_{GS} to the pinch-off voltage, typically -5 V.
2. Turn on V_{DS} to nominal supply voltage (+48 V).
3. Increase V_{GS} until I_{DS} current is attained.
4. Apply RF input power to desired level.

Turning the device OFF

1. Turn RF power off.
2. Reduce V_{GS} down to the pinch-off voltage, typically -5 V.
3. Adjust drain voltage V_{DS} to 0 V. Allow adequate time for drain voltage to reduce to 0 V from external drain capacitors.
4. Turn off V_{GS}.

13 Component layout and parts list

13.1 Component layout



Note: All data measured with device soldered to NXP reference circuit.

aaa-058530

Figure 3. A6G35S006N reference circuit component layout

13.2 Component designations and values

Table 16. A6G35S006N reference circuit component designations and values

Part	Description	Part Number	Manufacturer
C1, C3	0.5 pF chip capacitor	600S0R5AW250XT	ATC
C2	0.3 pF chip capacitor	600S0R3AW250XT	ATC
C4, C8	4.3 pF chip capacitor	600S4R3AW250XT	ATC
C5	1.5 pF chip capacitor	600S1R2AW250XT	ATC
C6, C9	6.2 pF chip capacitor	600S6R2AW250XT	ATC
C7	0.6 pF chip capacitor	600S0R6AW250XT	ATC
C10	2.2 µF chip capacitor	C3216X7S2A225M	TDK
C11, C12	10 µF chip capacitor	GRM32EC72A106KE05L	Murata
Q1	RF power GaN transistor	A6G35S006N	NXP
R1	10 Ω, 1/8 W chip resistor	RC0603FR-0710RL	Yageo
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D141239	MTL

14 Package information

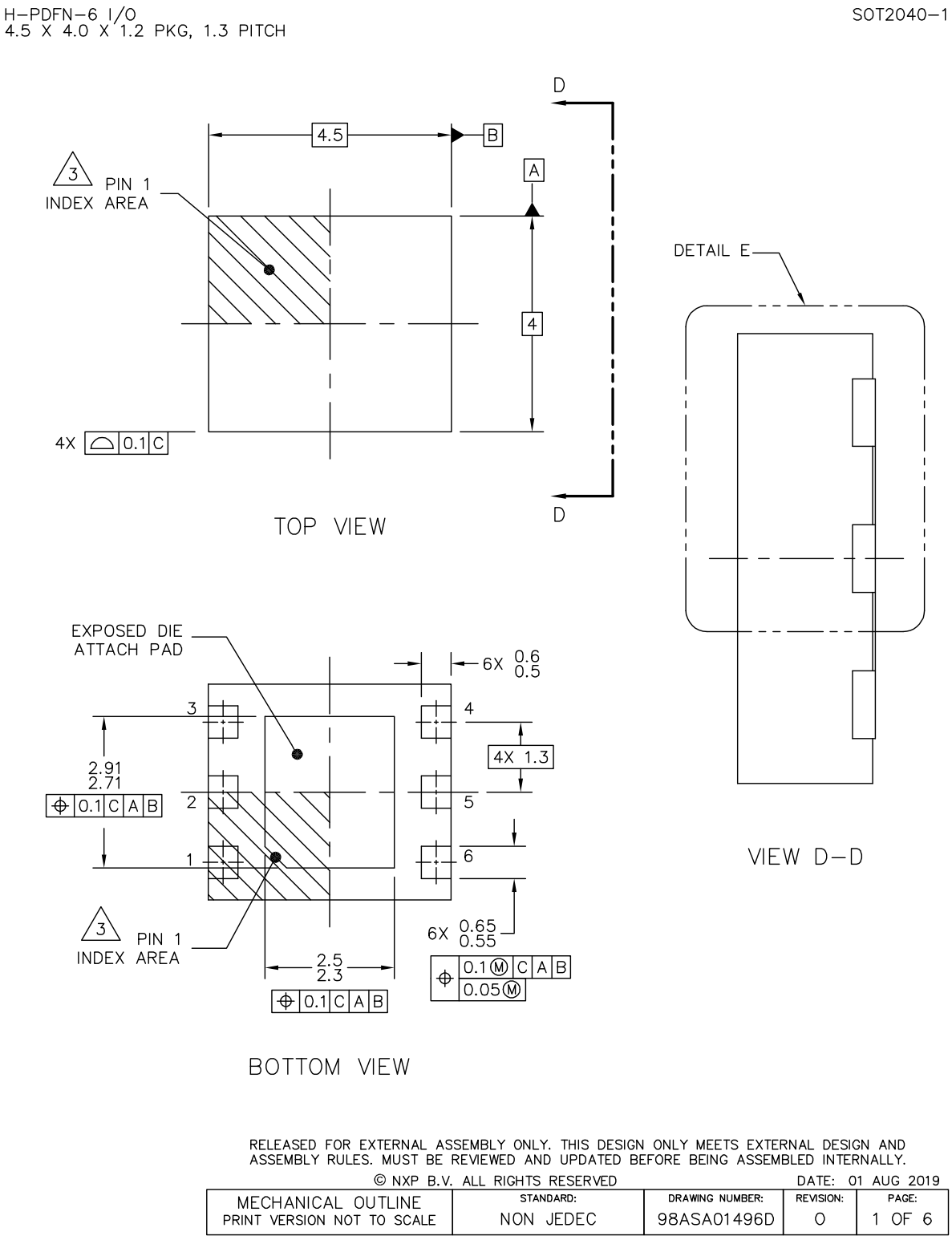


Figure 4. Package outline (DFN 4.5 mm × 4 mm) — top view, bottom view, detail E

H–PDFN–6 I/O
4.5 X 4.0 X 1.2 PKG, 1.3 PITCH

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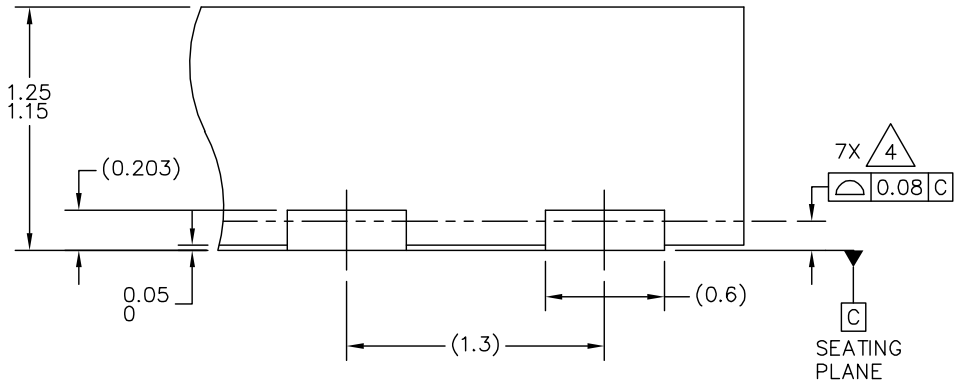

DETAIL E
VIEW ROTATED 90°CW

RELEASED FOR EXTERNAL ASSEMBLY ONLY. THIS DESIGN ONLY MEETS EXTERNAL DESIGN AND ASSEMBLY RULES. MUST BE REVIEWED AND UPDATED BEFORE BEING ASSEMBLED INTERNALLY.

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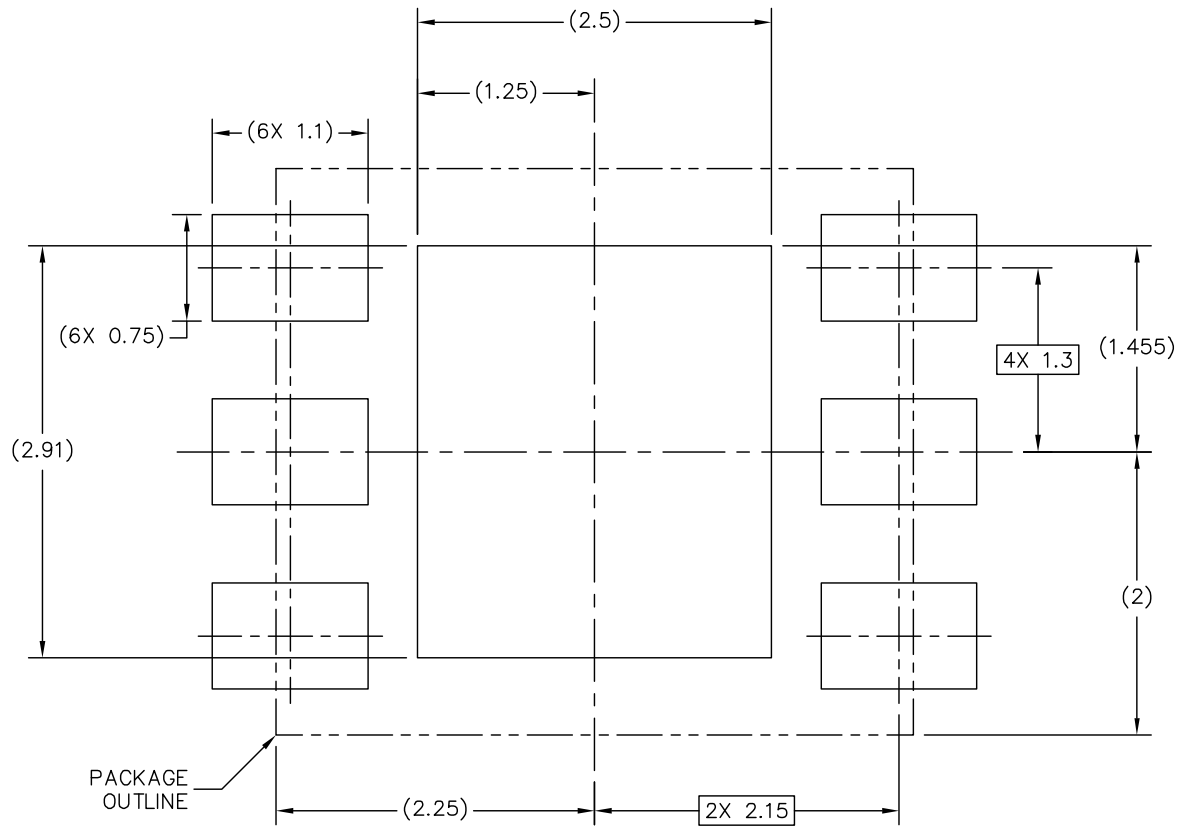
Figure 5. Package outline (DFN 4.5 mm × 4 mm) — detail E, rotated

H–PDFN–6 I/O
4.5 X 4.0 X 1.2 PKG, 1.3 PITCH

SOT2040–1



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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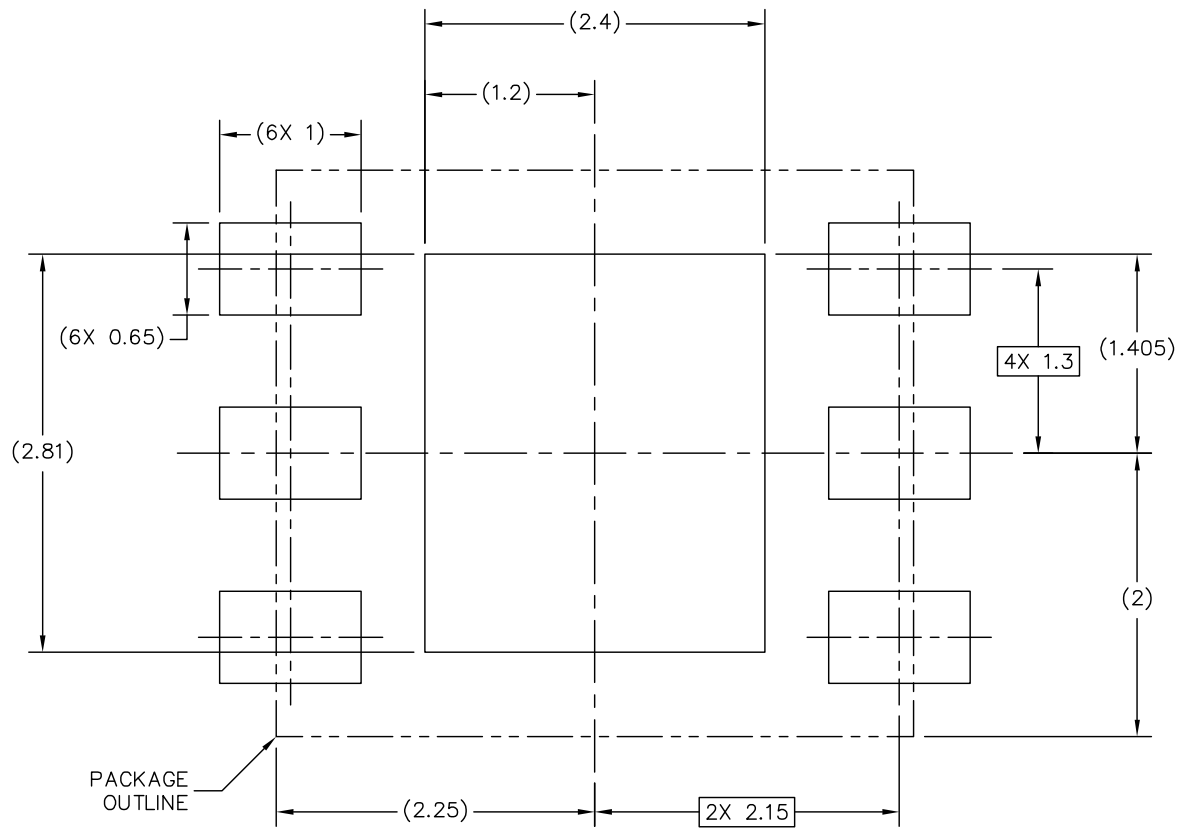
Figure 6. Package outline (DFN 4.5 mm × 4 mm) — PCB design guidelines: solder mask opening pattern



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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Figure 7. Package outline (DFN 4.5 mm × 4 mm) — PCB design guidelines: I/O pads and solderable area

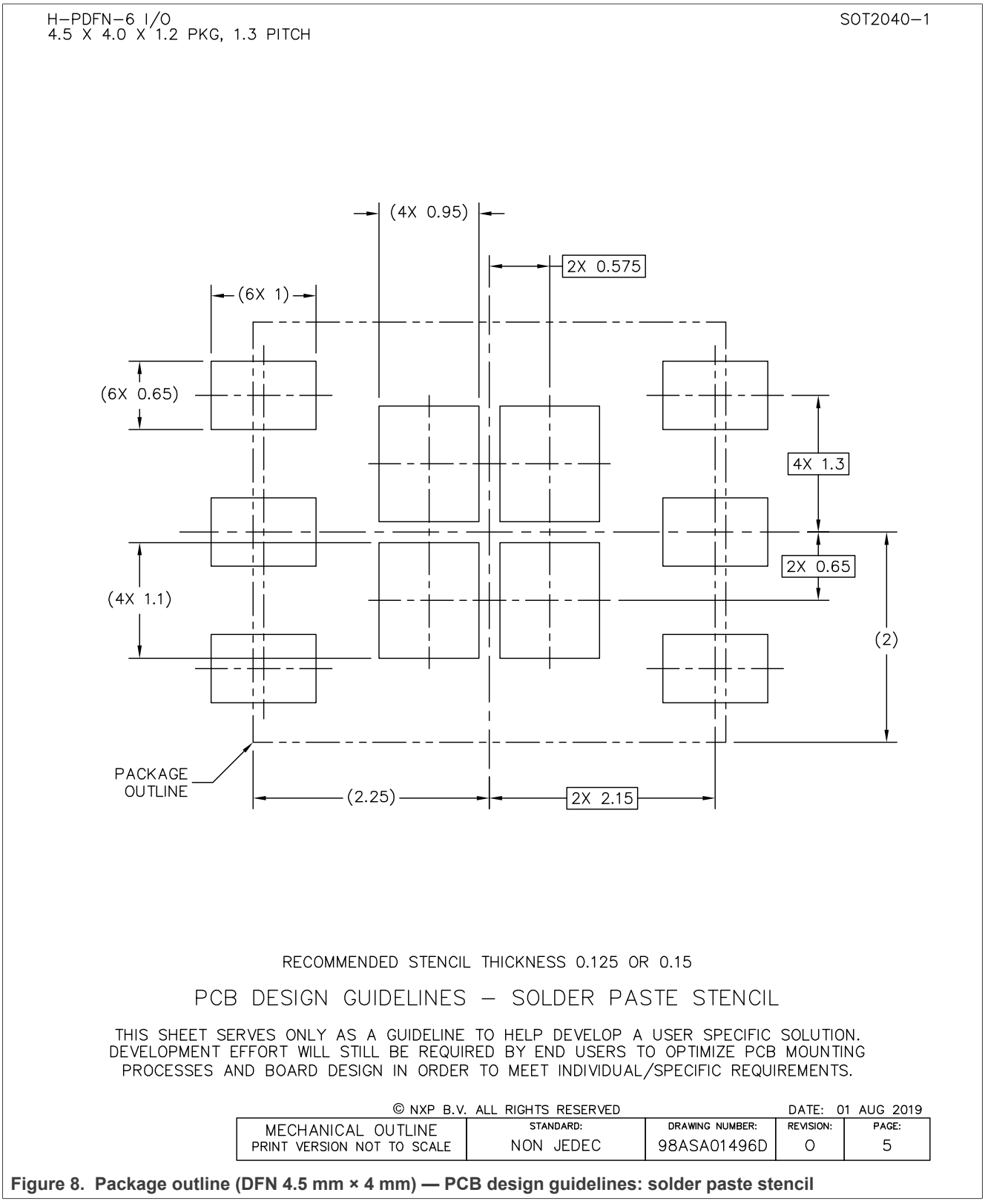

Figure 8. Package outline (DFN 4.5 mm × 4 mm) — PCB design guidelines: solder paste stencil

H–PDFN–6 I/O
4.5 X 4.0 X 1.2 PKG, 1.3 PITCH

SOT2040–1

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.

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Figure 9. Package outline (DFN 4.5 mm × 4 mm) — notes

15 Product documentation, software and tools

Refer to the following resources to aid your design process.

Application notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Software

- .s2p file

Development tools

- Printed circuit boards

16 Revision history

The following table summarizes revisions to this document.

Table 17. Revision history

Document ID	Release date	Description
A6G35S006N Rev. 2	13 January 2025	• Updated frequency band of operation for this device to 2496–5000 MHz, p. 1 • Added Table 3, 4900 MHz performance, p. 2
A6G35S006N Rev. 1	23 December 2024	• Initial release of product data sheet

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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