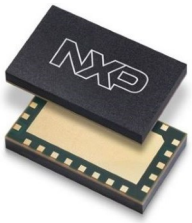
A5M37TG240

Airfast Power Amplifier Module

Rev. 2 — 1 April 2025 Product data sheet



1 General description

The A5M37TG240 is a fully integrated Doherty power amplifier module designed for wireless infrastructure applications that demand high performance in the smallest footprint. Ideal for applications in massive MIMO systems, outdoor small cells and low power remote radio heads. The field-proven LDMOS and GaN power amplifiers are designed for TDD LTE and 5G systems.

2 Features and benefits

- 2-stage module solution that includes an LDMOS integrated circuit as a driver and a GaN final stage amplifier
- Advanced high performance in-package Doherty
- Fully matched (50 ohm input/output, DC blocked)
- Designed for low complexity digital linearization systems
- Reduced memory effects for improved linearized error vector magnitude
- Supports up to 530 MHz instantaneous signal bandwidth

3 Typical performance

Table 1. 3400–4000 MHz — Typical LTE performance

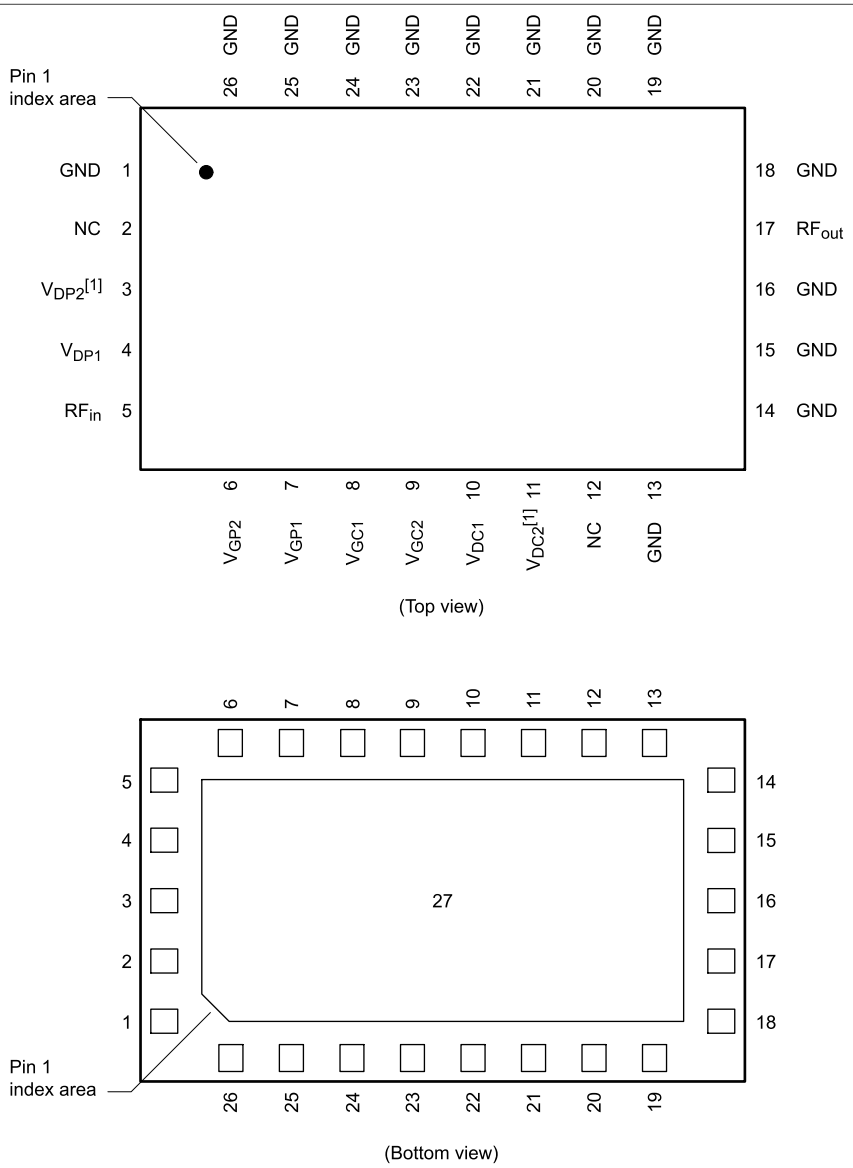
P_{out} = 9 W Avg., V_{DC1} = V_{DP1} = 5 Vdc, V_{DC2} = V_{DP2} = 48 Vdc, 1 × 20 MHz LTE, input signal PAR = 8 dB @ 0.01% probability on CCDF.[1]

Carrier center frequency	Gain (dB)	ACPR (dBc)	PAE (%)
3410 MHz	32.6	–26.9	44.0
3500 MHz	33.0	–26.2	45.5
3600 MHz	33.0	–26.8	46.8
3700 MHz	32.9	–29.1	47.0
3800 MHz	33.0	–32.6	46.8
3900 MHz	32.7	–36.1	46.1
3970 MHz	32.2	–36.1	45.9
3990 MHz	32.1	–35.9	45.8

[1] All data measured with device soldered to NXP reference circuit.

4 Pinning information

4.1 Pinning



Note: Exposed backside of the package is DC and RF ground.

[1] V_{DP2} and V_{DC2} are DC coupled internal to the package and must be powered by a single DC power supply.

Figure 1. Pin configuration

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

4.2 Pin description

Table 2. Pin description

Pin number	Pin function	Pin description
1, 13, 14, 15, 16, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27	GND	Ground
2, 12	NC	No connection
3	V_{DP2}	Peaking drain supply, stage 2
4	V_{DP1}	Peaking drain supply, stage 1
5	RF_{in}	RF input
6	V_{GP2}	Peaking gate supply, stage 2
7	V_{GP1}	Peaking gate supply, stage 1
8	V_{GC1}	Carrier gate supply, stage 1
9	V_{GC2}	Carrier gate supply, stage 2
10	V_{DC1}	Carrier drain supply, stage 1
11	V_{DC2}	Carrier drain supply, stage 2
17	RF_{out}	RF output

5 Functional electrical routing diagram

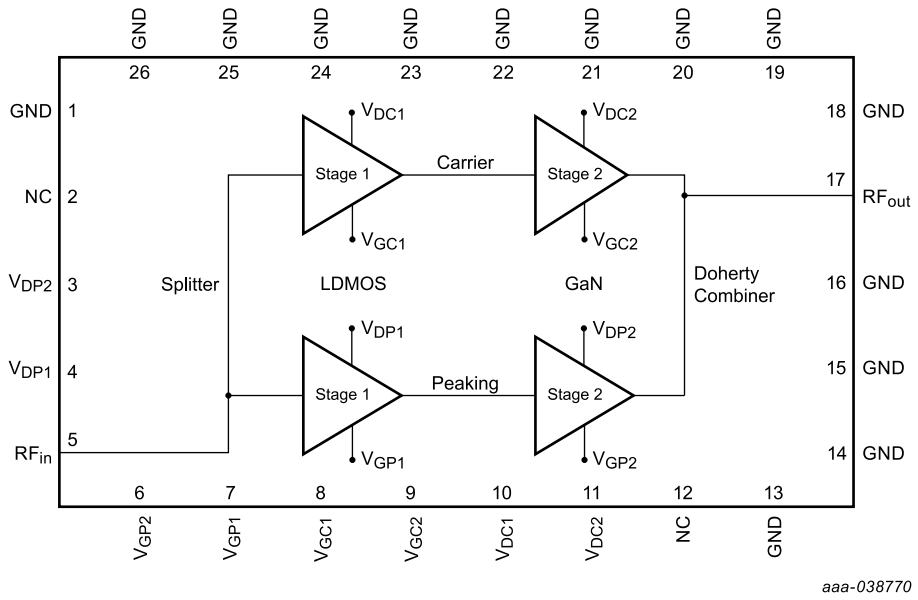


Figure 2. Functional electrical routing diagram

6 Ordering information

Table 3. Ordering information

Device	Tape and reel information	Package
A5M37TG240T2	T2 suffix = 2,000 units, 24 mm tape width, 13-inch reel	10 mm × 6 mm Module

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

7 Product marking

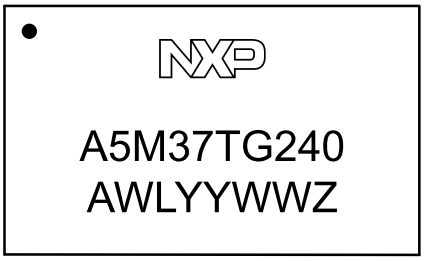


Figure 3. Product marking

Table 4. Product marking trace code

Identifier	Description
A	Assembly location
WL	Wafer lot indicator
YYWW	Date code
Z	Assembly lot

8 Limiting values

Table 5. Limiting values

Rating	Symbol	Value	Unit
Gate-bias voltage range	V_{G1} V_{G2}	–0.5 to +10 –8, 0	Vdc
Operating voltage range	V_{DD1} V_{DD2}	4.75 to 5.25 +38 to +55	Vdc
Maximum forward gate current, $I_{G\ (A+B)}$, @ T_C = 25°C	I_{GMAX}	8.7	mA
Storage temperature range	T_{stg}	–65 to +150	°C
Case operating temperature	T_C	125	°C
Maximum channel temperature	T_{CH}	225	°C
Peak input power (3700 MHz, pulsed CW, 10 µsec(on), 10% duty cycle, V_{DC1} = V_{DP1} = 5 Vdc, V_{DC2} = V_{DP2} = 48 Vdc)	P_{in}	28	dBm

9 Lifetime

Table 6. Lifetime

Characteristic	Symbol	Value	Unit
Mean time to failure (Case temperature 125°C, 75% duty cycle, 9 W Avg., V_{DC1} = V_{DP1} = 5 Vdc, V_{DC2} = V_{DP2} = 48 Vdc)	MTTF	> 10	Years

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

10 Thermal characteristics

Table 7. Thermal characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance by infrared measurement, active die surface-to-case (Case temperature 125°C, P_D = 13.0 W)	$R_{\theta SC}$ (IR)	5.7[1]	°C/W
Thermal resistance by finite element analysis, channel-to-case (Case temperature 125°C, P_D = 9.1 W) (Case temperature 110°C, P_D = 11.9 W)	$R_{\theta CHC}$ (FEA)	11.0[2] 9.7[2]	°C/W

[1] Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to http://www.nxp.com/RF and search for AN1955.

[2] $R_{\theta CHC}$ (FEA) must be used for purposes related to reliability and limitations on maximum channel temperature. MTTF may be estimated by the expression MTTF (hours) = $10^{[A + B/(T + 273)]}$, where T is the channel temperature in degrees Celsius, A = –12.47 and B = 9729.

11 ESD protection characteristics

Table 8. ESD protection characteristics

Test methodology	Class
Human Body Model (per JS-001-2023)	2
Charge Device Model (per JS-002-2022)	C3

12 Moisture sensitivity level

Table 9. Moisture sensitivity level

Test methodology	Rating	Package peak temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

13 Electrical characteristics

13.1 DC characteristics — off characteristics

Table 10. DC characteristics — off characteristics

(T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Carrier + peaking stage 2, GaN — off characteristics					
Off-state drain leakage[1] (V_{DS} = 150 Vdc, V_{GS} = –8 Vdc)	$I_{D(BR)}$	—	—	4.0	mAdc
Off-state gate leakage (V_{DS} = 48 Vdc, V_{GS} = –7 Vdc)	I_{GLK}	–4.0	—	—	mAdc

[1] Carrier side and peaking side are tied together for these measurements.

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

13.2 DC characteristics — on characteristics

Table 11. DC characteristics — on characteristics

(T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Typ	Range	Unit
Carrier stage 1, LDMOS — on characteristics				
Gate threshold voltage (V_{DS} = 5 Vdc, I_{DC1} = 120 µAdc)	$V_{GS(th)}$	1.4	±0.4	Vdc
Gate quiescent voltage (V_{DS} = 5 Vdc, I_{DQC1} = 90 mAdc, measured in functional test)	$V_{GS(Q)}$	2.0	±0.4	Vdc
Carrier stage 2, GaN — on characteristics				
Gate threshold voltage[1] (V_{DS} = 10 Vdc, I_D = 8.7 mAdc)	$V_{GS(th)}$	–2.6	±1.0	Vdc
Gate quiescent voltage (V_{DS} = 48 Vdc, I_{DQC2} = 58 mAdc, measured in functional test)	$V_{GS(Q)}$	–2.8	±1.0	Vdc
Peaking stage 1, LDMOS — on characteristics				
Gate threshold voltage (V_{DS} = 5 Vdc, I_{DP1} = 120 µAdc)	$V_{GS(th)}$	1.4	±0.4	Vdc
Gate quiescent voltage (V_{DS} = 5 Vdc, I_{DQP1} = 60 mAdc, measured in functional test)	$V_{GS(Q)}$	2.0	±0.4	Vdc
Peaking stage 2, GaN — on characteristics				
Gate threshold voltage[1] (V_{DS} = 10 Vdc, I_D = 8.7 mAdc)	$V_{GS(th)}$	–2.6	±1.0	Vdc
Gate quiescent voltage (V_{DS} = 48 Vdc, I_{DQP2} = 0 mAdc, measured in functional test)	$V_{GS(Q)}$	–3.9	±1.0	Vdc

[1] Carrier side and peaking side are tied together for these measurements.

13.3 Functional tests

Table 12. Functional tests — 3400 MHz

(In NXP Doherty production ATE[1] test fixture, T_A = 25°C unless otherwise noted, 50 ohm system)[2] V_{DD1} = 5 Vdc, V_{DD2} = 48 Vdc, I_{DQC1} = 90 mA, I_{DQC2} = 58 mA, I_{DQP1} = 60 mA, V_{GP2} = (V_{BIAS} – 1.0)[3] Vdc, P_{out} = 9 W Avg., 1-tone CW, f = 3400 MHz.

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G	29.9	33.2	—	dB
Drain efficiency	η_D	38.0	43.7	—	%
Saturated power[4] (Pulsed CW, 5% duty cycle)	P_{sat}	46.3	47.9	—	dBm

[1] ATE is a socketed test environment.
[2] Part input and output matched to 50 ohms.
[3] Increase V_{GP2} (peaking side) until I_{DQP2} = 20 mA current is attained, and then subtract 0.94 V for final V_{GP2} bias voltage.
[4] P_{sat} is defined at P6dB compression point.

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

13.4 Wideband ruggedness

Table 13. Wideband ruggedness

(In NXP Doherty power amplifier module reference circuit, T_A = 25°C unless otherwise noted, 50 ohm system)[1]
I_{DQC1} = 90 mA, I_{DQC2} = 58 mA, I_{DQP1} = 60 mA, V_{GP2} = (V_{BIAS} – 1.0)[2] *Vdc, f = 3700 MHz, Additive White Gaussian Noise (AWGN) with 10 dB PAR.*

Characteristic	Test results
ISBW of 400 MHz at 55 Vdc, 3 dB input overdrive from 9 W Avg. modulated output power	No device degradation

[1] All data measured with device soldered to NXP reference circuit.
[2] Increase V_{GP2} (peaking side) until I_{DQP2} = 20 mA current is attained, and then subtract 0.94 V for final V_{GP2} bias voltage.

13.5 Typical performance

Table 14. Typical performance

(In NXP Doherty power amplifier module reference circuit, T_A = 25°C unless otherwise noted, 50 ohm system)[1]
V_{DD1} = 5 Vdc, V_{DD2} = 48 Vdc, I_{DQC1} = 90 mA, I_{DQC2} = 58 mA, I_{DQP1} = 60 mA, V_{GP2} = (V_{BIAS} – 1.0)[2] *Vdc, f = 3700 MHz.*

Characteristic	Symbol	Min	Typ	Max	Unit
VBW resonance point, 2-tone, 1 MHz tone spacing (IMD third order intermodulation inflection point)	VBW_{res}	—	300	—	MHz
1-carrier 20 MHz LTE, 8 dB input signal PAR					
Gain	G	—	32.9	—	dB
Power added efficiency	PAE	—	47.0	—	%
Adjacent channel power ratio	ACPR	—	–29.1	—	dBc
Adjacent channel power ratio	ALT1	—	–43.4	—	dBc
Adjacent channel power ratio	ALT2	—	–47.6	—	dBc
Gain flatness[3]	G_F	—	0.9	—	dB
Pulsed CW, 10% duty cycle					
Saturated power[4]	P_{sat}	—	48.0	—	dBm
AM/PM @ saturated power[4]	Φ	—	–27.0	—	°
Gain variation @ Avg. power over temperature (–40°C to +105°C)	ΔG	—	0.062	—	dB/°C
Output power variation @ saturated power over temperature[4] (–40°C to +105°C)	ΔP_{sat}	—	0.004	—	dB/°C

[1] All data measured with device soldered to NXP reference circuit.
[2] Increase V_{GP2} (peaking side) until I_{DQP2} = 20 mA current is attained, and then subtract 0.94 V for final V_{GP2} bias voltage.
[3] Gain flatness = Max(G(f_{Low} to f_{High})) – Min(G(f_{Low} to f_{High})).
[4] P_{sat} is defined at P6dB compression point.

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

Correct Biasing Sequence

Turn ON:

Bias ON the GaN final stage first

1. Set gate voltage V_{GC2} and V_{GP2} to –5 V.
2. Set drain voltage V_{DC2} and V_{DP2} to nominal supply voltage (+48 V).
3. Increase V_{GP2} (peaking side) until I_{DQP2} = 20 mA current is attained, and then subtract 0.94 V for final V_{GP2} bias voltage.
4. Increase V_{GC2} (carrier side) until I_{DQC2} current is attained.

Bias ON the LDMOS driver stage second

5. Set drain voltage V_{DC1} and V_{DP1} to nominal supply voltage (+5 V).
6. Increase V_{GC1} (carrier side) until I_{DQC1} current is attained.
7. Increase V_{GP1} (peaking side) until I_{DQP1} current is attained.
8. Apply RF input power to desired level.

Turn OFF:

Bias OFF the GaN final stage first

1. Disable RF input power.
2. Adjust gate voltage V_{GC2} and V_{GP2} to –5 V.
3. Adjust drain voltage V_{DC2} and V_{DP2} to 0 V. Allow adequate time for drain voltage to reduce to 0 V from external drain capacitors.
4. Disable V_{GC2} and V_{GP2}.

Bias OFF the LDMOS driver stage second

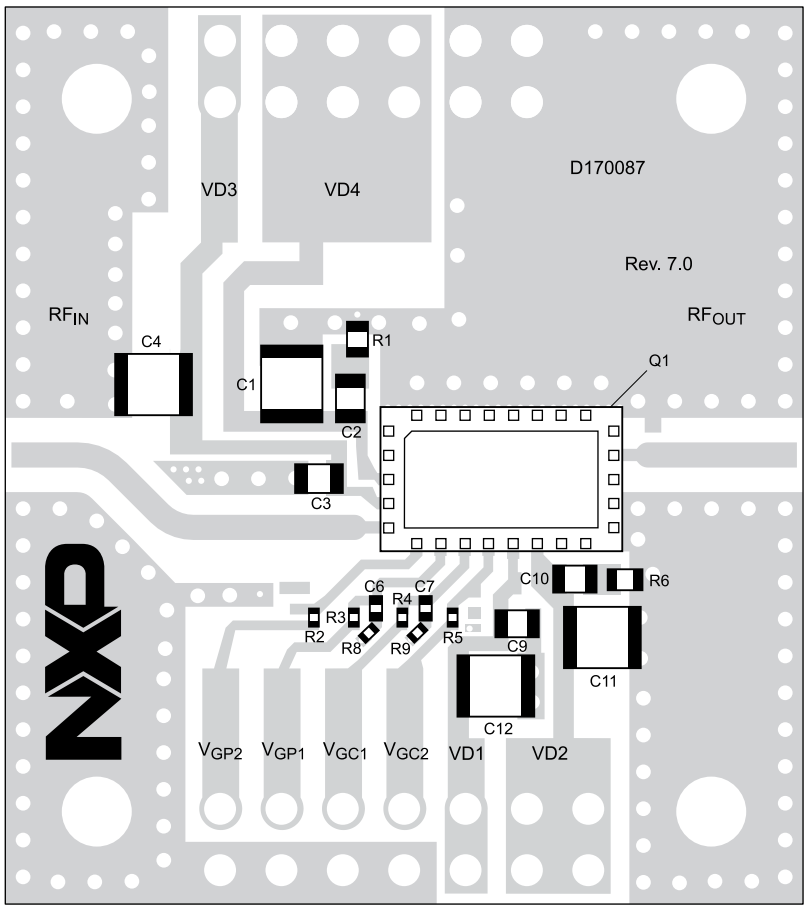
5. Adjust gate voltage V_{GC1} and V_{GP1} to 0 V.
6. Adjust drain voltage V_{DC1} and V_{DP1} to 0 V.

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

14 Component layout and parts list

14.1 Component layout



Board label	Pin description	Pin function
VD1	Carrier drain supply, stage 1	V_{DC1}
VD2	Carrier drain supply, stage 2	V_{DC2}
VD3	Peaking drain supply, stage 1	V_{DP1}
VD4	Peaking drain supply, stage 2	V_{DP2}

Figure 4. A5M37TG240 reference circuit component layout

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

14.2 Component designations and values

Table 15. A5M37TG240 reference circuit component designations and values

Part	Description	Part number	Manufacturer
C1, C4, C11, C12	10 µF chip capacitor	GRM32EC72A106KE05L	Murata
C2, C3, C9, C10	1 µF chip capacitor	GRM21BC72A105KE01L	Murata
C6, C7	1000 pF chip capacitor	GRM155R72A102KA01D	Murata
Q1	Power amplifier module	A5M37TG240	NXP
R1, R6	0 Ω, 0.063 W chip resistor	6-1622826-4	TE Connectivity
R2, R5, R8, R9	0 Ω, 1/20 W chip resistor	RC0201JR-070RL	Yageo
R3, R4	10 Ω, 1/20 W chip resistor	RC0201FR-0710RL	Yageo
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D170087	MTL

Note: Component numbers C5, C8 and R7 are intentionally omitted.

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

15 Package information

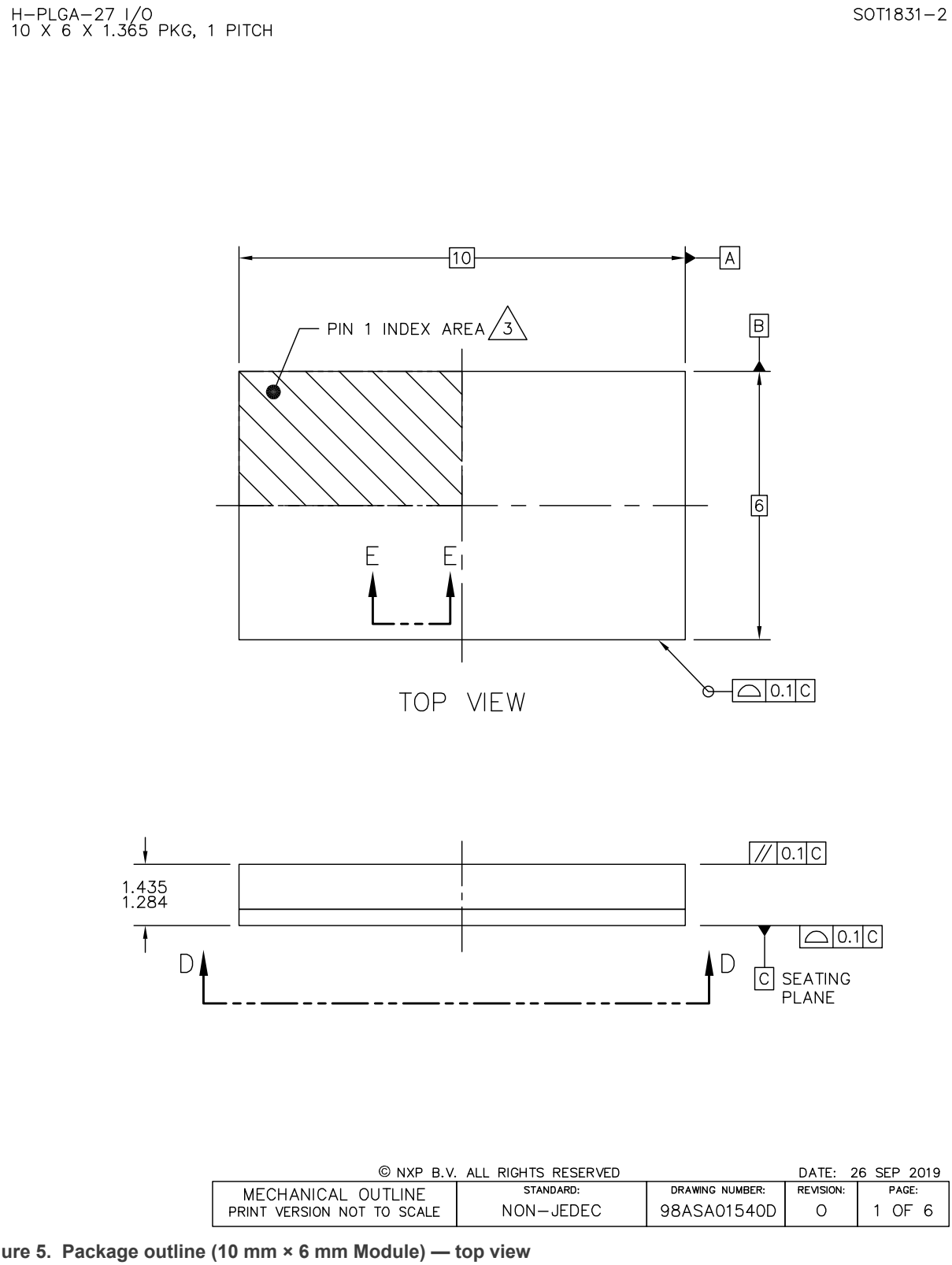


Figure 5. Package outline (10 mm × 6 mm Module) — top view

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

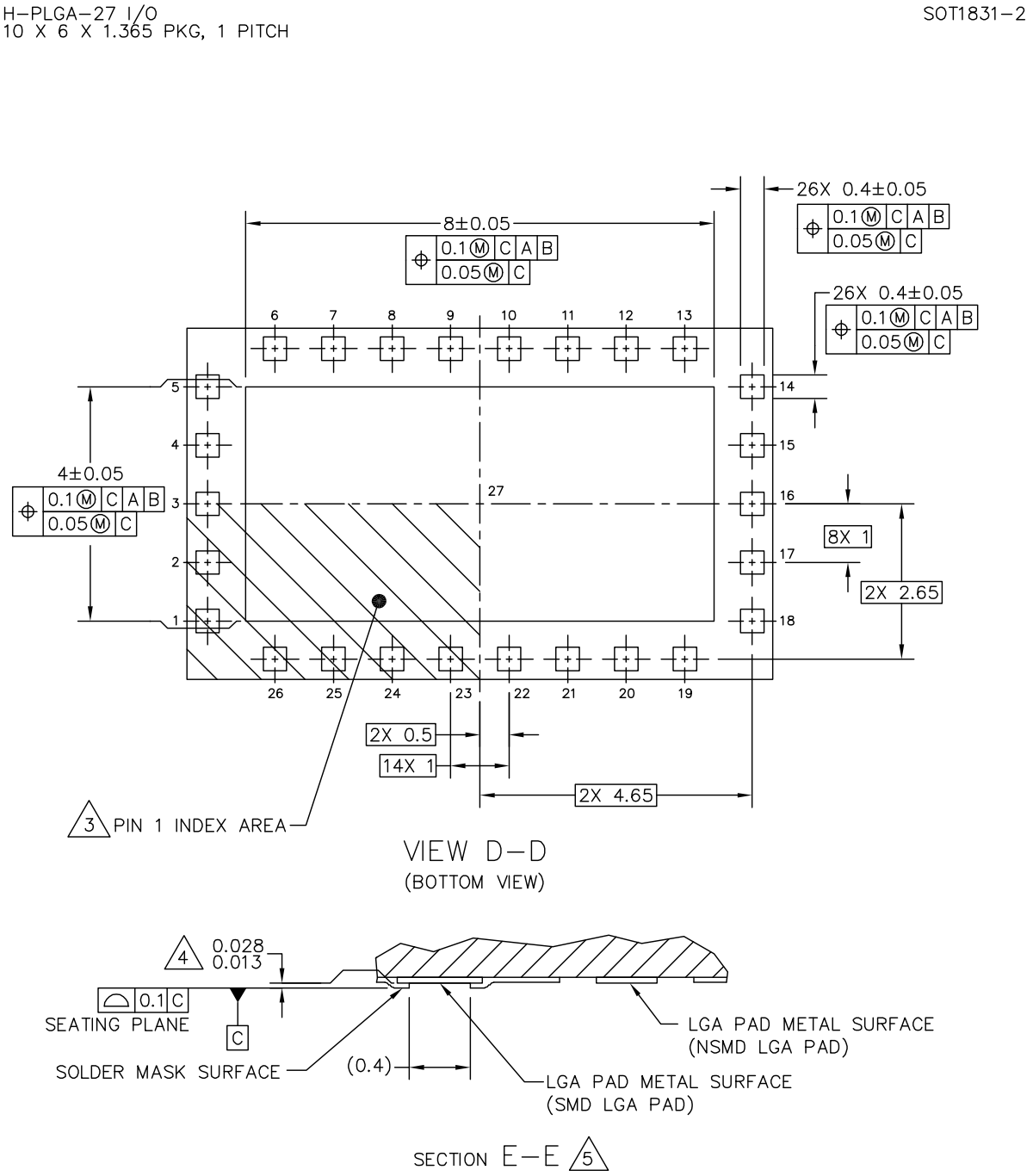
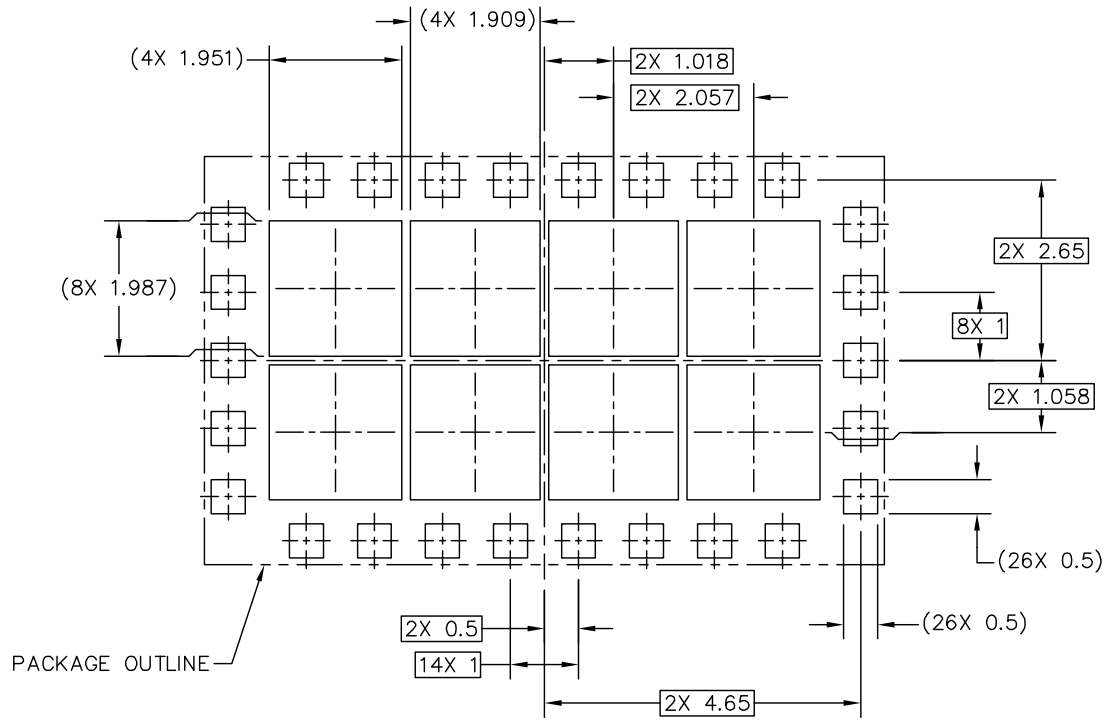


Figure 6. Package outline (10 mm × 6 mm Module) — bottom view

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 26 SEP 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON–JEDEC	DRAWING NUMBER: 98ASA01540D	REVISION: O	PAGE: 3

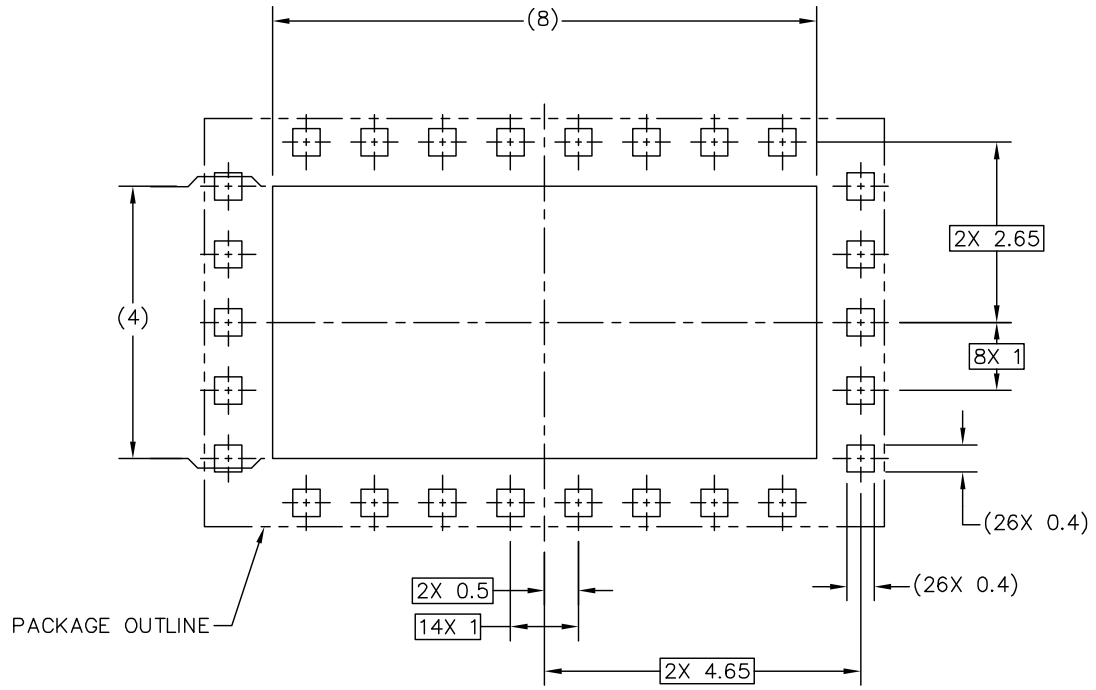
Figure 7. Package outline (10 mm × 6 mm Module) — PCB design guidelines: solder mask opening pattern

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

H–PLGA–27 I/O
10 X 6 X 1.365 PKG, 1 PITCH

SOT1831–2



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREAS

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 26 SEP 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON–JEDEC	DRAWING NUMBER: 98ASA01540D	REVISION: O	PAGE: 4

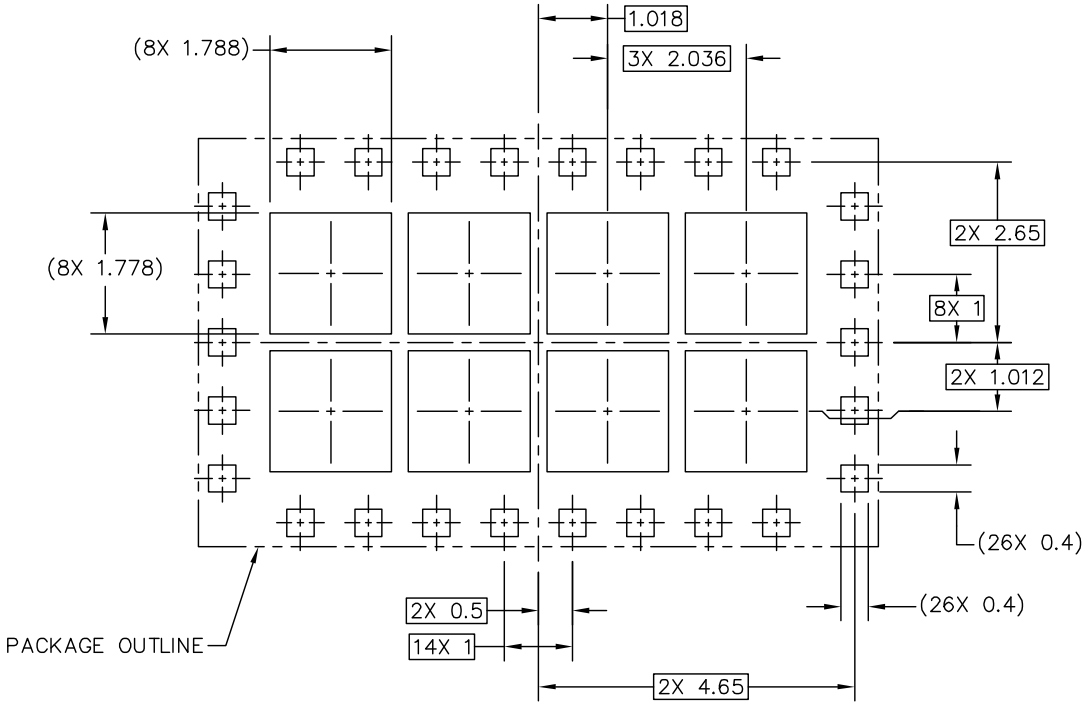
Figure 8. Package outline (10 mm × 6 mm Module) — PCB design guidelines: I/O pads and solderable areas

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

H–PLGA–27 I/O
10 X 6 X 1.365 PKG, 1 PITCH

SOT1831–2



RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 26 SEP 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON–JEDEC	DRAWING NUMBER: 98ASA01540D	REVISION: O	PAGE: 5

Figure 9. Package outline (10 mm × 6 mm Module) — PCB design guidelines: solder paste stencil

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

H–PLGA–27 I/O
10 X 6 X 1.365 PKG, 1 PITCH

SOT1831–2

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. DIMENSION APPLIES TO ALL LEADS AND FLAG.
5. THE BOTTOM VIEW SHOWS THE SOLDERABLE AREA OF THE PADS. THE CENTER PAD (PIN 27) IS SOLDER MASK DEFINED. SOME PERIPHERAL PADS ARE SOLDER MASK DEFINED (SMD) AND OTHERS ARE NON–SOLDERMASK DEFINED (NSMD).

© NXP B.V. ALL RIGHTS RESERVED

DATE: 26 SEP 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON–JEDEC	DRAWING NUMBER: 98ASA01540D	REVISION: O	PAGE: 6

Figure 10. Package outline (10 mm × 6 mm Module) — notes

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

16 Product documentation and tools

Refer to the following resources to aid your design process.

Application notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Development tools

- Printed circuit boards

17 Failure analysis

At this time, because of the physical characteristics of the part, failure analysis is limited to electrical signature analysis. In cases where NXP is contractually obligated to perform failure analysis (FA) services, full FA may be performed by third party vendors with moderate success. For updates contact your local NXP Sales Office.

18 Revision history

The following table summarizes revisions to this document.

Table 16. Revision history

Document ID	Release date	Description
A5M37TG240 Rev. 2	1 April 2025	• Biasing sequence note and corresponding footnotes: updated to reflect latest biasing sequence recommendations, pp. 6–8
A5M37TG240 Rev. 1	19 March 2024	• Initial release of product data sheet

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Airfast — is a trademark of NXP B.V.

All information provided in this document is subject to legal disclaimers.

© 2025 NXP B.V. All rights reserved.

Contents

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© 2025 NXP B.V. **All rights reserved.**