A5G08H800W19N

Airfast RF Power GaN Transistor

Rev. 1 — 21 December 2023 Product data sheet

This 112 W asymmetrical Doherty RF power GaN transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 865 to 960 MHz.

This part is characterized and performance is guaranteed for applications operating in the 865 to 960 MHz band. There is no guarantee of performance when this part is used in applications designed outside of these frequencies.

900 MHz

- Typical Doherty Single–Carrier W–CDMA Production Test Fixture Performance: V_{DD} = 50 Vdc, I_{DQA} = 350 mA, V_{GSB} = –5 Vdc, P_{out} = 112 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. (1)

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
865 MHz	19.3	60.5	8.8	–28.0
913 MHz	19.5	59.9	8.6	–28.8
960 MHz	19.1	58.7	8.3	–30.5

1. All data measured with device soldered to NXP production test fixture.

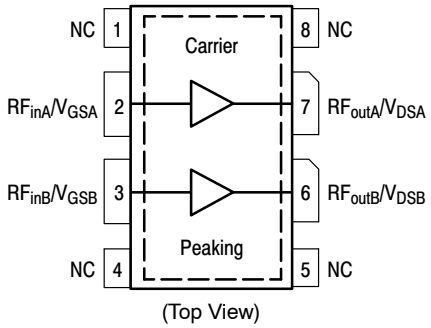
Features

- High terminal impedances for optimal broadband performance
- Advanced high performance in–package Doherty
- Improved linearized error vector magnitude with next generation signal
- Able to withstand extremely high output VSWR and broadband operating conditions
- Plastic package

A5G08H800W19N

865–960 MHz, 112 W Avg., 50 V AIRFAST RF POWER GaN TRANSISTOR

OM–780–4S4S PLASTIC



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain−Source Voltage	V_{DSS}	125	Vdc
Gate−Source Voltage	V_{GS}	−16, 0	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum Forward Gate Current, $I_{G\ (A+B)}$, @ T_C = 25°C	I_{GMAX}	95	mA
Storage Temperature Range	T_{stg}	−65 to +150	°C
Case Operating Temperature Range	T_C	−55 to +150	°C
Maximum Channel Temperature	T_{CH}	225	°C

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Value	Unit
Operating Voltage	V_{DD}	50	Vdc

Table 3. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance by Infrared Measurement, Active Die Surface−to−Case Case Temperature 83°C, P_D = 104 W	$R_{\theta SC}$ (IR)	0.37 (1)	°C/W
Thermal Resistance by Finite Element Analysis, Channel−to−Case Case Temperature 83°C, P_D = 103.5 W	$R_{\theta CHC}$ (FEA)	0.6 (2)	°C/W

Table 4. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JS−001−2017)	1A
Charge Device Model (per JS−002−2014)	C3

Table 5. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22−A113, IPC/JEDEC J−STD−020	3	245	°C

Table 6. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Off Characteristics (3)						
Off−State Drain Leakage		$I_{D(BR)}$				mAdc
(V_{DS} = 150 Vdc, V_{GS} = −8 Vdc)	Carrier		—	—	15.4	
(V_{DS} = 150 Vdc, V_{GS} = −8 Vdc)	Peaking		—	—	26.4	
On Characteristics — Side A, Carrier						
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 35 mAdc)		$V_{GS(th)}$	−4.6	−2.6	−1.9	Vdc
Gate Quiescent Voltage (V_{DD} = 50 Vdc, I_D = 350 mAdc, Measured in Functional Test)		$V_{GSA(Q)}$	−3.1	−2.6	−2.1	Vdc
On Characteristics — Side B, Peaking						
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 60 mAdc)		$V_{GS(th)}$	−4.6	−2.6	−1.9	Vdc

1. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.
2. $R_{\theta CHC}$ (FEA) must be used for purposes related to reliability and limitations on maximum channel temperature. MTTF may be estimated by the expression MTTF (hours) = $10^{[A + B/(T + 273)]}$, where T is the channel temperature in degrees Celsius, A = −11.6 and B = 9129.
3. Each side of device measured separately.

(continued)

Table 6. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1) (In NXP Doherty Production Test Fixture, 50 ohm system) V_{DD} = 50 Vdc, I_{DQA} = 350 mA, V_{GSB} = (V_t – 2.325) Vdc, P_{out} = 158 W Avg., f = 913 MHz, Single–Carrier W–CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	17.1	18.2	19.7	dB
Drain Efficiency	η_D	54.5	59.7	—	%
Saturated Power (Pulsed CW, 5% Duty Cycle)	P_{sat}	58.0	58.5	—	dBm
Adjacent Channel Power Ratio	ACPR	—	–30.2	–25.7	dBc
Wideband Ruggedness (In NXP Doherty Production Test Fixture, 50 ohm system) I_{DQA} = 350 mA, V_{GSB} = –5 Vdc, f = 913 MHz, Additive White Gaussian Noise (AWGN) with 10 dB PAR					
ISBW of 400 MHz at 55 Vdc, 159 W Avg. Modulated Output Power (3 dB Input Overdrive from 79 W Avg. Modulated Output Power)	No Device Degradation				
Typical Performance (In NXP Doherty Production Test Fixture, 50 ohm system) V_{DD} = 50 Vdc, I_{DQA} = 350 mA, V_{GSB} = –5 Vdc, 865–960 MHz Bandwidth					
Pulsed CW, 10% Duty Cycle					
Saturated Power (2)	P_{sat}	—	912	—	W
AM/PM (2) (Maximum value measured at saturated power across the 865–960 MHz bandwidth)	Φ	—	–20	—	°
Gain Variation @ Avg. Power over Temperature (–40°C to +85°C)	ΔG	—	0.007	—	dB/°C
Output Power Variation @ Saturated Power over Temperature (–40°C to +85°C)	ΔP_{sat}	—	0.003	—	dB/°C
Single–Carrier W–CDMA, Unclipped					
Gain Flatness in 95 MHz Bandwidth @ P_{out} = 112 W Avg. (2)	G_F	—	0.4	—	dB
2–Tone CW					
VBW Resonance Point (2) (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	110	—	MHz

Table 7. Ordering Information

Device	Tape and Reel Information	Package
A5G08H800W19NR3	R3 Suffix = 250 Units, 44 mm Tape Width, 13–inch Reel	OM–780–4S4S

1. Internally matched part.
2. All data measured with device soldered to NXP production test fixture.

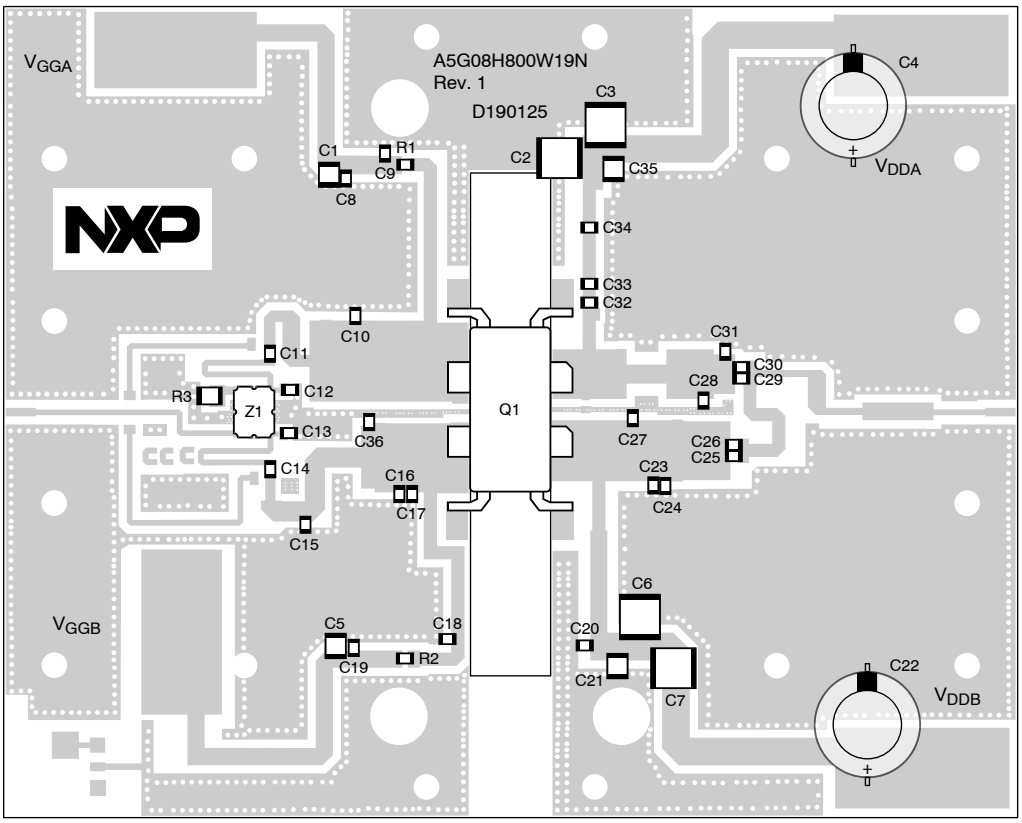
Correct Biasing Sequence for GaN Depletion Mode Transistors in a Doherty Configuration

Bias ON the device

1. Set gate voltage V_{GSA} and V_{GSB} to –5 V.
2. Set drain voltage V_{DSA} and V_{DSB} to nominal supply voltage (+50 V).
3. Increase V_{GSA} (carrier side) until I_{DQA} current is attained.
4. Increase V_{GSB} (peaking side) to target bias voltage.
5. Apply RF input power to desired level.

Bias OFF the device

1. Disable RF input power.
2. Adjust gate voltage V_{GSA} and V_{GSB} to –5 V.
3. Adjust drain voltage V_{DSA} and V_{DSB} to 0 V. Allow adequate time for drain voltage to reduce to 0 V from external drain capacitors.
4. Disable V_{GSA} and V_{GSB}.



Note: All data measured with device soldered to NXP production test fixture.

aaa−052004

Figure 2. A5G08H800W19N Production Test Circuit Component Layout

Table 8. A5G08H800W19N Production Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C5	10 µF Chip Capacitor	GRM32EC72A106KE05L	Murata
C2, C6	4.7 µF Chip Capacitor	C453X752A475M	TDK
C3, C7	10 µF Chip Capacitor	C5750X7S2106M	TDK
C4, C22	220 µF, 100 V Electrolytic Chip Capacitor	EEV−FK2A221M	Panasonic
C8, C9, C11, C14, C18, C19, C20, C25, C26	100 pF Chip Capacitor	800R101KT500XT	ATC
C10, C23	2.0 pF Chip Capacitor	600F2R0BT250XT	ATC
C12, C13, C15	1.2 pF Chip Capacitor	600F1R2BT250XT	ATC
C16	1.0 pF Chip Capacitor	600F1R0BT250XT	ATC
C17	2.2 pF Chip Capacitor	600F2R2BT250XT	ATC
C21, C35	1 µF Chip Capacitor	GRM32CR72A105KA35L	Murata
C24	5.1 pF Chip Capacitor	600F5R1BT250XT	ATC
C27	1.6 pF Chip Capacitor	600F1R6BT250XT	ATC
C28	3.3 pF Chip Capacitor	600F3R3BT250XT	Murata
C29, C30	20 pF Chip Capacitor	600F200JT250XT	ATC
C31	3.9 pF Chip Capacitor	600F3R9BT250XT	ATC
C32, C33, C34	68 pF Chip Capacitor	600F680JT250XT	ATC
C36	0.5 pF Chip Capacitor	600F0R5BT250XT	ATC
R1, R2	8.25 Ω, 1/4 W Chip Resistor	CRCW12068R25FKEA	Vishay
R3	50 Ω, 30 W Termination Resistor	RFP−375375N6Z50−2	Anaren
Q1	RF Power GaN Transistor	A5G08H800W19N	NXP
Z1	800−1000 MHz, 90°, 2 dB Asymmetric Coupler	CMX09Q02	RN2 Technologies
PCB	Rogers RO4360G2, 0.020″, ε_r = 6.15	D190125	MTL

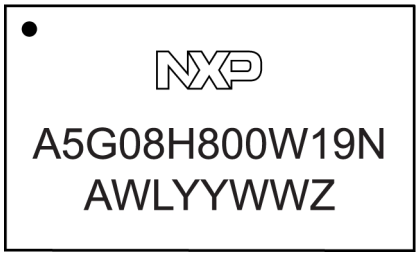


Figure 3. Product Marking

Table 9. Product Marking Trace Code

Identifier	Description
A	Assembly location
WL	Wafer lot indicator
YYWW	Date code
Z	Assembly lot

Package Information

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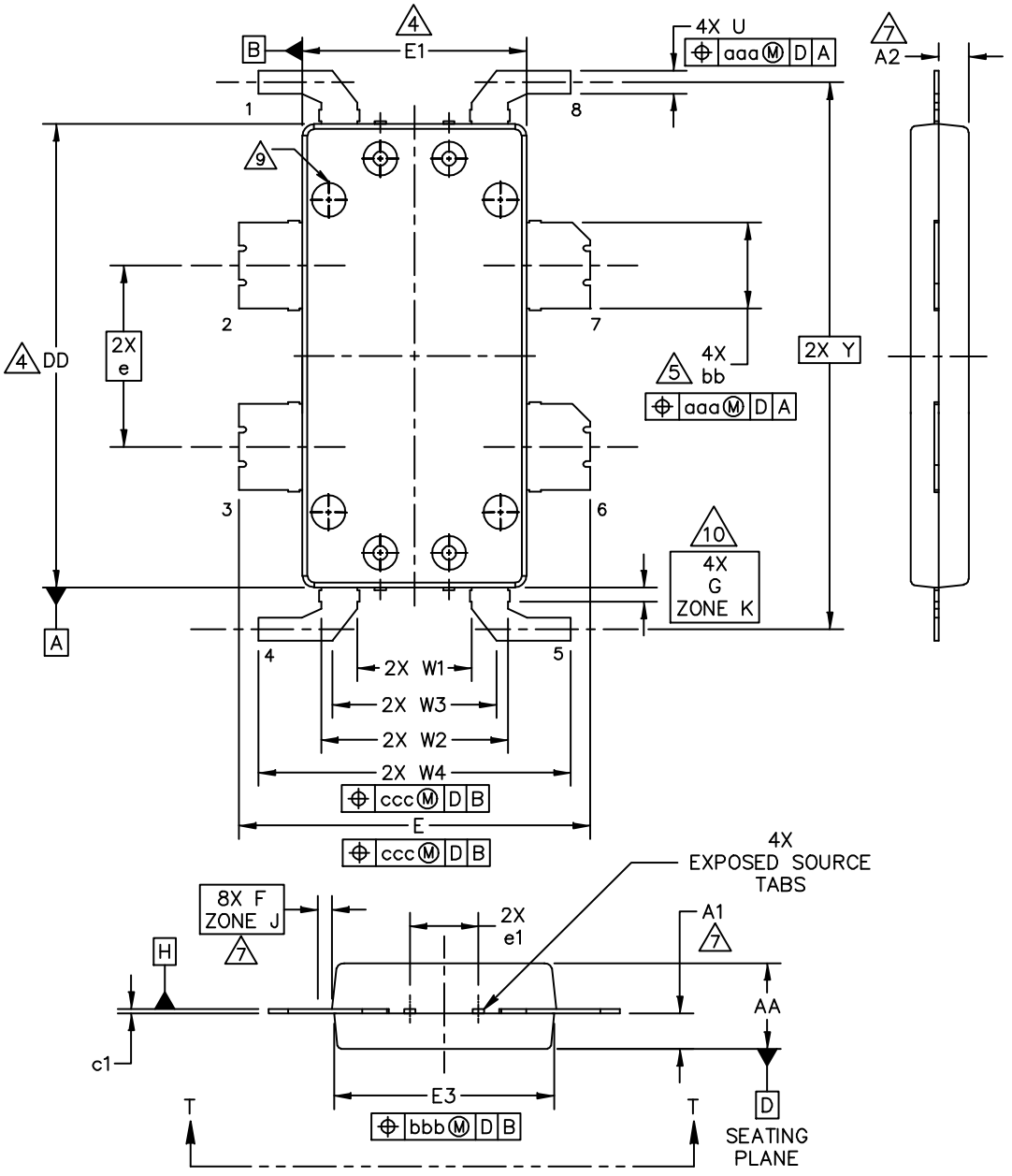

DATE: 29 JUL 2020

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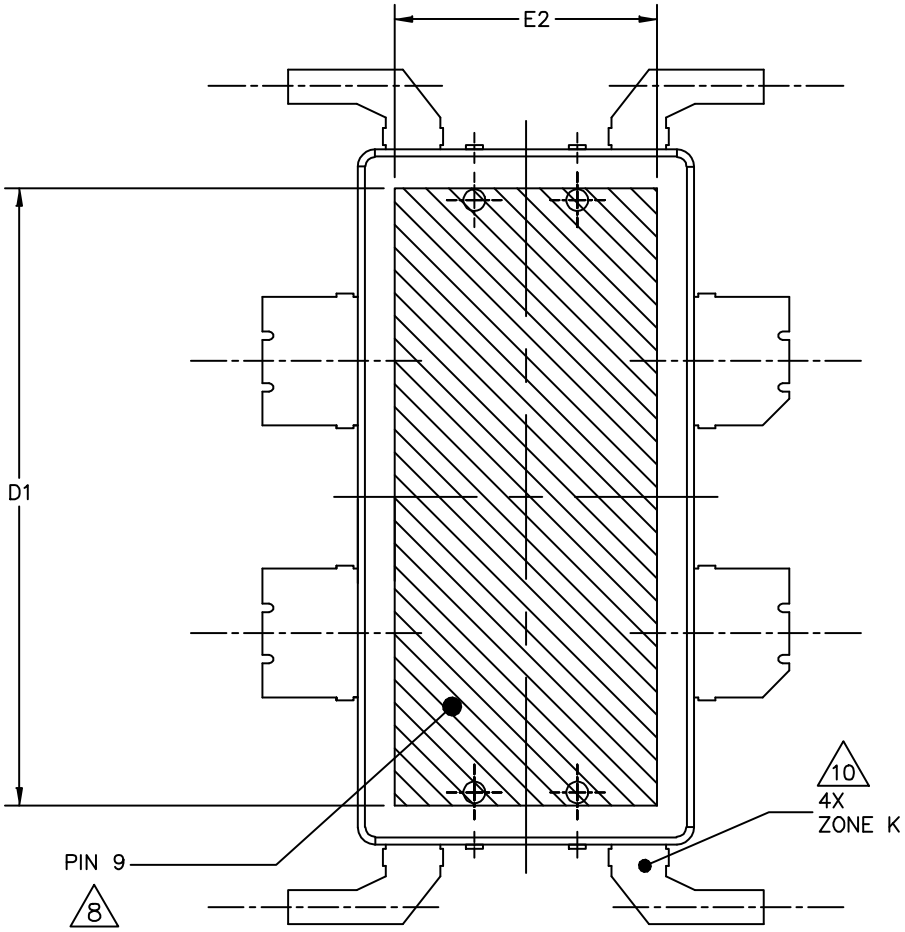

BOTTOM VIEW
VIEW T−T

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OM-780-4S4S SOT2082-1

NOTES:
1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. DATUM PLANE H IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS DD AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS DD AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSION bb DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. DIMENSIONS A1 AND A2 APPLIES WITHIN ZONE J ONLY. A1 APPLIES TO PINS 2, 3, 6 AND 7. A2 APPLIES TO PINS 1, 4, 5 AND 8.

8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.

9. DIMPLED HOLE REPRESENTS INPUT SIDE.

10. ZONE K REPRESENTS NON-SOLDERABLE REGION WHERE MOLD FLASH AND RESIN BLEED ARE PERMITTED ON BOTH SIDES OF THE LEADS.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.148	.152	3.76	3.86	W2	.321	.331	8.15	8.41
A1	.059	.065	1.50	1.65	W3	.281	.291	7.14	7.39
A2	.056	.068	1.42	1.73	W4	.538	.554	13.67	14.07
DD	.808	.812	20.52	20.62	U	.037	.043	0.94	1.09
D1	.720	----	18.29	----	Y	.956 BSC		24.28 BSC	
E	.610	.618	15.49	15.70	bb	.147	.153	3.73	3.89
E1	.390	.394	9.91	10.01	c1	.007	.011	0.18	0.28
E2	.306	----	7.77	----	e	.317 BSC		8.05 BSC	
E3	.383	.387	9.73	9.83	e1	.116	.124	2.95	3.15
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
G	.030 BSC		0.76 BSC		bbb	.006		0.15	
W1	.195	.205	4.95	5.21	ccc	.010		0.25	

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Product Documentation, Software and Tools

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Software

- .s2p File

Development Tools

- Printed Circuit Boards

Revision History

The following table summarizes revisions to this document.

Revision	Date	Description
0	17 August 2023	• Initial release of data sheet
1	21 December 2023	• Table 5, Moisture Sensitivity Level: package peak temperature updated to reflect actual test data, p. 2

Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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