StarCore DSP

StarCore SC3900FP

Flexible vector processor

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High-Performance Flexible Vector Processor Optimized for Wireless Infrastructure Applications

SC3900FP FVP Highlights

- Performance at 1.2 GHz
  - Up to 38.4 GMACS
  - Up to 19.2 GFLOPS
  - Up to 1.2 Tb/s memory bandwidth
- Architecture
  - Multiple instruction, multiple data
  - Up to eight instructions per cycles
  - Up to eight data lanes vector in a single instruction (SIMD8)
- High level programmability support
  - Up to 16 IEEE® single precision floating point operations per cycle
  - High performance for out-of-the box compiled DSP code
  - C, C++ and Embedded C support
- High-performance memory system
  - High bandwidth and data streaming capabilities
  - Clustering two SC3900FP cores under a 2 MB shared L2 cache
  - Hardware support for memory coherency between L1, L2 caches and the main memory
- Low power
  - Advanced low-power optimization methodology

Overview

Increasing demands of wireless data bandwidth have heightened the necessity for high-performance wireless infrastructure base station solutions.

The StarCore SC3900FP flexible vector processor (FVP) is the industry's highest performance next-generation communication DSP designed to address wireless infrastructure requirements for high-performance, low-power capabilities.

The SC3900FP is a binary compatible enhancement of the SC3900 core, adding mainly IEEE single precision floating point support, as well as other instruction set enhancements.

The high level of programmability of the SC3900FP core enables highly efficient and flexible implementation of the physical (PHY) layer of software-definable radio systems for existing and next-generation wireless standards of WCDMA, HSPA+, TD-SCDMA, WiMAX, LTE and LTE Advanced.

High-Performance Architecture for Wireless Infrastructure

The SC3900FP FVP is designed for wireless infrastructure, specifically PHY layer baseband applications. The PHY layer is not only composed of intensive and parallel DSP algorithms. Though these algorithms play an important role when offloading the highly regular/standardized ones to dedicated hardware accelerators like our Multi-Accelerator Platform Engine (MAPLE), what is left behind are complex, less parallel algorithms and control, which are usually OEM IPs.

PHY implementation can be placed into three main categories of functionality and based on levels of parallelism.

- Computation-intensive, highly parallel DSP code (mainly multiply-accumulate intensive)
- Data manipulation and less parallel DSP code
- Control code

Though highly dependent on the use case, the relative PHY processing requirements of each category are non-negligible when considering hardware acceleration of the most intensive functions.

Moreover, there is no clear separation between the different code categories for most functions. For example, control flow is often embedded in the middle of data manipulation functions, or data manipulation before, after, or even in the middle of a computation-intensive MAC kernel.

A solution that targets only one category, computation-intensive code (typical target for vector processors) for instance, will be ineffective in data manipulation, less parallel DSP kernels and in control code. This solution is less than optimal, as it results in higher power consumption and heat dissipation.

The SC3900FP FVP was augmented to accelerate baseband PHY processing from end to end, from computation intensive kernels to control code. To excel in computation intensive DSP processing, the SC3900FP introduces an optimized data path that includes very high memory bandwidth, matching register file and execution unit capacity supporting fixed point operations along with a variety of application-specific instructions.

Moreover, the SC3900FP data path is designed to be flexible, enabling each unit to execute different instructions and to access any register without penalty. This flexible data path is the essence of the FVP and enables customers to maintain high efficiency in less parallel DSP code where traditional vector processors become helpless and ineffective.

The SC3900FP instruction set includes extensive support for several data types, bit widths and SIMD levels, for both fractional and integer fixed point arithmetic, in addition to IEEE single precision floating point arithmetic. This flexibility allows the users to select the most suitable data representation for the calculation at hand.

Furthermore, the SC3900FP includes advanced control code features such as dynamic branch prediction, multiple predicates for calculating compound conditions and speculative execution.

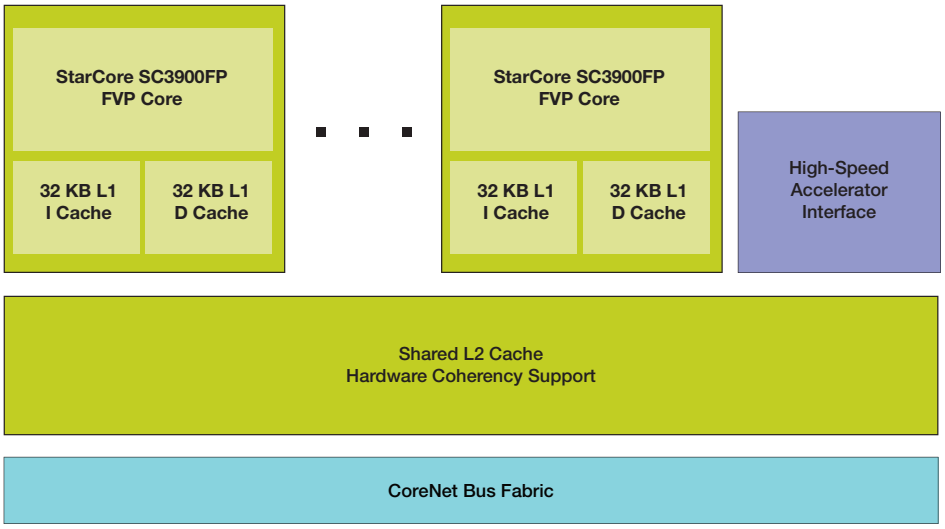
Table 1 provides examples of the performance improvement of the SC3900FP over the StarCore SC3850.

Table1: Performance Comparison: SC3900FP vs. SC3850

Function	Performance Improvement Factor SC3900FP vs. SC3850
FFT 2K Fixed Point	4x
Complex FIR	4x
Complex Matrix Multiplication	4x
Maximum Search	4x
LTE Descrambler	12x
LTE L1 Code Block Segmentation	8x
LTE L1 PRB Mapping	4x

According to a BDTI evaluation, the SC3900 attained the highest BDTIsimMark2000™ or BDTImark2000™ score recorded, with a huge advantage over competitors. Running at 1.2 GHz, the SC3900 outperforms the closest competitor's core running at 1.5 GHz by almost 2x. The BDTImark2000 and BDTIsimMark2000 provide a summary measure of signal processing performance. Visit BDTI.com for details.

Figure 1: StarCore SC3900FP Cluster



Multicore Support

The SC3900FP supports an advanced multicore technology, enabling multiple cores to be connected together to form a cluster of cores. The SC3900FP multicore approach considerably reduces the SoC fabric traffic and enables efficient code and data sharing. In addition, a dedicated accelerator port enables a direct and efficient connection of hardware accelerators directly to the shared L2 cache of the cores.

Each cluster is connected to the SoC through our CoreNet high-performance cache coherent fabric, delivering single-core programming simplicity into a multicore system. Coherency is supported by hardware throughout all memory levels inside cores, the clusters and the whole device.

Reduce Software Development and Time to Market

High-level programmability is essential to reduce development time, ease portability and reduce time to market. The SC3900FP is architecturally designed to enable optimizing C and C++ compilers, providing high-level programming support for both control and DSP code.

The SC3900FP compiler supports automatic vectorization, software pipelining and other advanced optimization techniques to achieve high C/C++ performance. Additionally, the SC3900FP compiler will support Embedded C, allowing the use of complex and fractional data types in high-level programming.

The memory system also has a critical influence on the development time and flexibility of a solution. A memory system based on tightly coupled SRAM memories (TCM) has two major drawbacks. First, fixed internal memory size implies constraints such as rigid allocation by limiting flexibility and recuding the ability to support multi-standard, multi-mode SDR. Secondly, in terms of programming simplicity and time to market, a system relying on DMA management implies scheduling overhead, even to reach the first non-optimized functional system.

The SC3900FP solves both issues by implementing a full cache-based memory. A cache-based system allows full flexibility and enables fast implementation of a functional system without the scheduling overhead of data movement. Flexible address translation and protection supported by the core-coupled MMU also contribute to faster application development by allowing a more abstract and protected software model.

To further accelerate time to market, the SC3900FP includes full support for hardware cache coherency based on our advanced CoreNet bus fabric, alleviating the burden from the software managing cache coherency. In addition, the SC3900FP provides TCM-like performance by introducing advanced, highly associative caches, pre-fetching mechanisms, partition and locking support which increase predictability and overall performance.

With an advanced memory system, the SC3900FP is the first DSP with true symmetric multi-processing capability, providing a high degree of flexibility that enables true multi-standard, multi-mode software-defined radio while significantly reducing software development and time to market.

Power efficiency is a fundamental requirement in modern systems as the level of integration increases.

Low-Power Methodology

Power efficiency is a fundamental requirement in modern systems as the level of integration increases. The power efficiency and energy savings of the SC3900FP is based on a low-power design methodology.

The SC3900FP was developed in an advanced low-power methodology spanning all stages of IP development. From the very early stage of the definition up to the layout implementation, power is constantly taken into account and optimized. The advanced methodology provides a significant advantage in terms of power reduction versus standard IP RTL and synthesis methodology.

Static power can be reduced by up to 80 percent by applying different techniques such as:

- Resource sharing: Reuse of the same logic for implementing different instructions
- Aggressive multi-threshold post optimization algorithm
- Automatic reduction in size of large cells in all sub-critical speed paths

Dynamic power can be reduced by up to 70 percent by applying different techniques such as:

- Semi-custom clock tree optimization (~20 percent power reduction)
- Extensive “fine grain” clock gating for all design sub-blocks
- Redundant transition elimination through control and data paths clear separation methodology

With state-of-the-art low-power optimization methodology, the SC3900FP sets a new standard in power efficiency for high-performance DSP processors.

Complete Development Tool Suite

The CodeWarrior Development Studio for SC3900FP provides a wide array of tools to help developers create applications for complex heterogenous multicore SoCs. The IDE is based on the Eclipse platform, allowing developers to leverage the support of the Eclipse community. Within the Eclipse framework, the build, debug, simulation and analysis tools are combined, unleashing the full potential of our high-performance DSPs. The tool suite includes:

- Feature-rich, Eclipse-based IDE
- High-performance C/C++ compiler
- Multicore debugger with multicore run control
- Extensive software analysis tools, including profiling and trace tools
- Royalty-free DSP SmartDSP OS with extensive driver support
- Advanced device simulation: Device instruction set simulator and performance accurate simulator
- Highly advanced software analysis tools, extended and integrated support for popular open source tools such as LTTng, OProfile and Valgrind
- The B4860QDS development board helps customers quickly develop software with the B4860 SoC
- The B4420QDS development board helps customers quickly develop software with the B4420 SoC

The CodeWarrior Development Studio for SC3900FP provides a wide array of tools to help developers create applications for complex heterogenous multicore SoCs.

The StarCore SC3900FP sets a new standard in performance and programmability.

Summary

Programmable DSP cores are the key processing elements in any mobile wireless infrastructure device. The StarCore DSP core is used in DSP and SoC devices deployed by many of the wireless OEMs in LTE, WCDMA, TD-SCDMA and WiMAX and has earned leading results from top benchmarking firms.

The StarCore SC3900FP sets a new standard in performance and programmability, enabling highly efficient and flexible implementation of software-definable, multi-standard and multi-mode radio systems.

For more information, visit freescale.com/StarCore

Document Number: BRSC3900DSPCORE REV 2