NXP I^{2}C-bus extender P82B715 in a proven application

Extend standard I^{2}C-bus devices without worrying about offset voltages

This analog bipolar IC lets you retain all the features of the standard I^{2}C-bus while easily extending its communication distance to 30 m or 3000 pF, well beyond the limits of the standard 400-pF bus.

Key features
- Dual, bidirectional, unity-voltage gain buffer
- Requires no external directional control
- Compatible with standard I^{2}C-bus
- Logic signal levels can include (but not exceed) supply and ground
- Logic signal input voltage levels are output without change, independent of V_{CC}
- 10x bus impedance transformation
- Wide supply voltage range (3 to 12 V)
- Clock speeds to at least 100 kHz and 400 kHz or beyond, depending on application
- ESD protection exceeds 2500 V HBM per Mil Std 883C-3015.7 and 400 V MM per JESD22-A115
- All I/O have diodes to V_{CC} and GND
- Latch-up free
  - Latch-up testing is done to JEDEC Standard D78, which exceeds 100 mA
- 8-pin SO and DIL packages

Applications
Upgrading standard I^{2}C-bus systems to:
- increase total connected capacitance
- easily drive signals over longer cables, up to 30 m
- drive larger I/O loads, including 30 mA Fm+
- improve noise immunity
- implement multi-drop signal distribution using low-cost, twisted-pair cables

The NXP P82B715 extends the reach of the I^{2}C-bus. It increases the drive capability of the data (SDA) and the clock (SCL) lines to 30 mA, the same level as Fast-mode Plus (Fm+).

Using one P82B715 at each end of a long cable (connecting Lx/Ly to Lx/Ly) reduces the cable's loading capacitance on the I^{2}C-bus by a factor of 10 (without changing logic voltage levels), and allows the total system capacitance load (all devices, connectors, traces, and wires connected to the I^{2}C-bus) to be around 3,000 pF. The loading on each I^{2}C-bus at the Sx/Sy sides remains below 400pF. (For details, see Application Note AN10710—*Features and applications of the P82B715 I^{2}C-bus extender.*)

Longer cables or low-cost, general-purpose, wiring can be used to link I^{2}C-based modules without degrading the noise margins. This can often be an attractive alternative to other I^{2}C-bus buffers, such as the P82B96, which require special voltage levels on one side but then provide complete isolation of the load capacitance on either side.

Multiple P82B715 devices can be connected together, linking their Lx/Ly ports in a star or multi-port architecture, as long as the total capacitance of the system is less than about 3000 pF

and each bus at an Sx/Sy connection is well below 400 pF. This configuration, with the master and/or slave devices attached to the Sx/Sy port of each P82B715, is capable of full multi-master communication.

The impedance-transforming action of the P82B715 means that a single, low-cost external transistor is all that's needed, when required, to implement logic voltage level translation.

There is no restriction on interconnecting the Sx/Sy I/O and, because the device output levels are always held within 100 mV of input drive levels, all the I/O are compatible with bus buffers that use voltage-level offsets. This feature makes the P82B715 attractive in AdvancedTCA applications that use radial IPMB and may use dynamic level-offset hot-swap buffers.

The logic levels can include (but not exceed) supply and ground. The logical signal input voltage levels are output without changes, independent of V_{CC}. When other system delays permit, the clock speed can reach at least 100 kHz and 400 kHz, depending on the application. The operating voltage range is 3 to 12 V and the operating temperature range is -40 to 85 °C. All the I/O have diodes to V_{CC} and GND, and, since the device is manufactured in a bipolar process that has no latching structures, operation is latch-up free. ESD protection exceeds Mil Spec and JEDEC standards, and the IC is available in 8-pin SO and DIL packages.
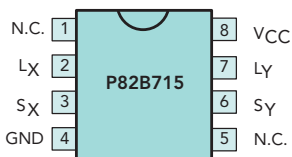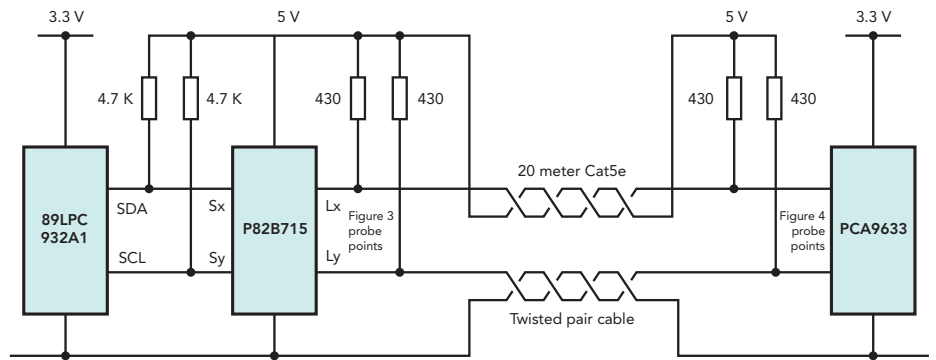
Figure 2. The P82B715 simplifies interfacing to the 30-mA drive levels of Fm+

Figure 3 shows the P82B715 interfacing between a standard I²C-bus processor (89LPC932A1) and the 30-mA drive levels of an Fm+ slave (PCA9633). The P82B715 enables direct connection to an Fm+ bus and supports the Fm+ slaves operating at the lower frequencies required by large bus-capacitance loading or long cables. The controlled rise-and-fall edge rates of the P82B715 minimize ringing on long cables while the system is running at 400 kHz, as shown in the waveforms.
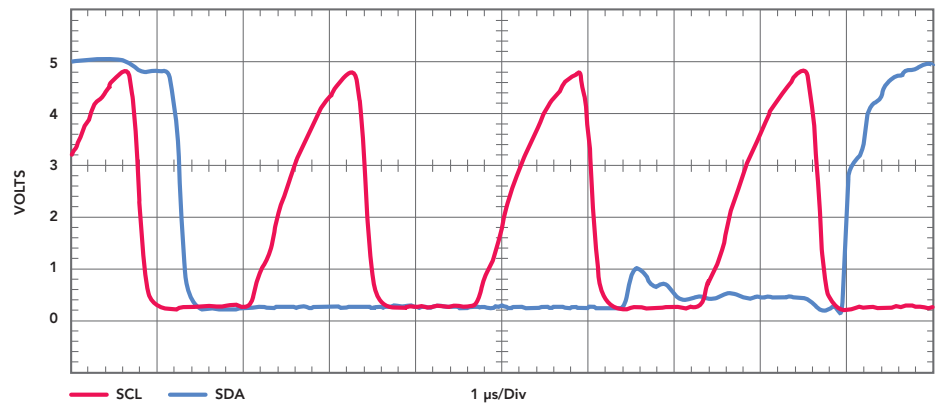
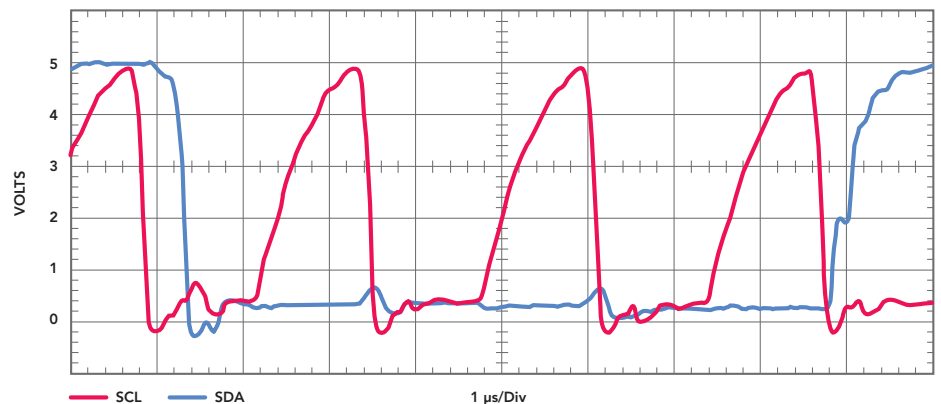Figure 3. The waveforms at the P82B715 end of the 20-m cable

Figure 1. Pin configurations

Figure 4. The waveforms at the PCA9633 end of the 20-m cable

Proven circuit with the P82B715

With many variables - cable length/ capacitance, local capacitive loading on each I²C-bus, bus voltages, and bus speed – optimizing a design can be complex and requires significant study of the Application Note. The following circuit and simplified approach (Figure 5) has been checked to provide adequate performance in the typical 100-kHz application and can be easily implemented by using the values and circuit shown for a point to point application (up to 30 m), and, if additional nodes need to be added along the way, in multi-point applications.

Figure 5. P82B715 circuit
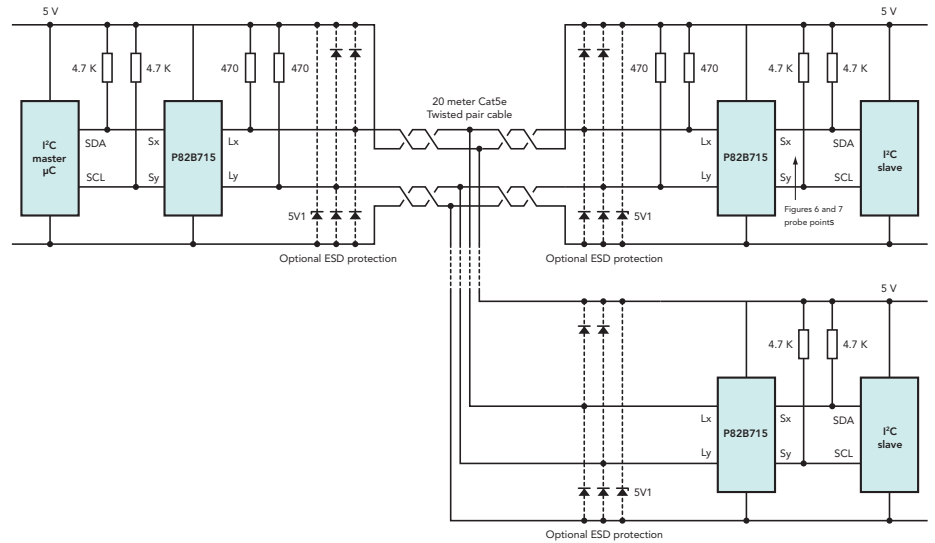
Note: Cable bus pull-ups only fitted at the cable ends, not fitted to modules connected along cable.

The P82B715 vs. the P82B96

Figure 6 shows the I²C-bus waveforms from the long-distance line as seen by the slave on the P82B715 Sx/Sy I/O. Notice that the offset is small and the static levels remain under 0.4 V. Coupling of SDA to SCL is negligible when SCL is low, but slight cross-coupling of SCL to SDA is visible when SDA is high (and therefore higher impedance). The waveforms are very clean and will easily support all available I²C masters and slaves.
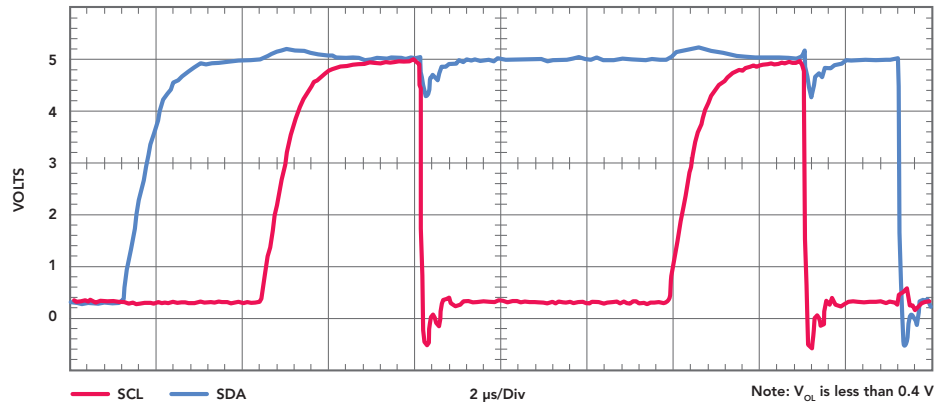
Figure 7 shows the waveforms on the Sx/Sy I/O as seen by the slave when a P82B96 is substituted. The P82B96 uses a static level offset on the slave side to isolate noise and loadings on either side of the device. The nominal offset is 0.8 V. That V_{OL} level may create worst-case design tolerance problems with slave devices that do not use I²C switching levels, for example TTL levels. It also precludes operation with other bus buffers using special non-compliant I²C levels. The lower V_{OL} level, combined with the ability to operate with any master, slave or bus buffer, is the primary advantage of using the P82B715 for long-distance buses. However, the P82B715 does not isolate bus capacitance, the way the P82B96 and the improved PCA9600 do.

Figure 6. Clock and data signal output at Sx/Sy from a system with P82B715 at each end of a 20m cable
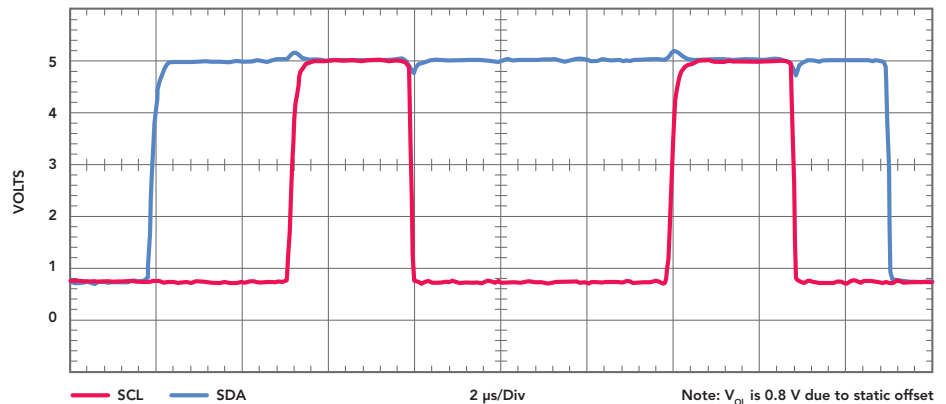

Figure 7. Clock and data signal output to a slave from Sx/Sy of a P82B96 replacing the P82B715
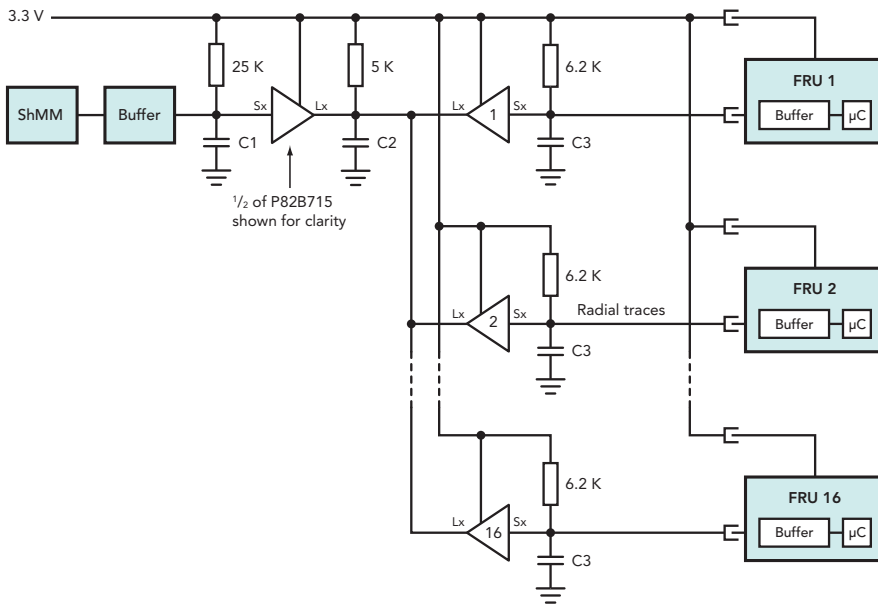
Figure 8. The P82B715 used to distribute signals in an IPMB analog radial shelf

Diagram labels: 3.3 V, ShMM, Buffer, 25 K, 5 K, 6.2 K, Sx, Lx, C1, C2, C3, ½ of P82B715 shown for clarity, FRU 1, FRU 2, FRU 16, Buffer, µC, Radial traces

Advanced TCA Architecture

In Figure 8, total system capacitance is 2,800 pF, distributed over 16 bus sections with approximate capacitances: shelf manager buffer bus C1 = 40 pF, common Lx bus C2 = 200 pF, and each radial distribution trace, including FRU load, C3 = 160 pF. Each individual bus section is designed to rise at least as fast as the IPMB requirement by setting R1 to 25 k, R2 to 5 k, and each R3 to 6.2 k. Typical bus offset (i.e. increase bus low level), measured between any two Sx points, is less than 100 mV.

For more information, visit www.nxp.com/i2clogic

Features and design guidelines

P82B715 characteristic	How it simplifies design	Restrictions
Bus logic signal levels are independent of V_{CC} supply	Handles all logic voltages in the range 0 V to V_{CC}	Logic voltage levels must be less than V_{CC}
Wide supply voltage range (3 to 12 V)	Can handle all logic levels up to 12 V	Less performance for supplies below 4.5 V, but typically retains full performance at 3.3 V
Supports simple paralleling of multiple ICs on its input or output sides	Supports all bus configurations, on input and output sides, including star and multi-drop architectures	Usual I²C-bus limitation of 400 pF (effective) applies on the Sx/Sy side and 10x scaled limit on Lx side.
10x drive capability on one side (Lx/Ly)	Driving low-impedance buses with large capacitance (to at least 3,000 pF) or driving long cables. Can drive 30 mA Fm+ devices.	Load on Lx side is not isolated. It is "transformed" so it appears at 1/10 actual load. Cable limit of about 40 m
Output bus signal voltage always equals input bus signal voltage (max. difference of 100 mV)	Does not alter the bus-logic levels used by I²C-bus or any derivative buses using TTL levels, such as SMBus. Even compatible with buffers having special (low) switching levels that are not compliant with the I²C-bus or TTL.	Logic voltage level shifting is not supported, but is easy to implement with only a few low-cost components
Controlled slew rate	Minimizes ringing and/or overshoot when driving long cables. Highly tolerant of different cables and configurations	Datasheet limits should be observed. Add conventional components for maximum protection
Has clamp diodes from I/O to V_{CC}	Improved ESD and overload characteristics	Not allowed by Fast-mode specifications, but can be used with the understanding that it will pull the connected buses low if the P82B715 V_{CC} supply fails

Order information

Package	Container	Package drawing	Part number
SO8	Tube	SOT96-1	P82B715TD,112
SO8	Tube and reel	SOT96-1	P82B715TD,118
DIP8	Tube	SOT97-1	P82B715PN,112